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Saptarshi Das  
*Doctoral Student*, sdas@purdue.edu

Joerg Appenzeller  
*Birck Nanotechnology Center, Purdue University*

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FETRAM. An Organic Ferroelectric Material Based Novel Random Access Memory Cell

Saptarshi Das†‡ and Joerg Appenzeller†‡

†Department of Electrical and Computer Engineering and ‡Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States

Supporting Information

ABSTRACT: Science and technology in the electronics area have always been driven by the development of materials with unique properties and their integration into novel device concepts with the ultimate goal to enable new functionalities in innovative circuit architectures. In particular, a shift in paradigm requires a synergistic approach that combines materials, devices and circuit aspects simultaneously. Here we report the experimental implementation of a novel nonvolatile memory cell that combines silicon nanowires with an organic ferroelectric polymer—PVDF-TrFE—into a new ferroelectric transistor architecture. Our new cell, the ferroelectric transistor random access memory (FeTRAM) exhibits similarities with state-of-the-art ferroelectric random access memories (FeRAMs) in that it utilizes a ferroelectric material to store information in a nonvolatile (NV) fashion but with the added advantage of allowing for nondestructive readout. This nondestructive readout is a result of information being stored in our cell using a ferroelectric transistor instead of a capacitor—the scheme commonly employed in conventional FeRAMs.

KEYWORDS: Nonvolatile memory, ferroelectric, organic polymer, nanowire

Ferroelectric materials have two stable spontaneous polarization states due to their low crystal symmetry. Hence these materials are a natural choice for binary code based nonvolatile RAM applications. Moreover, ferroelectric switching, a process of changing the polarization state of the ferroelectric by applying an appropriate external electric field, is intrinsically fast and hence can be employed for high-speed read and write memory operations with typical read/write times in the nanosecond range. To add to the advantages of ferroelectric memories, it has been experimentally found that FeRAMs are extremely endurable, meaning that their polarization state can be changed as many as 10¹⁴ times without fatigue. At the same time, the supply voltage has been continuously scaled down through progress in the field of thin film technology to ensure low power operation. Commercial one transistor one capacitor (1T1C) nonvolatile FeRAM technology is therefore considered an adequate solution for high speed, high endurance, and low power applications. The biggest challenge that conventional FeRAM is currently facing is that it suffers from destructive readout and that it poses problems when it comes to integration with conventional complementary metal–oxide semiconductor (CMOS) technology. As a consequence, FeRAMs only hold a relatively small part of the overall semiconductor market share if compared to FLASH memories.

The FETRAM proposed in this article overcomes the destructive readout problem by replacing the memory capacitor of a 1T1C FeRAM cell by a memory transistor. The data are stored in the ferroelectric gate oxide of the transistor while the readout is performed by interroging the conductance of the semiconducting channel of the transistor. Ferroelectric field-effect transistors (FeFETs) operating as resistive memory storage have been reported in the past by several groups for nondestructive readout operation. However, FeFETs discussed previously are based on crystalline ferroelectrics and thus lack compatibility with conventional silicon CMOS processes and are unavailable in a “top-gated” geometry for the same reason. Most importantly, because of the absence of a scheme to individually gate FeFETs implementation into a complete memory cell has not occurred as of yet.

Here we report a fully integrated novel approach that combines for the first time silicon nanowires and an organic polymer into a ferroelectric field-effect transistor based 1T1T memory cell. Our cell addresses all of the above challenges in terms of durability, compatibility with silicon CMOS, and scalability and is believed to be a viable option for the implementation into future generations of integrated circuit.

In detail the materials, device, and circuit advantages our approach offers are as follows:

The organic ferroelectric PVDF-TrFE has a low crystallization temperature (200 °C) and therefore is expected to form a ferroelectric film on a semiconducting substrate without any chemical reaction, a feat difficult to accomplish with crystalline ferroelectrics (PZT, BST, etc.). Since the dielectric constant of PVDF-TrFE is comparable to any interfacial layer that might be formed during the
crystallization process, the depolarizing field is small and stable operation is ensured. Moreover uniform thin films of the organic ferroelectric polymer PVDF-TrFE can be obtained by simple spinning techniques. Use of silicon nanowires as channel material for readout operation is motivated by two aspects. First, utilizing silicon in our demonstration as the channel material emphasizes the compatibility with conventional CMOS technology and, second, it underlines the potential of our approach for future scaling since nanowires as ultrathin body channels enable aggressive channel length scaling through improved electrostatic gate control if compared to their bulk or thin film planar device counterparts.16,17

Figure 1a shows how the novel FETRAM compares with a state-of-the-art FeRAM cell. Figure 1b illustrates schematically the ferroelectric memory transistor. In a conventional FeRAM cell the word line (WL) enables the control transistor (CT) for both read and write operation. For the write operation the bit line (BL) is charged to an appropriate voltage to enforce the state of the memory capacitor. For read operation the BL is charged to a predefined voltage so that a current which is associated with the switching of the polarization in the memory capacitor is detected in the sense line (SL). Due to the nature of the readout mechanism, this process is destructive and any data have to be rewritten into the cell. On the other hand, the FETRAM cell does not suffer from the same drawback. By replacing the ferroelectric memory capacitor by a ferroelectric memory transistor (MT), nondestructive readout is ensured. In the present example the control transistor (CT) is a depletion mode transistor which is in its conductive state (normally ON) when no gate bias is applied. This is why in order to perform the write operation, the WL is grounded which allows the BL voltage to be transferred to the gate of the memory transistor. Since MT has a ferroelectric insulator layer as gate oxide, the BL voltage enforces the ferroelectric to switch its polarization corresponding to the applied bias. When the BL voltage is positive (negative) 20 V, the dipoles in the ferroelectric are polarized in the upward (downward) direction which will be referred to as binary state “0” (“1”) as shown in the band diagram of the FeFET in Figure 1d. When the write voltage is removed from BL, the energy bands in the channel attempt to readjust toward their original equilibrium positions. However, the polarization charges in the ferroelectric oxide create a residual electric field which prevents this band movement. The exact position of the energy bands is determined by the respective orientation and strength of the polarization dipoles in the ferroelectric gate insulator as shown in Figure 1d. The dipole field in the ferroelectric is ultimately responsible for the nonvolatility of ferroelectric memory transistor. It is important to note that the write operation is similar to the conventional FeRAM cell with the only difference that WL is kept at ground potential to activate CT as it operates in depletion mode. For the read operation a positive voltage of 15 V is applied to WL to turn off the control transistor and thereby disconnecting BL from the memory transistor. Since the word line is also connected to the drain of the memory transistor (note that the source is grounded), a dc current is detected in the sense line whose amplitude depends on the polarization state of the ferroelectric. Figure 1c shows the desired transfer characteristics of the memory transistor. When MT is put into binary state “0” (green dot), the polarization of the ferroelectric ensures that the valence band of the channel material lies below the source and drain Fermi levels and hence no current can be detected. However if MT is put into binary state “1” (red dot), the polarization of the ferroelectric ensures that the valence band of the channel material lies above (or at least between) the source and drain Fermi levels and current can flow from source to drain (see also band diagram in Figure 1d). The above discussion implies that the state of the memory transistor after writing can be determined by reading the magnitude of the current through the channel of the memory transistor. Since the read out is performed by evaluating the magnitude of the current, it does not destroy the polarization state of the ferroelectric. Thus, the novel FETRAM cell not only is nonvolatile but also allows for nondestructive read out. The truth table for the FETRAM cell is shown in Figure 1e. Note that the read and write operations for the FETRAM cell are mutually exclusive improving the noise margin for the cell.
It is important to realize that for a finite voltage difference between the source and the drain of the memory transistor there will always be a potential drop inside the channel during the read out operation. To design the individual devices within the cell properly is the key in order to prevent that the associated depolarizing field is able to switch the ferroelectric polarization. Various scaling aspects need to be carefully considered in this context: It is desirable to reduce the ferroelectric film thickness to reduce the switching voltage and hence power consumption for next generations of FETRAMs. In order to avoid that the depolarizing field in the channel of the memory transistor becomes too large under these conditions, the channel length of MT needs to be scaled simultaneously. That in turn allows reducing the voltage at the word line. Our choice of nanowire devices is motivated by their ultrathin body nature that enables aggressive scaling in the above-mentioned context. Reducing the readout voltage however requires that the control transistor is scaled simultaneously since it is the voltage at the word line that ultimately turns CT on and off. The same argument as for MT now applies for CT and requires aggressive scaling of the gate oxide thickness and channel length of the control transistor emphasizing again the use of nanowires as channel material. In summary, the channel lengths and gate dielectric film thicknesses of both transistors need to be scaled simultaneously to ensure proper cell operation at low supply voltages.18

The reader might argue that the use of two transistors in the 1T1T FETRAM cell to store 1 bit of data occurs unnecessary since MT alone is capable of nonvolatile and nondestructive operation. However, for integration of the FETRAM cell into a memory array architecture, the use of CT is essential to select a particular memory word. Moreover, our cell layout, while utilizing two transistors, does not require two independent word lines for writing and reading, an advantage that compensates for the added complexity through the use of two FETs in our structure.

The complete set of fabrication steps for the FETRAM cell is shown in Figure 2. Silicon nanowires with body thicknesses in the range of 50–100 nm were spun onto a 100 nm silicon dioxide (SiO2) substrate with underlying highly doped silicon. Dry oxidation was carried out at 950 °C for 10 min to form a 4–6 nm shell of SiO2 around the Si nanowires to be used as top gate dielectric for CT. The top gate for the control transistor was patterned utilizing electron-beam lithography followed by 80 nm aluminum deposition and acetone lift-off (Figure 2a). Source and drain contacts for both CT and MT were fabricated using the same technique as described above, with the only difference that the SiO2 shell was removed in the contact areas using diluted BOE solution prior to metal deposition (see Figure 2b). Organic ferroelectric polymer PVDF-TrFE (80:20) pellets, were dissolved in methyl ethyl ketone (MEK) solution (PVDF-TrFE was 2% by volume), and the liquid was then spun onto the sample at 4000 rpm to produce a 100 nm ferroelectric film. By adjustment of either the composition of the solution or the spin speed, the thickness of the polymer layer can be adjusted.19 Finally, a stack of 10 nm aluminum and 90 nm titanium was deposited to create the top gate for the memory transistor. A fluorinated plasma was used to etch the metal stack (30 nm/min), and an oxygen plasma was employed to remove the polymer (120 nm/min) (see Figure 2c). An SEM image of the completed memory cell and its cartoon projection are depicted in Figure 3.

Figure 4a displays the measured transfer characteristics of the memory transistor within the FETRAM cell corresponding to a gate bias sweep from negative 20 V to positive 20 V and then again back to negative 20 V. When −20 V is applied to the gate, the dipoles in the ferroelectric gate insulator are switched in the downward direction as explained in the context of Figure 1 and the high current state is enabled. As the gate bias is increased, the valence band moves somewhat downward but still remains above the source and drain Fermi levels at zero gate bias due to the residual field in the ferroelectric as shown in Figure 1d (upper right). Increasing the gate bias beyond zero volts eventually moves the valence band below the source and drain Fermi levels and blocks the current flow. If the gate bias is still increased further, the conduction bands start to contribute to current flow...
and the current increases again. For the sweep from the positive gate voltage direction, when +20 V is applied, the dipoles in the ferroelectric gate insulator switch to the upward polarization direction as shown in Figure 1d (lower left). In this case, sweeping the gate bias to \(-20\ V\) results in the same curve as before but shifted toward the left due to the different polarization of the ferroelectric. In other words, the threshold voltage of the semiconductor channel is different for different orientations of the dipoles. Comparing the experimental device characteristics with the transfer characteristics of Figure 1c clearly shows that the desired high and low current states can be enabled provided that the polarization of the ferroelectric and the corresponding threshold voltage shift does not result in a complete overlap between the electron (right) and the hole (left) branch of the characteristics in Figure 4a.

A back gate bias of \(-30\ V\) was used to further enhance the on-state conductance of the silicon nanowire channel, in turn increasing the memory ratio (the ratio of currents in the two memory states). In general doping would be used instead of a back gate voltage to obtain the same current drive capability. It is important to note that the apparent hysteresis in the transfer characteristics of our device is mainly a result of the ferroelectric properties of the gate dielectric. While hysteresis in transfer characteristics frequently occurs due to trap and fixed charges in the dielectric, hysteretic behavior due to charging of a dielectric film cannot be utilized for memory applications since its effect decays quickly (typically within minutes) over time. In order to characterize the retention time of the ferroelectric memory transistor, we have performed a time domain measurement. During this measurement WL and SL were grounded and a switching voltage (+20/−20 V) was applied to BL. Next the bit line was grounded and WL was charged to 15 V. Readout current was measured as a function of time as shown in Figure 4b. Two distinct readout current values with a memory ratio \((I_{Hi}/I_{Lo} - 1) \times \%\) of 7990% and long retention period (more than 3 h) were observed. To further ensure that the retention in the FETRAM cell is indeed due to the ferroelectric behavior of the gate dielectric, we also characterized as a point of reference nanowire devices with a gate dielectric from SiO2 with the same 100 nm thickness. All of these devices showed some initial hysteresis that disappeared however within typically 100 s because of the expected lack of any memory property of SiO2.

![Figure 4](Image URL)  
Figure 4. (a) Transfer characteristics of the memory transistor for the respective sweep directions. The red dot shows the current through the device after applying negative 20 V gate bias and the green dot is the current through the device after applying positive 20 V gate bias. (b) Memory retention characteristics of the ferroelectric memory transistor at a back gate bias of \(V_{BG} = -30\ V\).

Figure 5 demonstrates the different operational regimes of the FETRAM cell and corresponding states of WL, BL, and SL. During the first voltage cycle WL is grounded and therefore writing is enabled. However, no read current can be measured because of the lack of a drain-to-source voltage difference at the memory transistor. During the second voltage cycle WL is biased at 15 V enabling the read out current to be detected in the sense line. The magnitude of the read out current corresponds (as expected) to the “1” state which was written during the first voltage cycle. Similar measurement results were obtained during the fourth voltage cycle with the difference that now the memory state “0” is detected which had been previously written during the third voltage cycle. To further test the reliable operation of the cell, the word line was biased for read operation in the fifth and sixth voltage cycle while different voltages were applied to the bit line. As evident from the current measurements, the cell is completely unaffected by the bit line voltage—as desired—under read conditions. In summary, Figure 5 clearly provides compelling evidence that the novel FETRAM cell provides all the desired functionality.

![Figure 5](Image URL)  
Figure 5. Measurement of the read out current as a function of different combinations of WL and BL voltages corresponding to different functional states of the FETRAM cell.
In conclusion, we have proposed and demonstrated a novel, fully functional, CMOS compatible 1T1T memory cell that allows for nondestructive readout operation using an organic ferroelectric—PVDF-TrFE—as memory storage unit and a silicon nanowire as channel.

ASSOCIATED CONTENT

Supporting Information. Fabrication of PVDF-TrFE thin film. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author
*E-mail: sdas@purdue.edu.

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