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Identification, Characterization, and Implications of Shadow Degradation in Thin Film Solar Cells

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Abstract— We describe a comprehensive study of intrinsic reliability issues arising from partial shadowing of photovoltaic panels (e.g., a leaf fallen on it, a nearby tree casting a shadow, etc.). This can cause the shaded cells to be reverse biased, causing dark current degradation. In this paper, (1) we calculate the statistical distribution of reverse bias stress arising from various shading configurations, (2) identify the components of dark current, and provide a scheme to isolate them, (3) characterize the effect of reverse stress on the dark current of a-Si:H p-i-n cells, and (4) finally, combine these features of degradation process with shadowing statistics, to project ‘shadow-degradation’ (SD) over the operating lifetime of solar cells. Our results establish shadow degradation as an important intrinsic reliability concern for thin film solar cell.

Keywords – Thin film solar cells, voltage stress, performance degradation, reliability

I. INTRODUCTION

Reliability has always been crucial to the economic viability of photovoltaic (PV) technologies [1]. Consequently, the safety issues like hot-spot breakdown [2], and parametric degradation issues like light induced degradation have been studied extensively [3]. One such problem arises due to partial shadowing of the panel, which results in a reverse bias appearing across the shaded cells [4]. The problem of shadowing of solar panels has been studied for quite some time; however, the work has focused primarily on the drop in system energy-yield due to partial shadows [5]. On the device level, the reverse bias caused by shading can also result in long term performance degradation of the shaded cells. In the worst case, the shaded cells may also undergo catastrophic reverse breakdown.

In case of crystalline cells, the problem is avoided by using a bypass diode in parallel to the cell [6]. However, the large area deposition processes, typically used in thin film PV technology, make insertion of such bypass diodes impractical. Consequently, the panel is susceptible to parametric failure due to reverse stresses induced by shadowing. Therefore, a thorough understanding of the effects of reverse bias stress, especially on long term stability and performance of thin film solar cells becomes very important. We note that the SD is a generic reliability concern for all thin film PV technologies, however, in this paper we illustrate the issue with reference to a-Si:H cells.

II. EFFECT OF SHADOWING

The equivalent circuit shown in Fig 1a identifies the main features of a solar cell. The two current components of a solar
I-V characteristics, namely dark (\( I_{\text{Dark}} \)) and light (\( I_{\text{Photo}} \)) currents, are shown shaded. The dark current is a combination of an exponential diode current (\( I_D \)) in parallel with a parasitic shunt current (\( I_{\text{SH}} \)). The photocurrent component is typically represented by a voltage-independent current source (\( I_{\text{PH}} \)) in parallel with the diode and shunt resistance. In order to obtain high panel output voltage, approximately 100-200 nominally identical cells are connected in series. In case of thin-film cells, this series connection is accomplished in following steps: patterning of TCO on glass by laser scribing, deposition of the semiconductor layer/s (PECVD for a-Si:H, sputtering for CIGS/CdTe), another scribing step to pattern the semiconductor layer, deposition of back contact, and final scribing and isolate, result in a structure shown in Fig. 1b.

This series connection is responsible for the reverse voltage stress due to shading. Under normal operating conditions the panel is biased at the maximum power point voltage (MPPV). For a-Si:H cells, this translates to \( V_{\text{cell}} \approx 1 \) V. Now, if some of the cells are accidentally shadowed, the photocurrent of the affected cells is suppressed (\( I_{\text{PH, shade}} < I_{\text{PH}} \)), and the new operating point will shift to \( V_{\text{cell, shade}} < 1 \) V. Depending on the number of cells shaded and the loss in photocurrent, \( V_{\text{cell, shade}} \) could be negative depending on the shading conditions [5, 7].

![Figure 2: (a) Measured dark IV of typical a-Si:H solar cell (squares), with the shunt current (\( I_{\text{SH}} \)) dominated region (\( V > -0.5 \) V), and diode current (\( I_D \)) dominated region (\( V < -0.5 \) V) shown shaded. (b) Schematic showing the p-i-n solar cell structure with a p-i-n shunt in the left formed due to Al diffusion and counter doping. Simulated dark IV of the structure shown in schematic (b) reproduces the qualitative features of \( I_{\text{Dark}} \), along with the shunt and diode dominated regimes (shown shaded). (i) The potential (contours) and current (quiver) distribution in shunt dominated regime shows current crowding in the p-i-n shunt region; (ii) at higher biases the diode current through p-i-n region takes over and current flow is more uniform.

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To determine the new operating point, we simulate a panel of 200 identical cells connected to a load resistance of \( R_L \). Initially, the cells are assumed to be operating at the MPPV. For an accurate estimate of the change in operating condition under shading through the simulations, we use a spline-fit of the measured dark IV characteristics and a constant current source for \( I_{\text{PH}} \) effectively mimicking the equivalent circuit in Fig. 1a. Fig. 1c shows the contour plot of the reverse voltage developed across each of the partially shaded cells, as a function of the degree of shading and number of cells shaded. This plot of the reverse voltage demonstrates that in majority of cases, when multiple cells are shaded partially (\( 0 < I_{\text{PH, shade}} < I_{\text{PH}} \) & \( N_{\text{shade}} > 1 \)), the shaded cells are stressed only at low to moderate reverse bias (\(< ~-5V\)). Extreme reverse biases (\(- 15V\)) causing hot-spot breakdown can only occur if one or a few cells are shaded completely (\( I_{\text{PH, shade}} = 0 & N_{\text{shade}} = 1 \)).

Fortunately, the form factor of the cells ensures that the probability of worst case shading is statistically rare and catastrophic hot-spot failure is unlikely for typical operating conditions. However, partial shadowing is more probable, which would result in moderate reverse stress on the shaded cells for the duration of shading. We find that such reverse stress leads to a parametric degradation in cell efficiency due to increase in dark current (e.g., a -5V stress for \( 10^4 \) sec can reduce the efficiency by 10% in the worst case). Since, it is impossible to control the random shading events, it becomes important to understand its mechanisms and effects clearly to predict the effect of shadow degradation on panel output over its operating lifetime.

### III. DARK CURRENT

#### A. Features of the dark current

In order to precisely understand the effect of shadow degradation on IV characteristics, it is important to understand the components of solar IV characteristics. The dark current (\( I_{\text{Dark}} \)) of a solar cell is known to consist of two components; an exponential diode current (\( I_D \)), and a parallel symmetric, non-ohmic shunt current (\( I_{\text{SH}} \)), so that \( I_{\text{Dark}} = I_D + I_{\text{SH}} \) [8]. At lower biases the non-ohmic shunt current dominates, while at higher biases the exponential diode current takes over, as shown by shaded regions in Fig. 2a. The shunt current is parasitic component and its magnitude varies from cell to cell even when they are manufactured under nominally identical conditions. The non-ohmic shunts have been observed in all types of solar cells [8, 9]. In case of thin film cells, this shunt current mechanism has been identified as space-charge-limited (SCL) current [10] through parasitic paths formed at different locations on the cell surface.

In a-Si:H p-i-n solar cells, these parasitic shunt paths are consistent with the hypothesis of aluminum incursion in the a-Si:H from the top ZnO:Al of the n contact [11]. This Al can counter-dope the material to p type, and result in a p-i-p parasitic structure, as opposed to the normal p-i-n device (see Fig. 2b) [10]. This parasitic p-i-p path will result in a SCL shunt current in parallel to the exponential diode current through the p-i-n device. Self consistent simulation of the 2D structure shown in Fig. 2b reproduces the measured dark IV with the shunt (marked (i)) and diode (marked (ii)) current dominated regimes (Fig. 2c). The contour and quiver plots in Fig. 2c show the current and potential distribution in different regimes of operation. In reverse and low forward biases (region (i)), the p-i-p shunt path provides the lowest potential barrier resulting in the localized SCL shunt current (arrows). At higher biases the diode current through the bulk p-i-n device becomes large enough and overtakes the shunt component (region (ii)). This results in uniform current flow through the device (see quiver plot in Fig 2c (iii)).
increase in dark current. Therefore for finding the forward didoe current we can separately by observing both degradation behavior of dark current (see Fig. 3a). This simple subtraction scheme provides a powerful method to isolate the two components of dark IV by ‘cleaning’ forward current. This means that we can now study the shadow-induced degradation of shunt current (I_{SH}) and diode current (I_D) components individually.

B. ‘Cleaning’ the forward dark IV

This analysis of the parasitic shunt current and bulk diode current components of the dark IV (Fig. 3a) allows us to identify the diode (I_D) and shunt (I_{SH}) current components of the dark current (I_{Dark}). Moreover, this picture can help us isolate the I_{D,fwd} from the measured I_{Dark}, by using the symmetry of I_{SH} about V = 0 point. From Fig. 3a we see that in reverse bias I_D << I_{SH}, this means that I_{Dark} = I_{SH} in reverse bias. Therefore for finding the forward diode current we can subtract the reverse shunt current (i.e., I_{D,fwd} = I_{Dark,fwd} – I_{Dark,rev}, see Fig. 3b). This simple subtraction scheme provides a powerful method to isolate the two components of dark IV by ‘cleaning’ forward current. This means that we can now study the shadow-induced degradation of shunt current (I_{SH}) and diode current (I_D) components individually.

IV. REVERSE DEGRADATION MEASUREMENTS

Fig. 4 shows the pre (squares) and post (circles) stress dark IV of a cell (-5V stress for 10^4 s), showing a significant increase in dark current I_{Dark} after stress. It is apparent that both I_D and I_{SH} increase significantly due to the stress. The degradation behavior of I_D and I_{SH} can be monitored separately by observing I_{Dark} at -0.4V (as I_{Dark} ~ I_{SH} here) and ‘cleaned’ I_{Dark} at 0.8V (as I_{Dark} ~ I_D here). This allows us to identify and characterize the degradation of these current components separately, as discussed next.

A. Diode current degradation – I_D(V_R, t)

In order to identify the features of the degradation mechanism, 22 devices were subjected to stresses ranging from -3V to -7V for a duration of 10^4 s each. Fig. 5a shows that time dependence of diode current degradation ΔI_D(t) for various reverse biases is described by robust power-law (ΔI_D(t) ∝ t^n). The power exponent n of the power law is ~ 0.2-0.26, across 22 devices measured. The voltage dependence of the ΔI_D can be obtained from the pre-factor (K(V_R)) of the power-law fit (ΔI_D = K(V_R)t^n) of the time dependence data. We find that the dependence of ΔI_D stress voltage (V_R) is rather weak, but higher degradation can be observed with higher stress (Fig 5b). Interestingly we find that the power exponent n is independent of stress voltage V_R (Fig. 5b inset).

Another feature of the I_{Dark} degradation is the distinct relaxation behaviors of diode and shunt current components. While diode current I_D relaxes to its original value after about a week of relaxation in a dark chamber. The shunt current degradation (ΔI_{SH}) on the other hand appears to be permanent (Fig. 6a). The relaxation kinetics for ΔI_D also shows power-law time dependence, similar to degradation kinetics (Fig. 6b).
Although the physics of time-exponents and weak voltage dependence are not explicitly known, the general features of time and voltage dependencies of degradation and relaxation phenomena \( I_D(t, V_R) \) suggest metastable defect generation in a-Si:H, due to reverse stress. The most likely cause is metastable defect creation near the midgap due to breaking of Si-H bonds. [12]. In order to explore this hypothesis for diode current degradation, we measured 14 small area devices, which exhibited no shunt current \( (I_{SH} = 0) \). This allowed us to probe the diode current in the voltage range (-1V to 1V), without any contamination from \( I_{SH} \). For these small area devices, we observe an asymmetrically high increase in \( I_D \) at low biases (Fig. 7a). The current increase at low biases is much faster compared to higher biases. This is reflected clearly in the power exponent of \( \Delta I_D(t) \) at different values measurement voltages from -0.8V to 0.8V. The exponent decreases monotonically from ~0.95 at -0.8V to ~0.25 at 0.8V measurement voltage (Fig. 7b). Note that the power exponent value of 0.25 at measurement voltage of 0.8V, obtained from these devices with \( I_{SH} = 0 \), coincides well with the power exponent obtained from the large area devices through 'cleaning' the shunt current (Fig. 5b inset). This shows the effectiveness and usefulness of the cleaning technique in reliability characterization experiments.

![Figure 7](image_url)

**Figure 7**: (a) Time evolution of Dark IV at reverse stress of -5V for 10^3s, for a small area device with \( I_{SH} = 0 \), shows disproportionately high increase in \( I_D \) at low biases. (b) The power exponent \( n \) of time dependence (\( I_D \sim t^n \)) shows a monotonic dependence on measurement voltage (showing and average of 14 devices measured). The value of \( n \) at \( V = 0.8V \) also coincides well with the power exponent obtained from 'cleaned' diode current of large area devices.

Note that in case of a-Si:H cells, the diode current \( I_D \) is dominated by recombination in the i-layer. This means that the ideality factor for a-Si:H p-i-n diodes is \( \sim 2 \). Therefore, an increase in midgap defects leading to higher recombination would imply an equal increase in current at all voltages between -1V and 1V. However, as apparent from Fig 7a, the current increase at reverse and low biases is much larger than the high bias regime. This asymmetry in the degraded diode current cannot be explained through increased recombination in the i-layer alone. Further experimental studies are required to clarify this degradation mechanism further.

### B. Shunt current degradation – \( I_{SH}(V_R,t) \)

The shunt current \( I_{SH} \) also increases due to stress (as seen in Fig 4, moreover, this increase in \( I_{SH} \) is permanent. However, unlike \( \Delta I_D(t) \), the time dependence of \( I_{SH} \) does not show a clean monotonic trend (Fig. 8a). The voltage dependence of shunt current \( (\Delta I_{SH}(V_R)) \) on the other hand shows weak increasing trend (Fig. 8b), for the 22 devices measured.

![Figure 8](image_url)

**Figure 8**: (a) \( \Delta I_{SH}(t) \) for the same 3 devices from Fig. 5a, shows more noisy time dependence behavior; and (b) the voltage acceleration for \( \Delta I_{SH} \) remains weak and positive (average of 22 devices).

We can see that the degradation characteristics of \( I_{SH} \) do not show as clear trends as the \( I_D \) component. However, based on the understanding of p-i-p shunt picture, we can postulate the possible mechanism. The most likely cause of enhancement in shunt current is due to decrease in shunt length associated with stress-induced diffusion of Al further into the i-layer (creating a larger p region in the process). Since the SCL current is inversely proportional to length \( (I_{SCL} \sim L^{-2(2+1/3)}) \), a decrease in shunt length will result in a increase in shunt current. There are two possible reasons for this Al incursion during stress. One possibility is that due to current crowding in the shunt region could lead to local temperature rise. This would result in enhanced Al diffusion leading to lower shunt length. Another possibility is that due to the high localized current densities in the shunt region, the Al ions can move due to hopping ionic transport in a-Si:H matrix. The exact mechanism of this Al motion however is not fully established, and further work is needed to identify the physics of this degradation kinetics.

The empirical results on diode and shunt current degradation described above provide a good starting point for exploring the stability of a-Si:H cells. Moreover, these observations when combined with circuit simulations and shading statistics also allow us to estimate the long term effects of this degradation phenomenon.

### V. PROJECTION OF EFFICIENCY DEGRADATION

Over the operating lifetime of a panel, a cell will be subjected to repeated shadow stresses of different magnitudes for random lengths of time. This would result in steady parametric increase in dark current due to increase in both \( I_{SH} \) and \( I_D \) (shown schematically in Fig. 9a). In order to estimate the increase in \( I_D \) during a particular shading event; we need to know the reduction in photocurrent of the shaded cells, the number of shaded cells, and the duration of shading. We can use the shading fraction and number of shaded cells, and use the simulation scheme discussed in Sec. II to obtain the reverse stress voltage VR caused by the shadow. We can then use this stress voltage value and stress duration in the empirical relation of \( \Delta I_D(t, V_R) \) shown in Fig. 5, to estimate the shadow-induced output degradation for each shading event.

We have three random variables in this statistical shadow stress problem, namely reduction in photocurrent \( (X_{shade}) = (1 - \frac{I_{wed}(t) \text{P}}{I_{wed}(t)}) \), number of shaded cells \( (N_{shade}) \), and shading duration \( (t_{shade}) \). For \( X_{shade} \) we can reasonably assume an
exponential distribution, to mimic the fact that worst case shading is least likely. For number of shaded cells $N_{shade}$ and the shading time $t_{shade}$, we assume a uniformly random distribution. For assessing the long term effect of shadow stresses, we generate random samples for the three random variables as defined above, then use the simulation to estimate $V_R$, and finally apply the empirical degradation relations to get the distribution of $\Delta I_D$ values. Finally, the cumulative $\Delta I_D$ is obtained for a particular shading distribution. This calculation process is illustrated in the flowchart in Fig. 9b.

We then use the time and voltage dependencies of over the operating lifetime of the cell these successive stress induced effects will accumulate to reduce the efficiency of the panel. Fig. 9c shows the mean degradation expected from this analysis, for different shading conditions (resulting in different cumulative shading time $t$). For different assumed shading statistics the simulation algorithm provided here can predict the mean degradation over the panel lifetime. While accurate shading statistics need to be obtained for calculating the exact SD value, the method proposed is quite general and will be useful in predicting long term panel performance.

![Figure 9: (a) Schematic representation of repeated shadow stresses during operation resulting in dark degradation. (b) Flowchart showing the simulation method used for estimating the statistical degradation mechanism. Varying $I$, results in different shading conditions, and cumulating shading times ($t$). (c) Projected degradation over operating lifetime of 30 years, vs. cumulative shading time during the lifetime ($t$) in days.](image)

Note that while this first order model of shadow degradation is based on a few reasonable (but untested) assumptions about shadow statistics, the estimates obtained are sufficient for putting a ballpark number for the shadow degradation effect over panel operating lifetime. In this calculation, we have not accounted for the partial relaxation in $I_D$, making the lifetime estimate somewhat conservative. However this is compensated by the fact that we also did not include the increase in $I_{SH}$, which tends to underestimate panel lifetime. On balance this preliminary calculation should give a decent estimate of the total degradation. It must be stressed that the circuit simulation methodology itself is flexible enough to incorporate these features as well, as they are better understood.

VI. Conclusions

We have demonstrated that for a panel operating under typical conditions, parametric shadow degradation is more likely than hot-spot breakdown. Consequently, the parametric degradation of the dark current over the operating lifetime, due to reverse stress, is an important intrinsic reliability consideration at par with other reliability issues of light-induced degradation and contact diffusion. We characterized the SD degradation phenomenon in a-Si:H p-i-n solar cells as a function of voltage and temperature, where the diode current enhancement and relaxation $\Delta I_D(t)$ is described by power-law time dependence, and weak voltage dependence. The increase in shunt current however, is non-systematic but permanent. A circuit simulation methodology to include the statistics of shading was developed. This allows a quantitative prediction of panel performance degradation due to shadow degradation.

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References


