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Interface Trap Density Metrology of state-of-the-art undoped Si n-FinFETs

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The presence of interface states at the MOS interface is a well-known cause of device degradation. This is particularly true for ultra-scaled FinFET geometries where the presence of a few traps can strongly influence device behavior. Typical methods for interface trap density (D_{it}) measurements are not performed on ultimate devices, but on custom designed structures. We present the first set of methods that allow direct estimation of D_{it} in state-of-the-art FinFETs, addressing a critical industry need.

PACS numbers:

I. INTRODUCTION

Non-planar trigated FinFET geometry (Fig. 1a, b) provides a viable solution to the channel length (L_{ch}) scaling due to their better gate to channel electrostatic coupling and reduced Short Channel Effects (SCEs) [1]. In a recent work [2], it has been demonstrated that by using thermionic emission, it is possible to measure (1) the active channel cross-section area (S) (inset Fig. 1), which represents the portion of the physical cross-section of channel where the charge flows, and (2) the source to channel barrier height (E_b), which reflects on the ease with which electrons travel from the source (drain) to the channel, hence opening new ways to investigate FinFETs. Furthermore, it was found that, although the trends of S in the experimental and the simulated data were identical, differences in the absolute values were observed. These differences were found to be caused by the presence of interface states at the metal-oxide-semiconductor interface of the experimental devices [2, 3]. These states can trap electrons and enhance the presence of screening, therefore reducing the action of the gate on the channel, and as a final result, a decrease in the absolute value of S in the experimental data is observed. Here we show that, by using simple mathematical manipulations and the difference between experimental and simulated values of S and of the capacitive coupling $\alpha = \frac{dE_b}{dV_g}$ [2], it is possible to infer the interface trap density (D_{it}). Typical D_{it} measurements are not performed on ultimate devices but on custom designed structures [4]. Such custom structures may only be partially reflective for the possibly surface orientation-dependent and geometry-dependent D_{it}. Here, we provide a simple set of methods for the direct estimation of D_{it} in ultimate devices. The comparison between the values of D_{it} obtained with our two methods and between our results and the results obtained using a method implemented in the past [4] show similar trend.

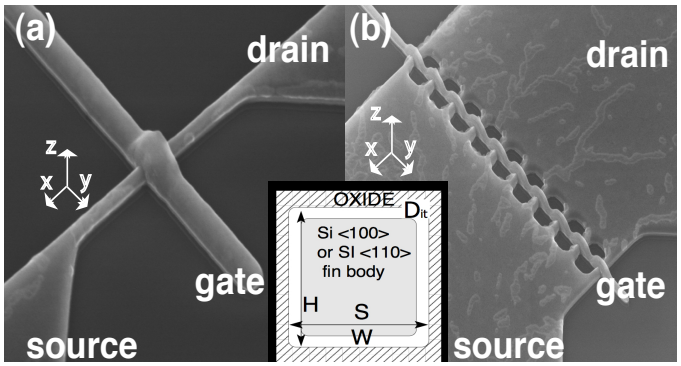


FIG. 1: Scanning-electron-microscope (SEM) image of a state-of-the-art FinFET device with the channel having a <100> orientation and a single fin. b) SEM image of a FinFET device with the channel having a <110> orientation and ten fins. In the inset the schematic of the cross-sectional cut in the Y-Z plane of a typical trigated FinFET is shown. The active cross-section (S) is in grey, H, W, and D_{it} are the physical height, the physical width and the interface trap density, respectively.

FinFET label	W(nm)	H(nm)	L(nm)	Number of channels	Channel orientation	H_2 anneal
A	25	65	40	1	< 100 >	Yes
B	25	65	40	1	< 100 >	No
C	5	65	40	1	< 100 >	No
D and E	18	40	40	10	< 110 >	Yes
F	∼ 3-5	40	40	10	< 110 >	Yes

TABLE I: Details of the n-FinFETs used in this study and the labels used for them. All FinFETs have undoped channel and n-doped source and drain.

A new approach to trap density metrology is of critical importance as CMOS scaling leads device dimensions into nanometer regime. At these scales, quantities such as D_{it} can vary rapidly with device geometry, rendering old techniques inadequate as they cannot be applied directly in these ultra-scaled devices.

II. DEVICE AND EXPERIMENTAL DETAILS

The undoped n-FinFETs used in this work ($A-F$, see table I) consist of nanowire channels etched on a Si intrinsic film with a wrap-around gate covering three faces of the channels (Fig. 1) [5]. An HfSiO layer isolates a TiN layer from the intrinsic Si channel [5]. Devices with the same channel length, (L = 40 nm), different channel height (H = 40 nm and 65 nm), different channel widths (3 nm $\lesssim W \lesssim$ 25 nm), <100> or <110> channel orientation and different surface treatment (A, D, E, F with hydrogen anneal step during fabrication [3] and B, C without) have been studied. Differential conductance ($G = \partial I_{SD}/\partial V_{SD}$) data are taken at $V_{SD} = 0$ V using a lock-in technique. The complete experimental procedure to extract S and E_b can be found in Ref. [2].

III. MODELING APPROACH

To obtain the self-consistent charge and potential in n-FinFETs, the electronic structure is calculated using an atomistic 10 band $sp^3d^5s^*$ semi-empirical Tight-Binding (TB) [6, 7], which captures the geometrical and potential confinement, takes into account the atomic positions in the device [6–8], and is coupled self-consistently to a $2D$ Poisson solver [8, 9]. The thermionic current in the FinFETs is obtained using a ballistic top-of-the-barrier (ToB) model [8, 9]. Due to the extensively large cross-section of the devices that combines up to 44,192 atoms (for H = 65 nm, W = 25 nm FinFETs) in the simula-

tion domain, a new NEMO 3D code has been integrated in the top of the barrier analysis [10]. Using thermionic fitting procedure [2], E_b, α and S can be extracted using the experimental and theoretical conductance (G) in the thermionic emission regime for a 3D system [11] as,

$$G_{3D} = SA^*T\frac{e}{k_B}exp\Big(-\frac{E_b(V_g)}{k_BT}\Big) \tag{1}$$

where A^* is the effective 3D Richardson constant ($A^*_{Si,3D} = 2.1 \times 120\, A \cdot cm^{-2} \cdot K^{-2}$), T is the temperature, k_B is the Boltzmann constant and e is the electronic charge. This will hold only when the cross-section size of the FinFET is large enough (i.e.: W, $H > 20$ nm) to be considered a 3D bulk system. In this study, S is extracted for FinFETs with W(H) $\approx$ 25 nm (65 nm). When the $3D$ approximation is not true anymore (eg. W or H $\lesssim$ 20 nm), only E_b and α can be correctly extrapolated [2].

IV. RESULTS AND DISCUSSION

Two techniques to extract D_{it} in n-Fin-FETs are presented.

A. Method I

The active cross-section in the undoped n-FinFETs is extracted from the temperature based conductance measurement using (1) as outlined in Ref. [2]. Theoretically S is extracted for two n-FinFETs with W/H = 25 nm/65 nm (A and B) and the comparison of the simulated value of S with experimental data is shown in Fig. 2a. The simulations overestimate the value of S due to the electrostatic screening of the channel from the gate due the interface trap charges (σ_{it}) present in these FinFETs [2, 4]. Based on the difference in the simulated S_{sim} and the experimental S_{expt}, values, a method to extract D_{it} in the FinFET devices is outlined (see table II). The method is based on the fact that the total charge in the channel at a given V_g must be the same in the experiments and in the simulations. We therefore assume that the difference between the simulated (ρ_{sim}) and the trap charge density (ρ_{it}) is equal to the experimental charge density (ρ_{expt}) (see appendix). This leads to the following equation:

$$\sigma_{it}(V_g) = \frac{\rho_{sim}(V_g)S_{sim}(V_g)}{e \cdot P}\left[\frac{\Big[1-\frac{S_{expt}(V_g)}{S_{sim}(V_g)}\Big]}{\Big[1-\frac{S_{expt}(V_g)}{W \cdot H}\Big]}\right] \; [\#/cm^2] \tag{2}$$

where P is the perimeter of the channel under the gate ($P = W + 2H$). The extracted D_{it} ($\approx \sigma_{it}$) with V_g (for W/H = 25 nm/65 nm), based on (6), is shown in Fig. 2b. The D_{it} value is almost constant with V_g showing that all the traps are filled (and therefore justifying the assumption $D_{it} \approx \sigma_{it}$). The average value of interface trap density $D_{it,avg}$ is obtained as $5.56 \times 10^{11} cm^{-2}$ for device A and $1.06 \times 10^{12} cm^{-2}$ for device B (Fig. 2b). The values for $D_{it,avg}$ compare quite well with the experimental D_{it} values for two different L_{ch} devices from Ref.[4] (table II). The validity of these results are also supported by the fact that the obtained interface trap density values are different for devices with different surface treatment,

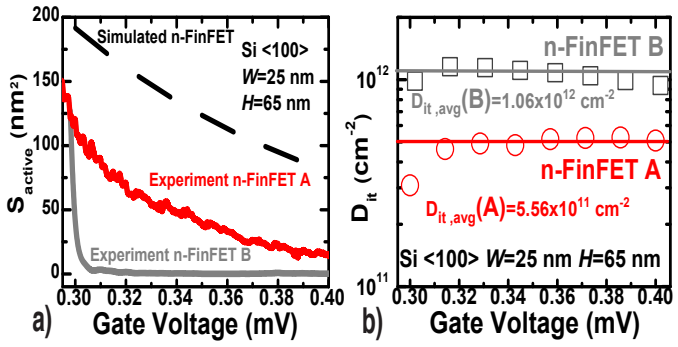


FIG. 2: a) Experimental values of S for an n-FinFET device fabricated (A) using H_2 annealing step [3] and (B) without H_2 annealing. These curves are then compared with the simulated one. All the devices have W= 25 nm, L= 40 nm, H= 65 nm and an identical gate stack, but the use of different deposition systems has led to a shift of 0.15 V in the V_T of (B), which is corrected in the figure for clarity. b) D_{it} extracted for the two devices using Eq. 6. The lines show the average D_{it} value ($D_{it,avg}$). Interface trap density is assumed to be constant for the top and the side walls of the FinFET which may not be always true [4].

as it is well known that the hydrogen anneal step during fabrication greatly improves device characteristics and reduces the interface trap density [3]. As expected, for device B we find much higher $D_{it,av}$ compare to device A.

B. Method II

By assuming that the surface potential (Ψ_s) and the E_b respond equaly to V_g [2, 11], a second extraction approach for D_{it} is developed. Simple calculations (see [11] and the appendix) result in an integrated trap charge density:

$$\sigma_{it} = \frac{C_{ox}}{e} \int \frac{1}{\alpha_{sim}(V_g)} \left[\frac{\alpha_{sim}(V_g)}{\alpha_{expt}(V_g)} - 1 \right] dV_g \; [\#/cm^2] \tag{3}$$

with C_{ox}=0.0173 F/m^2 (C_{ox} is assumed to be the same for all the devices since the oxide thickness is the same in all the devices). This method depends on the valid range of the V_g used for integration in Eq. (3). The limits are set from the V_g point where $\alpha_{sim} \approx 1$ till the threshold voltage (V_T) of the FinFET (Fig. 3), after the flat-band shift (ΔV_{FB}) of the simulated curve. All the extracted $D_{it} \approx \sigma_{it}$ from Method II are shown in table II. In the calculation few assumptions were made; (1) the extra charge contribution is assumed to come completely from the interface trap charges (σ_{it}) and any contribution from the bulk trap states have been neglected, (2) this method of extraction works best for undoped channels since any filling of impurity states is neglected in the calculations.

V. CONCLUSION

A new D_{it} determination methodology for state-of-the-art n-FinFETs is presented. Two complementary approaches provide (a) the gate bias (V_g) dependence of D_{it} (Method I) and, (b) the total D_{it} (Method II); both found consistent with each other. The following trends are observed; (i) devices fabricated without hydrogen annealing step, with smaller W's and with $\langle 110 \rangle$ channel orientation show higher D_{it} compared to the other devices, (ii) by comparison of the value of D_{it} obtained for device B in the two approaches (Fig. 2 and Fig. 3) and the

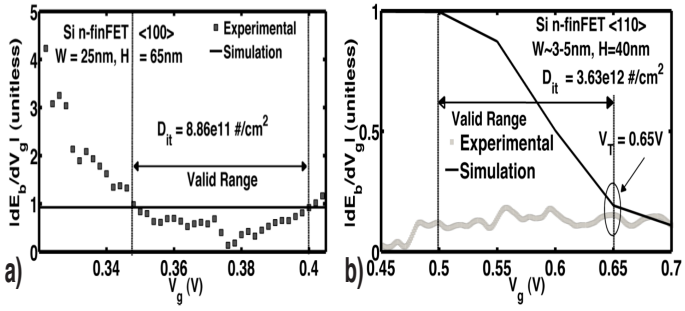


FIG. 3: a) Simulated and experimental $\alpha = dE_b/dV_g$ for FinFET B having $W = 25$ nm, $L = 40$ nm, $H = 65$ nm, <100> channel orientation and no hydrogen annealing step [3]. The observed mismatch is due to the presence of D_{it}, since excessive interface traps can screen the action of gate on E_b. Using Eq. 3 it is then possible to calculate $D_{it} \cong \sigma_{it}$. It is important to notice that the numbers obtained using this method II for device B, compares well with the value obtained for the same device using the method I (as shown in table II). This gives a strong indication of the complementarities between the two approaches that have been introduced in this study. b) Simulated and experimental $\alpha = dE_b/dV_g$ for FinFET (F) having $W \sim$ 3-5 nm, $L = 40$ nm, $H = 40$ nm, and <110> channel orientation. The increase (X2) of D_{it} compared to the devices with larger W (i.e.: D and E), may be attributed to the excessive etching required to make thinner fins.

value of D_{it} obtained for two identical devices (D and E) using the same approach (Method II), compatibility and reproducibility of the methods are demonstrated. The reported trends are similar to the one suggested in the literature [3].

n-FinFET label	Approach	D_{it} (10^{11} cm^{-2})	FinFET type	Remarks
L=140nm [4]	Charge Pumping	1.725	Gated-diode FET [4]	--
L=240nm [4]	Charge Pumping	2.072	Gated-diode FET [4]	--
A	Method I	5.560	Standard FET	H_2 anneal, Low D_{it}
B	Method I	10.6	Standard FET	**No H_2 anneal, higher** D_{it}
B	Method II	8.86	Standard FET	**No H_2 anneal, higher** D_{it}
C	Method II	9.26	Standard FET	Thin fin width, more etching, Higher D_{it}
D (E)	Method II	18.31 (15.3)	Standard FET	<110>, higher bond density, Higher D_{it}
F	Method II	36.3	Standard FET	Same as C+D, Much Higher D_{it}

TABLE II: D_{it} obtained previously ([4]) compared with our results. It is possible to infer three expected trends. a) In good agreement with ref. [3], the hydrogen annealing step substantially reduces D_{it}, b) The scaling of the W of the devices (i.e.: from A to C or from D (E) to F) increases the presence of interface traps and c) The change in the orientation of the channel (and therefore the sidewall surface where the interface traps are formed) from <100> (device A or C) to <110> (device D (E) or F) remarkably increases the presence of traps. Unlike in [4], the presented methods do not require any special device structure, which makes them easily applicable.

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VII. APPENDIX

As outlined in Ref. [2], in undoped n-FinFETs the active channel cross-section area (S) and the source-to-channel barrier height (E_b) can be extracted from the temperature based conductance measurements. Furthermore, in these devices, the differences between the values of the experimental and the simulated S and $|\partial E_b/\partial V_g|$ can be used for the extraction of interface traps density (D_{it}).

In this appendix, the details about the extraction procedure of D_{it} are outlined. The material is organized in the following sections. Interface trap extraction using difference in S is outlined in Sec. VII A along with the assumptions. Section VII B outlines the procedure for D_{it} extraction using the differences between experimental and simulated gate-to-channel coupling values ($\alpha = |\partial E_b/\partial V_g|$) along with the assumptions. Conclusions are given in Sec. VII C.

A. Method I

Based on the difference between the simulated and the experimental active channel cross-section area values (S_{sim} and S_{expt} respectively), a method to extract D_{it} in FinFET devices is outlined.

As the total charge in the channel at a given V_g must be the same in the experiments and in the simulations (charge neutrality), the following equation is obtained:

$$S_{sim} \cdot L_{ch} \cdot \rho_{sim} = S_{expt} \cdot L_{ch} \cdot \rho_{expt} + e \cdot \sigma_{it} \cdot L_{ch} \cdot P \quad (4)$$

where L_{ch} is the channel length, P is the perimeter of the channel under the gate (P $= W + 2H$ as show in Fig. 1 of the main paper), W is the width of the channel, H is the height of the channel, ρ_{sim} (ρ_{expt}) is the simulated (experimental) charge density, e is the electronic charge and σ_{it} the number of trap charges at the interface. Locally it can be assumed that ρ_{expt} can be obtained from ρ_{sim} and σ_{it} using Eq. (5):

$$\rho_{expt} = \rho_{sim} - \rho_{it} = \rho_{sim} - (e \cdot \sigma_{it} \cdot P)/(W \cdot H) \quad (5)$$

Using Eq. (4) and (5) a final expression for σ_{it} is obtained as,

$$\sigma_{it}(V_g) = \frac{\rho_{sim}(V_g) \cdot S_{sim}(V_g)}{e \cdot P} \left[\frac{\left[1 - \frac{S_{expt}(V_g)}{S_{sim}(V_g)}\right]}{\left[1 - \frac{S_{expt}(V_g)}{W \cdot H}\right]} \right] [\#/cm^2] \quad (6)$$

from this, the interface trap density can be extrapolated using the approximation $D_{it} \approx \sigma_{it}$.

1. *Assumptions in Method I*

In the calculation of σ_{it} (D_{it}) few assumptions were made. The extra charge contribution completely comes from the interface trap density (D_{it}) and any contribution from the bulk trap states have been neglected. Also all the interface traps are assumed to be completely filled which justifies the fact that we can assume that $D_{it} \approx \sigma_{it}$. This method of extraction works best for undoped channel since any filling of the impurity/dopant states is neglected in the calculation. Also the interface trap density is assumed to constant for top and side walls of the FinFET which is generally not the case [4].

B. Method II

Based on the difference between simulated and experimental value of α, a second method for the extraction of D_{it} has been demonstrated. Starting from the equivalent capacitance model for a MOSFET with and and without the interface traps, as shown in Figure 4, the basic idea comes from Eq.(38) on page 383 in Ref. [11] which gives,

$$|\frac{\partial E_b}{\partial V_g}| = 1 - \frac{C_{tot}}{C_{ox}}, \quad (7)$$

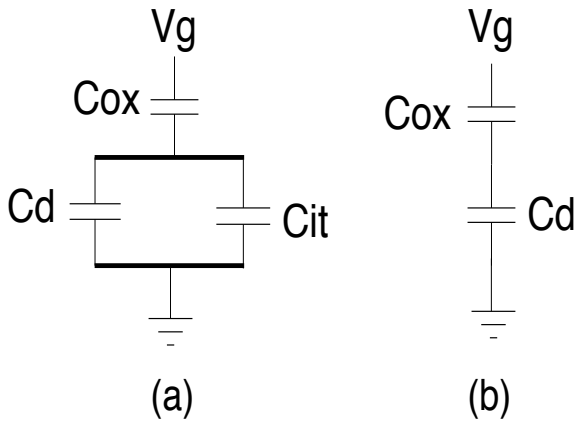


FIG. 4: Equivalent circuits (a) with interface-trap capacitance (C_{it}) and (b) without interface capacitance. C_d and C_{ox} are the depletion and the oxide capacitance, respectively. The idea for this equivalent circuit is obtained from page 381 in Ref. [11].

where C_{tot} and C_{ox} are the total and the oxide capacitance, respectively. For the two cases shown in Fig. 4 the total capacitance is given by,

$$C_{tot}^{exp} = \frac{C_{ox} \cdot (C_d + C_{it})}{C_d + C_{ox} + C_{it}}, \quad (8)$$

$$C_{tot}^{sim} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}, \quad (9)$$

with C_d being the depletion capacitance and C_{it} the interface capacitance. Equation (8) and (9) represent the total capacitances in the experimental and in the simulated device under ideal condition without any interface traps, respectively.

By combining Eq. (7), (8) and (9) and after some mathematical manipulations, we obtain,

$$\frac{1}{\alpha_{exp}} = \frac{1}{\alpha_{sim}} + \frac{C_{it}}{C_{ox}}, \quad (10)$$

where of course $\alpha_{exp/sim} = |\partial E_b^{sim/exp}/\partial V_g|$.

By manipulating Eq.(10) it is possible to obtain Eq. (11):

$$C_{it} = C_{ox} \cdot \Big(\frac{1}{\alpha_{sim}}\Big) \cdot \Big[\frac{\alpha_{sim}}{\alpha_{exp}} - 1\Big], \quad (11)$$

which can be associated with Eq. (12) [11];

$$C_{it} = e \cdot \frac{\partial \sigma_{it}}{\partial V_g}. \quad (12)$$

In Eq. (11) all the values are dependent on V_g except C_{ox}. Integrating Eq. (12) with regard to V_g the final expression for the integrated interface charge density in the FinFETs is,

$$\sigma_{it} = \frac{C_{ox}}{e} \cdot \int_{V_1}^{V_2 = V_T} \Big(\frac{1}{\alpha_{sim}(V_g)}\Big) \cdot \Big[\frac{\alpha_{sim}(V_g)}{\alpha_{exp}(V_g)} - 1\Big] dV_g [\#/cm^2], \quad (13)$$

where V_T is the threshold voltage of the FinFET and V_1 is the V_g at which $\alpha_{exp} = 1$. This is the integration range for Eq. (13) in the sub-threshold region.

1. *Assumptions in Method II*

While deriving the final equation for method II some assumptions were made. The first most important assumption is that the rate of change of the surface potential ($\Psi(V_g)$) is same as E_b with V_g. The extra charge contribution completely comes from the interface trap density (σ_{it}) and any contribution from the bulk trap states have been neglected. Also all the interface traps are assumed to be completely filled which means $\sigma_{it} = D_{it}$. This method works best when the change in DC and AC signal is low enough such that the interface traps can follow the change [11].

C. Conclusion

The detailed calculation for both the trap extraction methods have been provided along with the assumtions made to obtain the final equations. The important point to note here is that, method I provides the variation in interface trap charges with the gate bias however, method II provides the total interface trap charge density within a range of gate bias. The application and the results

obtained from these methods are provided in the main paper.

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