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Interface trap density metrology from sub-threshold transport in highly scaled undoped Si n-FinFETs

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Channel conductance measurements can be used as a tool to study thermally activated electron transport in the sub-threshold region of state-of-the-art FinFETs. Together with theoretical Tight-Binding (TB) calculations, this technique can be used to understand the evolution of source-to-channel barrier height (E_b) and of active channel area (S) with gate bias (V_{gs}). The quantitative difference between experimental and theoretical values that we observe can be attributed to the interface traps present in these FinFETs. Therefore, based on the difference between measured and calculated values of (i) S and (ii) |\partial E_b/\partial V_{gs}| (channel to gate coupling), two new methods of interface trap density (D_{it}) metrology are outlined. These two methods are shown to be very consistent and reliable, thereby opening new ways of analyzing in situ state-of-the-art multi-gate FETs down to the few nm width limit. Furthermore, theoretical investigation of the spatial current density reveal volume inversion in thinner FinFETs near the threshold voltage.

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I. INTRODUCTION

The non-planar tri-gated FinFET geometry (Fig. 1b) provides a viable solution to the channel length ($L_{ch}$) scaling due to its better gate to channel electrostatic coupling and reduced Short Channel Effects (SCEs) [1-3]. In a recent experimental study of undoped Si n-FinFETs [3], thermionic emission in the sub-threshold region was used to measure (1) the active channel cross-section area ($S$) (Fig. 1b), which shows the region of channel where the charge prevalently flows and (2) the source to channel barrier height ($E_b$) (Fig. 1c), which reflects on the ease with which electrons travel from the source/drain to the channel. Understanding the evolution of the active area ‘$S$’ and the barrier height ‘$E_b$’ thus opens up new ways to investigate these FinFETs.

To shed light into the complicated transport phenomena that can arise in these undoped FinFETs we expand our previous work [6,7] and theoretically investigate the evolution of $S$ and $E_b$. Since these devices are small and have finite number of atoms in the channel, modeling transport requires an atomistic representation of the device. A 20 band $sp^3d^5s^*$ atomic Tight-Binding (TB) model with spin orbit coupling (SO) [8-10] is well suited for modeling the bandstructure of these confined Si channels, since TB can easily take into account the material, geometrical, strain and potential fluctuations at the atomic scale [10,11]. This model also takes into account the coupling of the conduction (CB) and the valence bands (VB) which is neglected in simple models like the effective mass approximation (EMA) [12]. Thermally activated transport is modeled using a semi-classical ‘Top of the barrier’ (ToB) model (Fig. 1 c) [10,13]. The simple ToB approach has been shown to model thermionic emission accurately [14].

Qualitatively, we found similar theoretical and experimental trends for $S$ versus gate bias ($V_{gs}$) and $E_b$ versus $V_{gs}$ [6]. However, the theoretically obtained $S$ and $E_b$ values quantitatively over-estimated the experimental values. The reduced experimental values can be attributed to the presence of interface traps in these FinFETs [5,6,15,16]. The effect of interface traps on channel property are even more dominant in the extremely thin FinFETs [7]. This difference in $S$ and $E_b$ has been utilized to directly estimate the interface trap density ($D_{it}$) in these FinFETs, thereby eliminating the need to implement special FinFETs geometries to determine $D_{it}$ [15]. These methods now enable the direct implementation of interface trap density metrology in state-of-the-art undoped Si n-FinFETs.

This paper has been divided into the following sections. Section II provides the details about the FinFETs for which interface trap density metrology has been implemented and the fundamentals of our experimental procedures. The details about the self-consistent calculations are provided in Sec. III A and the theoretical extraction of $E_b$ and $S$ is outlined in Sec. III B. Section IV provides the details of the two procedures for obtaining the interface trap density. The theoretical and experimental results and the discussion on them are given in Sec. V. The conclusions are summarized in Sec. VI.

II. DEVICE AND EXPERIMENTAL DETAILS

Device details: In this work 7 different FinFETs (labeled A-G) with two different channel orientations of [100] ((FinFETs A-C and G)) and [110] ((FinFETs D-F)) have been used [4] (see Table I). All the FinFETs have the same channel length ($L = 40$nm). The channel height ($H$) is either 40nm or 65nm (Table I). The channel width ($W$) varies between 3 to 25nm. All the FinFETs consist of one or more Si nanowire channels etched on a Si intrinsic film with a wrap-around gate covering three faces of the channels (Fig. 1a) [4]. An HISiO (high-$\kappa$) layer isolates a TiN layer from the intrinsic Si channel [4]. These FinFETs have either one channel (FinFETs A-C and G) or ten channels (FinFETs D-F). These devices have two different surface treatments (with or without $H_2$ annealing) as shown in Table I.

Measurement procedure: The experimental value of $E_b$ and $S$ are obtained using a differential conductance ($G = \partial I_D / \partial V_{ds}$) method. The conductance data are taken at $V_{ds} = 0$ V using a lock-in technique. The full experimental method and the required ambient conditions have been outlined in detail in Ref. [4].

In the next section details of the theoretical approach to calculate the experimental values of $E_b$ and $S$ in tri-gated n-FinFETs are outlined.

III. MODELING APPROACH

A. Self-consistent calculation

The bandstructure for the Si channel is calculated using TB [10,11,13]. The TB calculation is coupled self-consistently to a 2D Poisson solver to obtain the charge and the potential [10,13]. Once the convergence between the charge and the potential is achieved the thermionic current in the FinFETs is obtained using a semi-classical ballistic ToB model as shown in Fig. 1. [10,13,17]. Due to the extensively large cross-section of the devices that combines up to 44,192 atoms (for $H = 65$nm, $W = 25$nm FET) in the simulation domain, a new NEMO-3D code has been
TABLE I. Si n-FinFETs used in this study along with their labels. The surface hydrogen annealing detail is also shown. The channel is intrinsic Si, while the source and the drain are n-type doped for all the FinFETs.

<table>
<thead>
<tr>
<th>Label</th>
<th>H</th>
<th>W</th>
<th>L</th>
<th>Channel Orientation</th>
<th>H2 anneal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>65</td>
<td>25</td>
<td>40</td>
<td>[100]</td>
<td>Yes</td>
</tr>
<tr>
<td>B</td>
<td>65</td>
<td>25</td>
<td>40</td>
<td>[100]</td>
<td>No</td>
</tr>
<tr>
<td>C</td>
<td>65</td>
<td>~5</td>
<td>40</td>
<td>[100]</td>
<td>No</td>
</tr>
<tr>
<td>D</td>
<td>40</td>
<td>18</td>
<td>40</td>
<td>[110]</td>
<td>Yes</td>
</tr>
<tr>
<td>E</td>
<td>40</td>
<td>18</td>
<td>40</td>
<td>[110]</td>
<td>Yes</td>
</tr>
<tr>
<td>F</td>
<td>40</td>
<td>~3-5</td>
<td>40</td>
<td>[110]</td>
<td>Yes</td>
</tr>
<tr>
<td>G</td>
<td>65</td>
<td>~7</td>
<td>40</td>
<td>[100]</td>
<td>Yes</td>
</tr>
</tbody>
</table>

integrated in the top of the barrier analysis [18]. Since the FinFETs studied here show (i) negligible source-to-drain tunneling current and (ii) reduced SCEs [6], the ToB model is applicable to such devices [13]. All the FinFETs are n-type doped in the source and drain to a value of $5 \times 10^{19} \text{cm}^{-3}$. A 1.5nm SiO$_2$ cover is assumed.

Next we outline the procedure to calculate $E_b$ and $S$.

B. Calculation of $E_b$ and $S$

For pure thermionic emission any carrier energetic enough to surmount the barrier from the source (Src) to the channel (C) (Fig. 1c) will reach the drain (Drn) provided the transport in the channel is close to ballistic [17]. Typically Src/Drn in FETs are close to thermal and electrical equilibrium (since heavy scattering in the contacts is assumed which leads to instantaneous carrier relaxation). This allows us to make the assumption that most of the carriers in the Src/Drn are thermalized at their respective Fermi-levels ($E_{fs}$, $E_{fd}$ in Fig. 1c). Also the channel potential ($U_{scf}$) can be determined under the application of $V_{gs}$ using the self-consistent scheme (discussed in Sec III A). Hence, for the source-to-channel homo-junction inside a FET, the barrier height ($E_b$) can be determined as a function of $V_{gs}$,

$$E_b(V_{gs}) = U_{scf}(V_{gs}) - E_{fs}.$$ (1)

This definition of $E_b$ implicitly contains the temperature dependence since the simulations are performed at different temperatures ($T$) which enters through the Fermi-Dirac distribution of the Src/Drn. We show in a later section, that the temperature dependence of $E_b$ in the sub-threshold region is very weak. Therefore, all the theoretical $E_b$ results shown in this work are at $T = 300K$.

The study of thermionic emission model is applicable when the barrier height is much larger than the thermal broadening ($E_b \gg k_B T$) [19], where $k_B$ is the Boltzmann constant. For this reason, Eq. (1) works only in the subthreshold region where $E_b$ is well defined [13]. Once the FinFET is above the threshold, $E_b (\leq k_B T)$ is not a well defined quantity [13]. Using the $E_b$ value, $S$ can be extracted using the conductance ($G$) in the thermionic emission regime for a 3D system [6, 19] as,

$$G_{3D} = S A^* T^* e \exp\left(-\frac{E_b(V_{gs})}{k_B T}\right)$$ (2)

where $A^*$ is the effective 3D Richardson constant ($A^*_{Si,3D} = 2.1 \times 120 Acm^{-2}K^{-2}$) [19], and $e$ is the electronic charge. This will hold only when the cross-section size of the FinFET is large enough (i.e.: $W, H > 20nm$) to be considered a 3D bulk system. For a very narrow width FinFET, $S$ cannot be extracted using (2) since the system is close to 1D. For a 1D system the $G$, under a small drain bias ($V_{ds}$) at a temperature $T$, is given by the following relation (for a single energy band [20]),

$$G_{1D} = \frac{2e^2}{h} \cdot \left[1 + e^{\frac{E_b(V_{gs})}{k_BT}}\right]^{-1}$$ (3)

where $h$ is the Planck’s constant. Since Eq.(3) lacks any area description, $G$ for 1D systems is no more a good method to extract $S$. 
IV. TRAP EXTRACTION METHODS

In Ref. [6] it was observed that the active cross-section area ($S_{sim}$) obtained theoretically was an over-estimation of the experimental value ($S_{exp}$). In the results section it will be further shown that also the theoretical $E_b$ value can over estimate the experimental $E_b$ value. These mismatches can be attributed to the presence of traps at the oxide-channel interface of multi-gate FETs where these traps can enhance the Electrostatic screening and suppress the action of the gate on the channel [6, 7, 15, 16]. This simple idea is a powerful tool used for the estimation of interface trap density ($D_{it}$) in these undoped Si n-FinFETs.

A. Method I: $D_{it}$ from active area

Based on the difference between the simulated and the experimental active area ($S$) values, a method to calculate the density of interface trap charges, $\sigma_{it}$, in the FinFETs is outlined. The method is based on the assumption that the total charge in the channel at a given $V_{gs}$ must be the same in the experiments and in the simulations. This requirement leads to the following,

$$S_{sim} \cdot L_{ch} \cdot \rho_{sim} = S_{exp} \cdot L_{ch} \cdot \rho_{exp} + e \cdot \sigma_{it} \cdot L_{ch} \cdot P$$

(4)

where $S_{sim}$ ($S_{exp}$) is the simulated (experimental) active area, $P$ is the perimeter of the channel under the gate ($P = W + 2H$) and $\rho_{sim}$ ($\rho_{exp}$) is the simulated (experimental) charge density. By applying Gauss’s law at the oxide channel interface, $\rho_{exp}$ is obtained from $\rho_{sim}$ and $\sigma_{it}$ as,

$$\rho_{exp} = \rho_{sim} - \rho_{it} = \rho_{sim} - (e \cdot \sigma_{it} \cdot P) / (W \cdot H)$$

(5)

Using (4) and (5) the final expression for $\sigma_{it}$ is obtained as,

$$\sigma_{it}(V_{gs}) = \frac{\rho_{sim}(V_{gs}) S_{sim}(V_{gs})}{e \cdot P} \times \left[ 1 - \frac{S_{exp}(V_{gs})}{S_{sim}(V_{gs})} \right] \left[ 1 - \frac{S_{exp}(V_{gs})}{W \cdot H} \right] \left[ \text{#/cm}^2 \right]$$

(6)

This method is useful for wider devices for which Eq.(2) is valid. For very thin FinFETs (close to a 1D system) this method cannot be utilized.

Assumptions in Method I: The extra charge contribution completely stems from the interface trap density ($D_{it}$) and any contribution from the bulk trap states has been neglected. All the interface traps are assumed to be completely filled which implies $\sigma_{it} \equiv D_{it}$. The interface trap charges are assumed to be situated very close to the oxide-channel interface for Eq.5 to be true. Also the interface trap density is assumed to be constant and identical for the top and the side walls of the FinFET which is generally not the case [15, 16]. This method of extraction works best for undoped channel since any filling of the impurity/dopant states is neglected in the calculation. Orientation dependent $D_{it}$ for different surfaces could be included as a further refinement.

B. Method II: $D_{it}$ from barrier control

The second method does not utilize the $E_b$ value directly but its derivative w.r.t $V_{gs}$. The term $\alpha = |\partial E_b / \partial V_{gs}|$ represents the channel to gate coupling [6]. The presence of interface traps weakens this coupling due to the electrostatic screening. This method of trap extraction is based on the difference in the experimental and the simulated $\alpha$ value. The $\alpha$ value can be represented in terms of the channel and the oxide capacitance. The equivalent capacitance model for a MOSFET with and without interface traps ($D_{it}$) is shown in Fig.2.

The $\alpha$ value can be associated to the oxide, interface and semiconductor capacitance which is given in Eq.(38) on page 383 in Ref. [19]. This leads to the following relation,

$$\frac{\partial E_b}{\partial V_{gs}} = 1 - \frac{C_{tot}}{C_{ox}}$$

(7)
where $C_{\text{tot}}$ is the total capacitance. For the two cases, as shown in Fig. 2, the total capacitance is given by,

$$C_{\text{tot}}^\text{exp} = \frac{C_{\text{ox}} \cdot (C_d + C_{\text{it}})}{C_d + C_{\text{ox}} + C_{\text{it}}},$$

(8)

$$C_{\text{tot}}^\text{sim} = \frac{C_d \cdot C_{\text{ox}}}{C_d + C_{\text{ox}}},$$

(9)

where $C_{\text{it}}, C_{\text{ox}}$ and $C_d$ are the interface trap capacitance, the oxide capacitance and the semi-conductor capacitance, respectively. Eq. (8) represents the capacitance in the experimental device and Eq. (9) represents the capacitance in the simulated device under ideal conditions without any interface traps. Combining Eq. (7), (8) and (9) and after some mathematical manipulations, we obtain,

$$\frac{1}{\alpha_{\text{exp}}} = \frac{1}{\alpha_{\text{sim}}} + \frac{C_{\text{it}}}{C_{\text{ox}}},$$

(10)

Manipulating Eq. (10) gives the following relation for $C_{\text{it}}$,

$$C_{\text{it}} = C_{\text{ox}} \cdot \left( \frac{1}{\alpha_{\text{sim}}} \cdot \frac{\alpha_{\text{sim}}}{\alpha_{\text{exp}}} - 1 \right)$$

(11)

Also $C_{\text{it}}$ can be related to the interface charge density ($\sigma_{\text{it}}$) as [19],

$$C_{\text{it}} = e \cdot \frac{\partial \sigma_{\text{it}}}{\partial V_{\text{gs}}}$$

(12)

In Eq. (11) all the values are dependent on $V_{\text{gs}}$ except $C_{\text{ox}}$. Combining Eq. (11) and (12) and integrating w.r.t $V_{\text{gs}}$ yields the final expression for the integrated interface charge density in these FinFETs as,

$$\sigma_{\text{it}} = \frac{C_{\text{ox}}}{e} \cdot \int_{V_1}^{V_2=V_T} \left( \frac{1}{\alpha_{\text{sim}}(V_{\text{gs}})} \right)$$

$$\times \left[ \frac{\alpha_{\text{sim}}(V_{\text{gs}})}{\alpha_{\text{exp}}(V_{\text{gs}})} - 1 \right] dV_{\text{gs}} \ [\#/\text{cm}^2],$$

(13)

where $V_T$ is the threshold voltage of the FinFET and $V_1$ is the $V_{\text{gs}}$ at which $\alpha_{\text{exp/sim}} \approx 1$. Thus $V_1$ and $V_2$ is the integration range for Eq. (13) in the sub-threshold region.

The second method derived from barrier control has the advantage that it is independent of the dimensionality of the FinFET. Hence, Eq. (13) can be used for wide as well as thin FinFETs.

Assumptions in Method II: The most important assumption is that the rate of change of the surface potential ($\Psi(V_{\text{gs}})$) is the same as $E_b$ w.r.t $V_{\text{gs}}$. The extra charge contribution completely originates from the density of interface trap charges ($\sigma_{\text{it}}$) and any contribution from the bulk trap states have been neglected. Also all the interface traps are assumed to be completely filled which implies $\sigma_{\text{it}} = D_{\text{it}}$. This method works best when the change in the DC and the AC signal is low enough, such that the interface traps can follow the change in the bias sweep [19].

C. Limitations of the methods

It is important to understand the limitations of the new trap metrology methods to apply them properly. One of the main limitation is how closely the simulated FinFET structure resembles the experimental device structure. This depends both on the SEM/TEM imaging as well the sophistication of the model. In the present case we create the FinFET cross-section structure using the TEM image making the simulated structure as close to the experimental device as possible. With the development of better TCAD tools, the proximity of the simulated structure to experimental structure has increased. The physical device model needs to comprehend the crystal directions, atomistic details, strain and gating realistically to realize the working of the nano-scale FETs. Effective mass models fail to properly represent the bandstructure in these type of ultra-scaled nanowires/FinFETs [12]. Our model enables the calculation of theoretical conductance value with good confidence to be used in the trap calculation. Furthermore, the calculated G is calculated as close to ideal as possible and all the difference between the ideal and experimental G is attributed to the traps which may not be true always. An important difference between the two methods is that they are calculated over different $V_{\text{gs}}$ ranges. This is important since the trap filling and their behavior changes with $V_{\text{gs}}$ range which should be taken into account accurately. One must also be aware of the embedded assumption of complete interface trap filling and the neglect of the bulk traps in the gate dielectric.
V. RESULTS AND DISCUSSION

In this section the theoretical results as well as their comparison with the experimental data are provided.

A. 3D vs. 1D system

The conduction band structure (E-K) can be utilized to distinguish a 1D system from a 3D system. The bulk silicon conduction band (CB) has 6 degenerate valleys ($\Delta_e$) (see inset of Fig. 3 and Fig. 2) which split into 2 sets of degenerate valleys called the ‘$4 - 2$ configuration’ ($\Delta_4 - \Delta_2$) for [100] and [110] 1D nanowires (NWs) due to the geometrical confinement [10]. In Si bulk the $\Delta_2$ valleys are along the [100] direction. For a [100] Si nanowire channel the bulk $\Delta_2$ valleys are projected along the channel axis away from the $\Gamma$ point due to the folding of the Brillouin Zone (Fig. 3a and b) [10]. The bulk $\Delta_4$ valleys are projected at the $\Gamma$ point [10]. The bandstructure of conduction band for silicon channel with $W = 3 \text{nm}$ and $H = 15 \text{nm}$ is shown in Fig. 3a and b, respectively. For [110] oriented Si channel the valley projection is different compared to the [100] channel. The CB minima is at the Off-$\Gamma$ position as shown in Fig. 3. This happens due to the different atomic positions and geometrical confinement in [100] and [110] channels [10].

The energy separation between the $\Gamma$ and Off-$\Gamma$ valleys is given by,

$$\Delta E_c = E(\Gamma) - E(\text{Off} - \Gamma),$$

which gives a measure of how close (or far) a 1D NW system is from a 3D bulk system. The observation of a large $\Delta E_c$ value strongly points towards a 1D system, whereas a value close to zero points to a bulk system. Tight-binding simulations predict a $\Delta E_c$ value of around 120 meV for a [100] Si nanowire channel with $W = 3 \text{nm}$ and $H = 15 \text{nm}$ (Fig. 3a) while this value reduces to 6 meV for a Si nanowires channel with $W = H = 15 \text{nm}$ (Fig. 3b). For a [110] Si channel the $\Delta E_c$ value is around 34 meV for $W = 3 \text{nm}$ and $H = 15 \text{nm}$ (Fig. 3a) which reduces to 3.4 meV for $W = 15 \text{nm}$ and $H = 15 \text{nm}$ (Fig. 3b). This indicates that larger cross-section silicon channels are closer to the 3D bulk system for both [100] and [110] oriented channels.

The conduction band minimum (CBM) decreases with increasing channel width for both [100] and [110] SiNWs (Fig. Fig. 4a). Also the $\Delta E_c$ value decreases with silicon channel width for a fixed height of 15nm ((Fig. 4b). The $\Delta E_c$ value is negative for [110] channel since the $\Gamma$ valley is lower in energy compared to the $\Gamma$ valley. For $W > 15 \text{nm}$ the $\Delta E_c$ is less than 5 meV ($\leq k_b T_{300K}$) for both [100] and [110] Si channels. This suggests that silicon channels with $W \geq 15 \text{nm}$ and $H = 15 \text{nm}$ behave electrically close to the bulk Si system at room temperature.

B. Temperature dependence of $E_b$

The source-to-channel barrier height has been assumed to be temperature independent in the sub-threshold region. Figure 6 shows the results of a temperature dependent ToB calculations and proves that the barrier height ($E_b$) is only weakly temperature dependent. In the subthreshold region, the $E_b$ value for a device identical to FinFET C, is same at four different temperatures (T=140K, 200K, 240K and 300K). The variation with temperature becomes more prominent when the FinFET transitions into the on-state. Thus, $E_b$ has a weak temperature dependence in the sub-threshold region allowing us to evaluate $E_b$ from the 300K simulations only.

C. Evolution of $E_b$ and S with $V_{gs}$

Experimentally, it has been shown that, for undoped silicon n-FinFETs [6], $E_b$ reduces as $V_{gs}$ increases. Theoretically, the $E_b$ value is determined using Eq. (1) which depends on the self-consistent channel potential ($U_{scf}$). As the gate bias increases, the channel can support more charge. This is obtained by pushing the channel CB lower in energy to be populated more by the source and drain Fermi level [10]. Figure 7 and 8 show the experimental and theoretical evolution of $E_b$ in FinFETs G, C and D, E, respectively. Theory provides correct qualitative trend for $E_b$ with $V_{gs}$. Few important observations here are, (i) the theoretical $E_b$ value is always higher than the experimental value and (ii) [110] Si devices (D and E) show a larger mismatch to the experimental values. The reason for the first point is suggested to be the presence of interface traps in the FinFETs which screen the gate from the channel [6, 7]. The second observation can be understood by the fact that [110] channels with (110) sidewalls have higher interface trap density due to the higher surface bond density [19] and poor anisotropic etching of the (110) sidewalls [15, 16].
The active channel area ($S$) represents the part of the channel where the charge flows [6]. Experimentally $S$ is shown to be decreasing with gate bias since the inversion charge moves closer to the interface which electrostatically screens the inner part of the channel from the gate [6]. This gives a good indication of how much channel area is used for the charge transport. Figure 9a and b show the experimental evolution of $S$ in FinFET B and E, respectively. However, the absolute values do not match. In fact theory over-estimates the experimental $S$ value (Fig. 9) which is attributed to the interface traps.

D. Trap density evaluation

In this section we present the results on the interface trap density ($D_{it}$) in the undoped Si n-FinFETs.

1. $D_{it}$ using $S$: Method I

The calculated $D_{it}$ values for FinFET B and E are 1.02e12 cm$^{-2}$ and 1.81e12 cm$^{-2}$ (Fig 10a and b, respectively). The $D_{it}$ values compare quite well with the experimental $D_{it}$ values presented in Ref. [15] and also shown in Table II. As expected the $D_{it}$ value for FinFET E (with [110] channel and (110) sidewalls) is higher than FinFET B ([100] channel with (100) sidewalls). This is attributed to the higher $D_{it}$ ($\sim 2\times$) on the (110) surfaces [15, 16]. Our results show $\sim 1.8\times$ more $D_{it}$ for (110) sidewalls, in close agreement to the experiments. This method allows to obtain the $D_{it}$ in the actual FinFETs rather than custom made FETs.

2. $D_{it}$ using $|\partial E_b/\partial V_{gs}|$: Method II

The $C_{ox}$ value needed in this method is taken as $\sim 0.0173 F/m^2$ which is assumed to be the same for all the devices since these FinFETs have similar oxide thickness. The calculated $D_{it}$ values for FinFET C and D are 9.26e11 cm$^{-2}$ and 1.563e12 cm$^{-2}$ (Fig.11a and b, respectively). These calculations also show that the [110] channel device (FinFET E) shows a higher $D_{it}$ compared to the [100] channel device (FinFET C), again consistent to the observations made in Ref. [15]. The advantage of this method is that it can be used to obtain $D_{it}$ in extremely thin FinFETs (close to 1D system) unlike method I which is applicable only to wider FinFETs (due to the reasons discussed in Sec. III B).

3. Discussion on the two methods and $D_{it}$ trends

The $D_{it}$ values for all the FinFETs used in this study are shown in Table II. The important outcomes about the two methods are outlined below:

- The $D_{it}$ values obtained by the two methods compare very well with the experimental measurement in Ref. [15] for similar sized FinFETs (A and B), demonstrating the validity of these new methods.
- The $D_{it}$ values calculated using method I and II (for B and E) compare very well with each other which shows that the two methods are complimentary [7] for large cross-section devices.
- The $D_{it}$ values calculated for the two similar FinFETs (D and E) compare very well showing the reproducibility of the methods [7].

The calculated $D_{it}$ values also reflect some important trends about the FinFET width scaling and surfaces (Table II). The central points are:

- Hydrogen passivation considerably reduces $D_{it}$ [5]. This is observed for FinFETs A and B where $H_2$ passivation results in $\sim 2\times$ less $D_{it}$ in FinFET A [7].
- Width scaling requires more etching which also increases $D_{it}$ [15, 16]. The same trend is observed in devices A to C and D to F (decreasing W).
- (110) sidewalls show higher $D_{it}$ compared to (100) sidewalls [15]. The same trend is also observed for FinFETs A, B, C, G ((100) sidewall) compared to FinFETs D, E and F ((110) sidewall).
### E. Current distribution

The spatial current distribution in FinFETs can provide a better insight for optimizing the channel cross-section area utilization. Theoretical calculations show that the charge flow in n-FinFETs depends strongly on the geometrical confinement. For very small width FinFET (W \sim 5) the entire body gets inverted (Fig.12 (a)) and shows little change in $S$ with $V_{gs}$ [6]. For wider FinFETs (W \sim 25) the current flow starts from a weak volume inversion and moves towards surface inversion as $V_{gs}$ increases (Fig.12 (b)) [6]. For extremely thin n-FinFETs ($W = 5$nm, $H = 65$nm) the charge flows through the entire body (volume inversion) compared to the wider n-FinFETs ($W = 25$nm, $H = 65$nm) where the charge flows at the edges. Thus thin FinFETs can show better channel area utilization for the charge flow compared to the wider devices. However thin FinFETs show an increase in $D_{it}$ due to more side-wall etching (Table II) which can severely limit the action of the thin FinFETs. The advancement of fabrication methods and strain technology may improve the performance of thin FinFETs as reported by some experimental works [21][23].

### VI. CONCLUSIONS

Two new trap charge density metrology methods in ultra-scaled Si n-FinFETs are presented. The Top-of-the-barrier model, combined with Tight-binding calculations, explains very well the thermally activated sub-threshold transport in state-of-the-art Si FinFETs. The qualitative evolution of $E_b$ and $S$ with $V_{gs}$ are well explained by the theory. The systematic mismatch in the experimental and theoretical values of $E_b$ and $S$ led to the development of two new interface trap density metrology schemes. The advantage of these schemes is that they do not require any special MOSFET structure as needed by the present experimental methods allowing to probe the interface quality of the ultimate channel. These methods are shown to provide consistent and reproducible results which compare very well with the independent experimental trap measurement results. The calculated trends of interface trap density with channel width scaling, channel orientation and hydrogen passivation of the surfaces show a good correlation with the experimental observations. Thin width FinFETs could lead to a better channel utilization due to strong volume inversion only if surface roughness and the density of interface traps created during the extreme etching of these ultra-scaled devices can be reduced.

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FIG. 1. (a) Scanning-electron-microscope (SEM) image of a Si n-FinFET with [100] channel orientation and single fin. (b) The schematic of the cross-sectional cut in the Y-Z plane of a typical tri-gated FinFET. The active cross-section (S) is in gray, \( H \) and \( W \) are the physical height and width, respectively. (c) Ballistic top of the barrier model employed for calculating the thermionic current in the FinFETs.

FIG. 2. Equivalent circuits (a) with interface-trap capacitance \( (C_{it}) \) and (b) without interface capacitance. \( C_d \) and \( C_{ox} \) are the depletion and the oxide capacitance, respectively. The idea for this equivalent circuit is obtained from page 381 in Ref. [19].

FIG. 3. Simulated conduction band E-K, using TB, for [100] Si channel with $H = 15$nm for (a) $W = 3$nm and (b) $W = 15$nm. The inset shows 6 equivalent bulk Si conduction band ellipsoids. The $\Delta_2$ valleys (brown cigars) are along the transport direction [100] whereas the $\Delta_4$ valleys (blue cigars) are in the quantized plane.

FIG. 4. Simulated conduction band E-K, using TB, for [110] Si channel with $H = 15$nm for (a) $W = 3$nm and (b) $W = 15$nm. The CB minima is at Off-$\Gamma$ position for the thinner [110] Si channel. Inset shows the bulk Si 6 equivalent conduction valleys.

FIG. 5. (a) Variation of the conduction band minimum ($E_c$) for [100] and [110] oriented Si channels with width for a fixed height of 15nm. (b) The separation of the $\Delta_2$-$\Delta_4$ valleys with width (W) for rectangular [100] and [110] Si channel for a fixed height of 15nm.

FIG. 6. Temperature dependence of the simulated barrier height ($E_b$) in n-FinFET C. At $T=300K$, $V_T$ of the FinFET is 0.62V. The overlap of the curves at different temperatures with $V_{gs}$ below $V_T$ at 300K, shows a weak temperature dependence of $E_b$ in the sub-threshold region. The impact of temperature becomes prominent after $V_{gs}$ goes above $V_T$.

FIG. 7. Experimental and simulated barrier height ($E_b$) in n-FinFET (a) G and (b) C. Both the devices have same $V_T$. Both experiment and simulation show a decreasing value of $E_b$ with $V_{gs}$, but the absolute values are different.

FIG. 8. Experimental and simulated barrier height ($E_b$) in n-FinFETs (a) D and (b) E. Both the devices have similar $V_T$. Both experiment and simulation show a decreasing value of $E_b$ with $V_{gs}$, but the absolute values are different.

FIG. 9. Experimental and simulated channel active cross-section (S) in n-FinFETs (a) B and (b) E. Both experiment and simulation show a decreasing value of S with V_{gs}, but the absolute values are different.

FIG. 10. Extracted trap density using the difference in active device area (method I) for n-FinFETs (a) B and (b) E.

FIG. 11. Experimental and simulated value of α in n-FinFETs (a) C and (b) E.

FIG. 12. Spatial current distribution in the (100) undoped Si n-FinFET intrinsic with $H = 65\text{nm}$ and (a) $W = 5\text{nm}$ and (b) $W = 25\text{nm}$. $V_{gs} = 0.4\text{V}$ and $V_{DS} = 30\text{mV}$ at 300K. 5nm device shows a complete volume inversion. In the 25nm device the current mainly flows at the edges.