Purdue University
Purdue e-Pubs

Birck and NCN Publications | Birck Nanotechnology Center

11-1-2010

On the Nature of Shunt Leakage in Amorphous Silicon p-i-n Solar Cells

Sourabh Dongaonkar
Purdue University - Main Campus, sourabh@purdue.edu

Karthik Y
Indian Institute of Technology - Bombay, karthiky@ee.iitb.ac.in

Dapeng Wang
Dapeng_Wang@amat.com

Michel Frei
Michel_Frei@amat.com

Souvik Mahapatra
Indian Institute of Technology - Bombay, souvik@ee.iitb.ac.in

See next page for additional authors

Follow this and additional works at: http://docs.lib.purdue.edu/nanopub

Part of the Electronic Devices and Semiconductor Manufacturing Commons, and the Nanotechnology fabrication Commons

Dongaonkar, Sourabh; Y, Karthik; Wang, Dapeng; Frei, Michel; Mahapatra, Souvik; and Alam, Muhammad A., "On the Nature of Shunt Leakage in Amorphous Silicon p-i-n Solar Cells" (2010). *Birck and NCN Publications.* Paper 709.
http://docs.lib.purdue.edu/nanopub/709

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Authors
Sourabh Dongaonkar, Karthik Y, Dapeng Wang, Michel Frei, Souvik Mahapatra, and Muhammad A. Alam

This article is available at Purdue e-Pubs: http://docs.lib.purdue.edu/nanopub/709

On the Nature of Shunt Leakage in Amorphous Silicon p-i-n Solar Cells

Sourabh Dongaonkar, Karthik Y, Dapeng Wang, Michel Frei, Souvik Mahapatra, *Senior Member, IEEE*, and Muhammad A. Alam, *Fellow, IEEE*

***Abstract*—In this letter, we investigate the nature of shunt leakage currents in large-area (on the order of square centimeters) thin-film a-Si:H p-i-n solar cells and show that it is characterized by following universal features: 1) voltage symmetry; 2) power-law voltage dependence; and 3) weak temperature dependence. The voltage symmetry offers a robust empirical method to isolate the *diode* current from measured "shunt-contaminated" forward dark IV. We find that space-charge-limited current provides the best qualitative explanation for the observed features of the shunt current. Finally, we discuss the possible physical origin of localized shunt paths in the light of experimental observations from literature.**

***Index Terms*—Amorphous silicon solar, dark current, shunt leakage, space-charge-limited (SCL) current.**

I. Introduction

LARGE-AREA thin-film amorphous silicon p-i-n solar cells are often considered as promising alternatives to crystalline silicon solar cells because of the reduced manufacturing and installation costs [1]. The measured dark current (I_{meas}) in large-area cells, however, is known to exhibit a high leakage current at low forward biases. This phenomenon is known in literature as *shunt* leakage current (I_{shunt}). It is often represented by a variable ohmic current in parallel to the diode current (I_{diode}) of a p-i-n cell. While the diode current part (I_{diode}) has been studied extensively [2], [3], I_{shunt} remains poorly understood. Study of I_{shunt} is important because excessive shunt current can adversely affect the efficiency of a cell and compromise module output. In this letter, we report a detailed and systematic study of I_{shunt} and establish its key phenomenological features. We utilize this characterization to provide a simple method for isolating I_{diode} from measured dark IV (I_{meas}) by subtracting out the shunt current $(I_{\mathrm{diode}} = I_{\mathrm{meas}} - I_{\mathrm{shunt}})$. This "cleaned" I_{diode} can then be used to accurately characterize the device performance for optimizing process conditions. We find that the defining features of I_{shunt} are generally consistent with space-charge-limited (SCL) transport. We also correlate this analysis with reported experimental observations to suggest the nature of the shunt paths.

Manuscript received July 8, 2010; revised July 19, 2010; accepted July 22, 2010. Date of publication September 7, 2010; date of current version October 22, 2010. This work was supported in part by the Solar Business Group, Applied Materials. The simulation work was supported as part of the Center for Re-Defining Photovoltaic Efficiency Through Molecule Scale Control, an Energy Frontier Research Center funded by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Award DE-SC0001085. The review of this letter was arranged by Editor P. K. -L. Yu.

S. Dongaonkar and M. A. Alam are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: sourabh@purdue.edu; alam@purdue.edu).

K. Y and S. Mahapatra are with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India.

D. Wang and M. Frei are with the Solar Business Group, Applied Materials, Santa Clara, CA 95054-3299 USA.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2064754

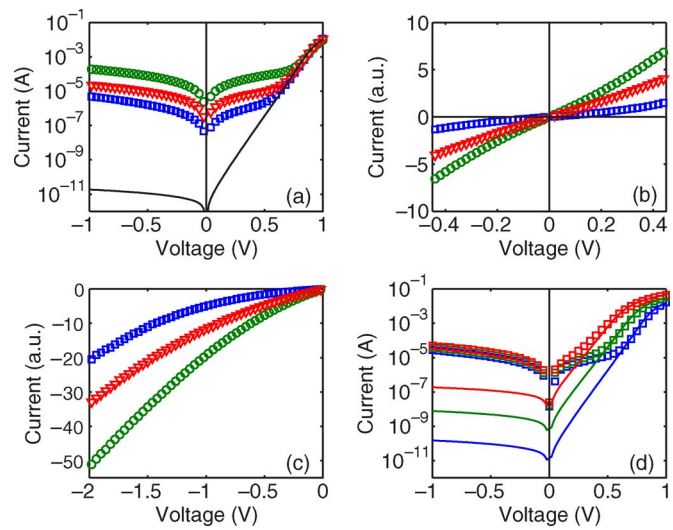

Fig. 1. (a) Dark IV characteristics of three nominally identical cells (symbols), compared to simulated IV (solid line). The (b) symmetry and (c) nonlinearity of the leakage current for the same three devices (current values are scaled for clarity). (d) Temperature-dependent dark IV of one of the devices (symbols), at 45 °C, 85 °C, and 120 °C, compared to simulations (solid lines).

II. Measurements and Observations

The devices measured were single-junction a-Si:H p-i-n solar cells, manufactured by PECVD process on a commercial TCO-coated glass. The layer structure is SnO_2:F/p(10 nm)-i(250 nm) -n(20 nm) a-Si:H/ZnO:Al, and the cell area is 0.5 cm^2. The room temperature dark IV (voltage range from -4 to 1 V) was measured for 60 cells. The temperature-dependent IV measurements at 45 °C, 85 °C, and 120 °C were obtained for 23 cells. The measurements were made using a standard Agilent 4155C parametric analyzer. Self-consistent 1-D simulation (electron-hole transport along with Poisson equation and tunneling) of the p-i-n structure was carried out using Synopsys Medici TCAD software. In this simulation, we used typical a-Si:H material parameters, including the band tails and deep defect distributions, as described in the literature [4], [5].

Fig. 1(a) shows the room temperature dark IV (I_{meas}) of three nominally identical devices (symbols), compared to the

0741-3106/$26.00 © 2010 IEEE

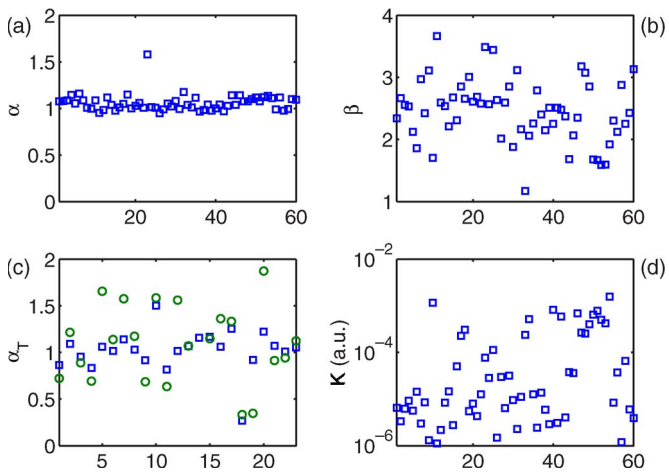

Fig. 2. Scatter plots showing the statistical robustness of shunt current features (symbols). Here, the x-axis shows the number of devices measured. (a) Symmetry ratio $\alpha = |I_{\rm meas}(0.3\ {\rm V})/I_{\rm meas}(-0.3\ {\rm V})|$ for 60 devices, (b) extracted voltage exponent β for 60 devices, (c) temperature acceleration ratio α_T given as $I_{\rm shunt}(85\ ^\circ{\rm C})/I_{\rm shunt}(45\ ^\circ{\rm C})$ (squares) and $I_{\rm shunt}(120\ ^\circ{\rm C})/I_{\rm shunt}(45\ ^\circ{\rm C})$ (circles) for 23 devices, and (d) the factor K from the fit $I_{\rm shunt} = K|V|^\beta$ of the shunt current for 60 devices.

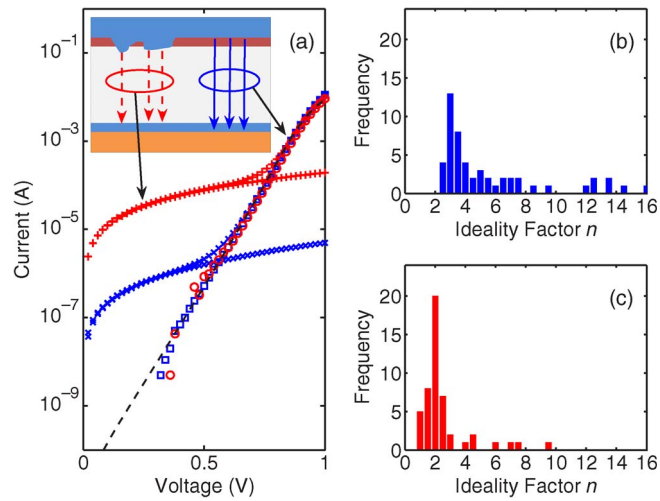

Fig. 3. (a) Plot showing that the cleaned IV (circles and squares), obtained by subtracting off the symmetric shunt in two devices (crosses and plusses), shows the expected exponential behavior. Histograms compare the spread of extracted ideality factor n (using $n = q(V_2 - V_1)/k_BT\ln(I_2/I_1)$, with $V_2 = 0.7$ and $V_1 = 0.4$) (b) before and (c) after removing the shunt component.

simulated bulk IV characteristics $I_{\rm diode}$ (solid line). First, we note that, while $I_{\rm meas}$ in high forward bias region ($V >\sim 0.5$) is the same for all devices, the current at low forward bias and reverse biases ($-4 < V <\sim 0.5$) varies by more than two orders of magnitude, from device to device. Moreover, for $V >\sim 0.5$, the measurement agrees very well with our detailed numerical simulations ($I_{\rm meas} \approx I_{\rm diode}$ in this range). On the other hand, at low forward bias and reverse bias, the measured current is four to five orders of magnitude higher than the simulated value ($I_{\rm shunt} = I_{\rm meas} - I_{\rm diode} \approx I_{\rm meas}$ for $V <\sim 0.5$). A closer look at this leakage current at low biases (on a linear scale and appropriately scaled for clarity) shows that it is remarkably symmetric around $V = 0$ [see Fig. 1(b)]. Such symmetry is unexpected in a rectifying p-i-n diode structure. In addition, as shown in Fig. 1(c), this leakage current shows nonlinear (power-law) voltage dependence ($I_{\rm shunt} \propto |V|^\beta$), with the exponent $\beta \sim 2 - 3$. Finally, consider the temperature-dependent dark IV of one of the cells [Fig. 1(d)]. We find that, in high forward bias, the temperature dependence is exponential (squares), as expected from simulations (solid lines). In contrast, the shunt leakage at low biases and reverse bias is remarkably insensitive to temperature, as opposed to the simulated $I_{\rm diode}$ (solid lines).

We now show that these features of $I_{\rm shunt}$ discussed earlier are not anomalous but reproducible and statistically robust in large-area cells. First, we demonstrate the voltage symmetry quantitatively by plotting the ratio $\alpha = |I_{\rm meas}(0.3\ {\rm V})/I_{\rm meas}(-0.3\ {\rm V})|$ at room temperature for all 60 devices [Fig. 2(a)]. Notice that 90% of them are within one standard deviation (SD) of 1, compared to typical diode current ($I_{\rm diode}$) where $\alpha \sim 300$. Second, we demonstrate the nonlinearity by fitting the current in the range $-4 < V < 0.5$ using a power law ($I_{\rm shunt} = K|V|^\beta$). We find that the power exponent $\beta \sim 2 - 3$ (within one SD) for 70% of the devices [Fig. 2(b)]. Third, we verify the weak temperature dependence of the leakage current by plotting the temperature sensitivity ratio $-\alpha_T = I_{\rm shunt}(T_2)/I_{\rm shunt}(T_1)$ for 23 devices [Fig. 2(c)]. Remarkably, over the 75 °C variation, $\alpha_T \approx 1 \pm 0.4$. This is in contrast to the activated diode current ($I_{\rm diode}$), where α_T would be ~400 over the same temperature range [see Fig. 1(d)]. Finally, we observe that the magnitude of this leakage component, which is proportional to the parameter K, obtained from the $|I_{\rm shunt}| = K|V|^\beta$ fit, varies over three orders of magnitude for these 60 devices [Fig. 2(d)]. Such statistical fluctuation establishes $I_{\rm shunt}$ as a parasitic current, separate from nominally identical diode current $I_{\rm diode}$.

III. Parameter Extraction

We now demonstrate how this characterization of $I_{\rm shunt}$ can be used to isolate the actual p-i-n diode current ($I_{\rm diode}$) by subtracting out the shunt current ($I_{\rm diode} = I_{\rm meas} - I_{\rm shunt}$). Fig. 3(a) shows the plot of $|I|$ versus $|V|$ for two devices (crosses and pluses). Now, using the symmetry, we can subtract the magnitude of reverse current $|I_{{\rm meas},r}|$ from the measured forward current $I_{{\rm meas},f}$ to obtain the actual forward current of the p-i-n device $I_{{\rm diode},f} = I_{{\rm meas},f} - I_{{\rm meas},r}$ (squares and circles), free from shunt leakage component. Notice that after this "cleaning," the forward currents of the two devices become almost identical and match the simulations better (dashed line). The robustness of this cleaning is illustrated by comparing the ideality factors, extracted from the original forward IV, and the "cleaned" IV using $n = q(V_2 - V_1)/k_BT\ln(I_2/I_1)$ [Fig. 3(b) and (c)]. We find that, while the original forward IV gives an unphysical $n > 2$ for all the devices, the "cleaned" IV yields $n \sim 2$ for most of them. The residual spread in n values after cleaning reflects subtraction errors at low current values and measurement tolerances. This provides a simple method to isolate the actual diode current when the measurement is contaminated by $I_{\rm shunt}$.

IV. Discussion

In the literature, $I_{\rm shunt}$ has been attributed to ohmic shunts through microscopic pinholes [6]. While an ohmic shunt does

capture the voltage symmetry and weak temperature dependence of $I_{\rm shunt}$, it cannot explain the power-law voltage dependence [Fig. 2(c)]. The transport mechanism that appears to capture all observed features of $I_{\rm shunt}$ is SCL current $I_{\rm SCL}$. For (shallow) trap-dominated materials like a-Si:H, this can be approximated as [7]

$$I_{\rm SCL} = \frac{9\epsilon\mu_c(\gamma)A}{8}\frac{|V|^{\gamma+1}}{L^{2\gamma+1}}. \quad (1)$$

Here, ϵ is the material permittivity, μ_c is the effective carrier mobility, A is the total area, and L is the thickness. The voltage symmetry of SCL current conduction is immediately obvious from (1), as observed for $I_{\rm shunt}$ [Fig. 2(a)]. The parameter γ is determined by trap distribution inside the bandgap, and with $\beta = \gamma + 1$, it captures the observed nonlinear voltage dependence of $I_{\rm shunt}$ [Fig. 2(b)]. In addition, the temperature dependence of SCL current, which arises from the weak temperature sensitivity of μ_c [7], readily explains the weak temperature dependence of shunt leakage [Fig. 2(c)].

We have seen that the characteristic features of $I_{\rm shunt}$ (Fig. 2) and the empirical method for "cleaning" the dark IV (Fig. 3) are statistically robust results. Moreover, the SCL current postulate also captures the qualitative features consistently. The physical origin of $I_{\rm shunt}$, however, remains an open question and requires further study. The experimental evidences in literature, however, do provide useful clues. First is the metastable nature of $I_{\rm shunt}$, used in shunt "busting/curing" [8]. This involves application of a prolonged reverse bias to eliminate/reduce $I_{\rm shunt}$, without affecting $I_{\rm diode}$. There is also experimental evidence in literature correlating $I_{\rm shunt}$ with localized parasitic conduction paths across the device surface [6], [9]. These observations readily account for the large variation in shunt current magnitude [Fig. 2(d)].

These evidences also suggest that $I_{\rm shunt}$ can be attributed to local nonuniformities, where the ideal p-i-n structure is modified to allow SCL current flow. One possibility, which would result in SCL shunt current, may arise due to the thin n layer ($\sim$10 nm) in these devices. We postulate that, in certain localized spots, the Al from the top AZO layer can diffuse into a-Si:H to form a partial Al filament (shown schematically in Fig. 3(a), inset). This parasitic M/(i)a-Si:H/(p)a-Si:H/M structure can exhibit a single-carrier (hole) symmetric SCL current. We note that similar filaments are observed in a-Si:H based RRAM with Al electrodes [10]. These filaments are also known to exhibit symmetric nonohmic current [11]. The usual barrier for holes is absent for such filaments, possibly due to alloy formation [12] or enhanced electric fields due to sharp metal spikes. Interestingly, this picture can also correlate the switching in a-Si:H resistive memories to shunt "busting" observed for the solar cells. Indeed, other mechanisms suggested for resistive memories (e.g., localized regions of low hydrogen concentration or high defect density) might also be able to explain the mechanism of $I_{\rm shunt}$.

In conclusion, we have established the electrical characteristics of shunt leakage in a-Si:H solar cells. These observations can be explained qualitatively by SCL conduction through localized shunt paths, distributed randomly throughout the film. We have also demonstrated a simple method to extract intrinsic diode current from shunt-contaminated IV measurements. We note that other thin-film PV technologies like CdTe [13] and organic bulk heterojunction cells [14] are also known to show similar nonohmic shunt currents. It is possible that a similar mechanism is also applicable in these cells. If that is the case, the characterization of shunt leakage, and the extraction algorithm presented here, will have broad applications in the process optimization of all thin-film PV technologies.

ACKNOWLEDGMENT

The authors would like to thank D. Kyser and O. Nalamasu for their support and also M. Abraham, K. Ahmed, and M. Lundstrom for the fruitful discussions. The authors would also like to thank the anonymous reviewers for their insightful comments, which helped improve the manuscript significantly.

REFERENCES

[1] K. L. Chopra, P. D. Paulson, and V. Dutta, "Thin-film solar cells: An overview," *Progr. Photovolt.: Res. Appl.*, vol. 12, no. 2/3, pp. 69–92, Mar.–May 2004.

[2] H. Matsuura, A. Matsuda, H. Okushi, and K. Tanaka, "Dark current transport mechanism of p-i-n hydrogenated amorphous silicon diodes," *J. Appl. Phys.*, vol. 58, no. 4, pp. 1578–1583, Aug. 1985.

[3] J. Deng and C. R. Wronski, "Carrier recombination and differential diode quality factors in the dark forward bias current-voltage characteristics of a-Si:H solar cells," *J. Appl. Phys.*, vol. 98, no. 2, pp. 024 509-1–024 509-10, Jul. 2005.

[4] S. S. Hegedus and A. Luque, *Handbook of Photovoltaic Science and Engineering*. Chichester, U.K.: Wiley, 2003.

[5] J. Deng, J. M. Pearce, R. J. Koval, V. Vlahos, R. W. Collins, and C. R. Wronski, "Absence of carrier recombination associated with the defect pool model in intrinsic amorphous silicon layers: Evidence from current-voltage characteristics on p-i-n and n-i-p solar cells," *Appl. Phys. Lett.*, vol. 82, no. 18, pp. 3023–3025, May 2003.

[6] O. Kunz, J. Wong, J. Janssens, J. Bauer, O. Breitenstein, and A. G. Aberle, "Shunting problems due to sub-micron pinholes in evaporated solid-phase crystallised poly-Si thin-film solar cells on glass," *Progr. Photovolt.: Res. Appl.*, vol. 17, no. 1, pp. 35–46, Jan. 2009.

[7] W. Hwang and K. C. Kao, "Unified approach to theory of current injection in solids with traps uniformly and non-uniformly distributed in space and in energy, and size effects in anthracene films," *Solid State Electron.*, vol. 15, no. 5, pp. 523–529, May 1972.

[8] K. R. Lord, II, M. R. Walters, and J. R. Woodyard, "Investigation of shunt resistances in single-junction a-Si:H alloy solar cells," in *Proc. Amorphous Silicon Technol., Mater. Res. Soc. Symp.*, Pittsburgh, PA, 1994, pp. 729–734.

[9] B. G. Yacobi, T. J. McMahon, and A. Madan, "Electron-beam-induced current microcharacterization of fabrication defects in hydrogenated amorphous silicon solar cells," *Solar Cells*, vol. 12, no. 3, pp. 329–335, Aug. 1984.

[10] J. W. Seo, S. J. Baik, S. J. Kang, Y. H. Hong, J.-H. Yang, L. Fang, and K. S. Lim, "Evidence of Al induced conducting filament formation in Al/amorphous silicon/Al resistive switching memory device," *Appl. Phys. Lett.*, vol. 96, no. 5, pp. 053 504-1–053 504-3, Feb. 2010.

[11] A. E. Owen, P. G. L. Comber, J. Hajto, M. J. Rose, and A. J. Snell, "Switching in amorphous devices," *Int. J. Electron.*, vol. 73, no. 5, pp. 897–906, Nov. 1992.

[12] M. Jafar and D. Haneman, "Switching in amorphous-silicon devices," *Phys. Rev. B, Condens. Matter*, vol. 49, no. 19, pp. 13 611–13 615, May 1994.

[13] T. J. McMahon, T. J. Berniard, and D. S. Albin, "Nonlinear shunt paths in thin-film CdTe solar cells," *J. Appl. Phys.*, vol. 97, no. 5, p. 054 503, Mar. 1, 2005.

[14] M. D. Irwin, J. Liu, B. J. Leever, J. D. Servaites, M. C. Hersam, M. F. Durstock, and T. J. Marks, "Consequences of anode interfacial layer deletion. HCl-treated ITO in P3HT:PCBM-based bulk-heterojunction organic photovoltaic devices," *Langmuir*, vol. 26, no. 4, pp. 2584–2591, Feb. 2009.