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An Integration Technology for RF and Microwave Circuits Based on Interconnect Programming

Laleh Rabieirad, Member, IEEE, Edgar J. Martinez, and Saeed Mohammadi, Senior Member, IEEE

Abstract—A configurable integration technology suitable for implementing application specific radio-frequency (RF) and microwave circuits is presented. This postfabrication integration scheme is compatible with complementary metal–oxide–semiconductor (CMOS) technology and utilizes room temperature deposited Parylene-N as low loss and low permittivity dielectric material. Interconnect lines, inductors, and transmission lines fabricated on top of arrays of prefabricated 0.13 μm and 90 nm CMOS transistors coated with Parylene-N are configured to design interconnect programmable RF and microwave circuits. The technology is used to demonstrate three proof of concept interconnect programmable narrowband amplifiers. These amplifiers have center frequencies of 5.5, 6.4, and 18 GHz with forward gain $S_{21}$ of 16.6, 11, and 18.7 dB, respectively. Fabrication simplicity and programmable nature of this technology compared to standard application specific integrated circuit (ASIC) fabrication lowers the cost and time to market of individual ASIC chip.

Index Terms—Coplanar waveguide (CPW) transmission line, inductor, interconnect, low-k dielectric material, narrowband amplifiers, Parylene-N, programmable circuits, radio frequency (RF).

I. INTRODUCTION

HIGH performance radio-frequency and microwave monolithic integrated circuits (RFICs and MMICs) require high quality factor ($Q$) inductors and low loss transmission lines to achieve high gain and low power dissipation [1]–[3]. In advanced complementary metal–oxide–semiconductor (CMOS) and SiGe technologies with the availability of transistors with cutoff frequencies ($f_T$) and maximum oscillation frequencies ($f_{max}$) in the excess of hundreds of gigahertz [4]–[6], back-end-of-line (BEOL) process inductors, and transmission lines have become the bottleneck of RFIC and MMIC designs [7]. The limitation is mainly due to a thin dielectric layer that separates a low resistivity Si substrate from the top metallization used as inductors or transmission lines. Electromagnetic field generated by the RF or microwave signal passing through interconnects, planar inductors and transmission lines penetrates the relatively thin (thickness $<5\,\mu m$) multilayer SiO$_2$ and generates Eddy currents in the low resistivity Si substrate. Heat dissipation due to Eddy currents results in thermal noise injection and RF signal loss that translates into low quality factors of these passive components. Moreover, the thin dielectric layer in the BEOL process results in capacitive coupling to the Si substrate and cross-talk between neighboring signal lines.

Substrate removal of spiral inductors and 3-D helical inductors with and without substrate have been proposed to enhance the quality factor of inductors [8]–[10]. The drawbacks of these techniques, however, are that they are not mechanically stable and are not compatible with standard packaging technologies. A more attractive and cost effective solution is to utilize a thick dielectric layer (>5 $\mu m$) as part of the wafer-level packaging (WLP) process to separate inductors and transmission lines from the substrate. With thick top metallization layer (>2 $\mu m$), this technique results in high quality factor inductors and low loss transmission lines. In [11] and [12] multiple layers of low-k BCB (benzo-cyclobutene) with a permittivity of $\kappa = 2.65$ or SU-8 with permittivity of $\kappa = 3.6$ are used to reduce loss, parasitic capacitance and substrate coupling of inductors or transmission lines. A comparison between the above-IC inductors and transmission lines with the standard BEOL version in [11] shows considerable improvement in the quality factor i.e., by 100%–300% in transmission lines for 16-$\mu m$ thick BCB and 5 $\mu m$ Cu metallization. In [13] inductors on top of BCB are used to demonstrate a high performance voltage controlled oscillator (VCO) and a low noise amplifier (LNA) on a 90 nm CMOS active chip. Moreover, in [14] and [15] a multi-layer polyimide/Au is used to fabricate multifunctional 3-D MMICs using master-slices of GaAs MESFETs or Si bipolar transistors. Despite using a complex multi-layer fabrication on high cost GaAs or Si bipolar devices, this technique achieves a reduced time to market (TTM) by almost a factor of two and lower overall system cost by 50%–75% assuming that GaAs or Si bipolar devices are prefabricated in high volume.

In this paper, we report an interconnect programmable integration technique based on a single layer of Parylene-N as the dielectric layer and a thick Au metal layer as configurable (or programmable) RF interconnects on CMOS substrate. The integration technique is used to integrate RF and microwave circuits on an array of identical CMOS transistor cells [16]. The ability to reroute and program the interconnect layer through the post-processing integration technology facilitates the implementation of application specific RF and microwave circuits based on an identical array of CMOS transistors. The integration technology is used to fabricate three proof-of-concept narrow band RF amplifiers on standard 0.13 $\mu m$ and 90 nm CMOS technologies. It is shown that the low-loss low-$\kappa$ Parylene-N significantly reduces the loss of inductors, and transmission lines resulting in significant gain improvement in RF circuits implemented in this work.

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The cost analysis of this technology shows that despite the added cost of postprocessing procedure, the overall cost per chip is less than standard application specific integrated circuit (ASIC) implementation for low and medium volumes of total throughput. The cost saving is very significant for low throughputs, which means the technology is well suited for low volume manufacturing as well as research and product development. Moreover, ability to program the interconnect lines and passive components reduces the time to market (TTM) when compared with standard ASIC implementation.

II. DIELECTRIC CHARACTERISTICS

In this technology Parylene-N is used as the low-κ low-loss dielectric material that separates interconnects, inductors and transmission lines from the lossy Si substrate. Parylene has been used as an interlayer or coating material in various technologies [17]–[19]. In [17] various types of Parylene as interlayer films are studied and in [18] and [19], Parylene has been used as a coating dielectric. Parylene-N is a member of Parylene family that exhibits very low dissipation factor (tan δ < 6 × 10^{-4}), a low dielectric constant (κ = 2.4), high volume resistivity (1.4 × 10^{17} Ω·cm), as well as high dielectric strength (7000 V/mil) [20]–[22]. Parylene-N deposition is done using a chemical vapor deposition (CVD) system at room temperature resulting in a conformal coverage. Compared to other organic dielectric materials such as SU-8 and BCB which require high temperature procedures, Parylene-N is an excellent choice for coating sensitive circuits with low thermal budgets. Table I illustrates the dielectric properties of Parylene-N and compares it to other organic dielectrics. High frequency electrical properties of Parylene-N are superior to those of Parylene-C and other dielectric materials shown in Table I.

### Table I

<table>
<thead>
<tr>
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<th></th>
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<tbody>
<tr>
<td>Dielectric Constant (ε)</td>
<td>2.4</td>
<td>2.95</td>
<td>2.5</td>
<td>3.4</td>
<td>3.2</td>
</tr>
<tr>
<td>Loss Tangent Tan(δ)</td>
<td>&lt;6 × 10^{-4}</td>
<td>0.002</td>
<td>2 × 10^{-3}</td>
<td>0.0018</td>
<td>0.037</td>
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<tr>
<td>Volume Resistivity (Ω·cm)</td>
<td>1.4 × 10^{17}</td>
<td>8.8 × 10^{16}</td>
<td>1 × 10^{19}</td>
<td>1.5 × 10^{17}</td>
<td>1.8 × 10^{16}</td>
</tr>
<tr>
<td>Melting Point (°C)</td>
<td>420</td>
<td>290</td>
<td>350</td>
<td>None</td>
<td>82</td>
</tr>
<tr>
<td>Thermal Expansion Coefficient (ppm/°C)</td>
<td>69</td>
<td>35</td>
<td>42</td>
<td>~20</td>
<td>~52</td>
</tr>
<tr>
<td>Deposition/Anneal/Cure Temperature (°C)</td>
<td>27</td>
<td>27</td>
<td>180–300</td>
<td>130–200 for ~1 hour</td>
<td>&gt;100 for 1/2 hour</td>
</tr>
<tr>
<td>Dielectric Strength (V/mil)</td>
<td>7000</td>
<td>5600</td>
<td>~5700</td>
<td>7700</td>
<td>2920</td>
</tr>
</tbody>
</table>

The main drawback of Parylene-N is its high thermal expansion coefficient (69 ppm/°C) compared to Si (3.2 ppm/°C [21]), which results in thermal mismatch between Parylene-N layer and Si substrate for large coated areas at high temperatures.

III. FABRICATION PROCEDURE

The interconnect programmable integration technology is performed in two steps. First a device array containing identical transistor cells is fabricated in a standard CMOS or BiCMOS process in high volume. Fig. 1(a) shows the microphotograph of a part of an array chip with an overall size of 4 mm × 4 mm used in this work. The chip contains an array of 60 finger common source RF CMOS transistors with Width W = 60 μm and Length L = 0.13 μm. Each transistor has four contact pads connected to each terminal (2 x source/1 x drain/1 x gate) each with dimensions of 30 μm × 30 μm. A different array chip containing 90 nm CMOS transistors shown in Fig. 1(b) is also used in this work with a pair of 100 finger cascode transistor cells with W = 150 μm, L = 90 nm and contact pad sizes of 30 μm × 30 μm. Once the array chips are fabricated, the postprocessing step which involves deposition of Parylene-N dielectric layer followed by programmable interconnect metallization is carried out on top of the chips.

The postfabrication process starts with deposition of a 15-μm-thick Parylene-N dielectric layer on top of the array chip. The deposition is done at room temperature using a CVD system in around 60 mtorr pressure. Details of the deposition process are discussed in [21]. Following Parylene-N deposition, lithography and reactive ion etching (RIE—Plasma O2 with 990 sccm flow rate for 45 min) are used to create via holes in the dielectric layer to access the terminals of transistors used in the specific circuit. Next, programmable interconnect lines are implemented using lithography, sputtering of Ti(0.05 μm)/gold(0.2 μm) and lift off processes. Walls of via holes are covered with metal due to the conformal nature of the sputtering process, which ensures proper dc contact to each cell. In order to reduce the RF losses of vias, 3 μm Au electroplating is performed. A cross section of the integrated chip is shown in Fig. 2.
IV. INDUCTOR AND TRANSMISSION LINE PERFORMANCE

Schematics of a one turn on-chip inductor of the BEOL process and a one turn inductor fabricated using the postprocessing technology are shown in Fig. 3(a) and (b).

In a typical 0.13 \( \mu m \) CMOS process such as the one used here, the on-chip inductor is fabricated using 0.6 \( \mu m \) of Al metallization on top of 5 \( \mu m \) silicon dioxide multilayer dielectric and Si substrate with a resistivity of 1 \( \Omega \cdot \text{cm} \). The inductor metallization is covered by a 5 \( \mu m \) polyimide passivation layer [Fig. 3(a)]. On the other hand, the postprocessed inductor is fabricated on top of the 5 \( \mu m \) BEOL polyimide and an additional 15-\( \mu m \)-thick Parylene-N layer.

Equivalent circuit models of both inductors with their significant elements are shown in Fig. 3(c) and (d). \( L_s \) and \( R_s \) represent the inductance and series resistance, respectively. \( C_{ds} \) models the feed-through path capacitance. \( C_{ik} \) represents the dielectric capacitance and \( C_{sk} \) and \( R_{sk} \) model the capacitance and resistance of the Si substrate, respectively. Using a thick low loss low permittivity dielectric layer such as the one used in Fig. 3(b) reduces \( C_{ik} \) and effectively isolates the inductor from the substrate. Inductor dielectric loss and high frequency coupling to the substrate are substantially reduced. Equivalent circuit model of the postprocessed inductor reduces to a simple and more ideal model shown in Fig. 3(d). Additionally, the series resistance \( R_s \) of the inductor in the postprocessing technology is slightly lower than the BEOL inductor due to thicker metal used in the process (0.6 \( \mu m \) Al in BEOL device as opposed to 3 \( \mu m \) Au in the postprocessed device). The quality factor and self-resonance frequency of inductors fabricated using the postprocessing technology are expected to be significantly higher than those of the BEOL process due to mitigation of series resistance \( R_s \) and virtual elimination of substrate capacitance and loss in postprocessed inductors. High-frequency electromagnetic simulation (Sonnet) is used to simulate the inductors in both BEOL and postprocessing technologies. The quality factor and inductance values are obtained according to the following equations:

\[
Q = \frac{\text{imag}(Y_{11})}{\text{real}(Y_{11})}, \tag{1}
\]

\[
L = \frac{-\text{imag}(1/Y_{21})}{2\pi f}. \tag{2}
\]

Fig. 4 shows simulation results of one-turn inductors with 1 \( mm \) diameter and 21 \( \mu m \) metal width with various thicknesses of Parylene-N (5 \( \mu m \), 15 \( \mu m \), and 20 \( \mu m \)) as well as the BEOL inductor with same dimensions. The quality factor increases as the thickness of Parylene-N increases. The improvement in the quality factor is significant for Parylene-N layers with thicknesses of more than 15 \( \mu m \) and is more pronounced at higher frequencies because of eliminated effect of the substrate loss. The results also show that inductors with 15- \( \mu m \) and 20-\( \mu m \)-thick Parylene-N have essentially the same performance. 15-\( \mu m \)-thick Parylene-N seems to be the optimum choice for this technology.

We have also studied coplanar waveguide (CPW) transmission lines for the integration technology. Thick Parylene-N layer underneath the CPW line significantly reduces the RF signal loss. Ansoft High Frequency Structure Simulator (HFSS) is used to simulate CPW lines on the CMOS substrate (CMOS BEOL process: 0.6 \( \mu m \) Al metal layer on 5-\( \mu m \)-thick SiO\(_2\) coated Si wafer and passivated by 5 \( \mu m \) Polyimide layer) as well as on Parylene-N layer covering the BEOL chips. Fig. 5 shows the simulated and measured S-parameters of two 1 mm CPW lines studied here. The first CPW line (TL1) has signal width \( W = 21 \mu m \) and signal to ground gap \( G = 28 \mu m \), while the second line (TL2) has \( W = 18 \mu m \) and \( G = 40 \mu m \). CPW lines with exact same geometries are simulated in the BEOL technology. The figure suggests that by using 15- \( \mu m \)-thick Parylene-N layer the transmission loss of the CPW line is reduced by 1.1 dB/mm for TL1 and 0.7 dB/mm for TL2 at 20 GHz compared to BEOL lines.

To verify the accuracy of the simulation, both TL1 and TL2 CPW lines are fabricated on 15 \( \mu m \) Parylene-N dielectric layer coating a 1 \( \Omega \cdot \text{cm} \) CMOS substrate. In order to obtain the inherent S-parameters of the fabricated CPW lines, an open-thru-de-embedding technique on measured S-parameters of the lines is performed [29]. Fig. 5 shows a good agreement between measured and simulated S-parameters for both lines. The measured loss of fabricated TL1 and TL2 at 20 GHz is 0.6 dB/mm and 0.95 dB/mm, respectively.

V. AMPLIFIER DESIGN

Two narrow band RF amplifiers (Amp1 and Amp2) are fabricated on top of a 15 \( \mu m \) Parylene-N layer using one-turn spiral inductors and interconnect lines. Fig. 6(a) shows the schematic of these two-stage amplifiers. Inductor \( L_2 \) is used for input matching, while inductor \( L_2 \) is used as a load. The first stage is a Cascade stage amplifier that provides the voltage gain while the second stage acts as a buffer and facilitates the output matching. All transistors in these two amplifier designs are prefabricated 60 finger CMOS 0.13 \( \mu m \) RF transistors with \( W = 60 \mu m \) and \( L = 120 \mu m \).

Inductors and programmable interconnects are simulated in both Sonnet and HFSS and are optimized for each circuit. The simulated S-parameter data is used in combination with CMOS transistor models available from the foundry to simulate the amplifiers in Cadence Virtuoso Spectre Circuit Simulator. The two amplifiers are optimized to operate at 5.5 GHz and 6.4 GHz with power gains of \( \sim16 \) dB and \( \sim11 \) dB, respectively. It is found that the operating frequency of the amplifiers is limited by the choice of the technology (0.13 \( \mu m \) CMOS), limited self-resonance frequency of inductors and large pad size (30 \( \mu m \times 50 \mu m \)) of transistors, which introduces additional parasitic capacitance.

A third amplifier (Amp3) shown schematically in Fig. 6(b) is designed to operate at microwave frequencies using an array of
Fig. 3. Structure of (a) BEOL inductor and (b) postprocessed inductor. Equivalent circuit model of a spiral inductor on (c) BEOL process (d) thick low-loss dielectric. (Silicon dioxide (5 μm) and polyimide (5 μm) are part of BEOL layers. Polyimide layer is covering the inductor on left and is under the inductor on right; Parylene-N layer is 15 μm.

Fig. 4. Simulation comparison among 1-turn BEOL inductor and inductors on different thicknesses of Parylene-N. All inductors are on top of 1 Ω – cm resistivity Si substrate and a 5-μm-thick silicon dioxide. A 5 μm BEOL polyimide layer covers the BEOL inductor but is underneath other inductors. Parylene-N thicknesses of 5 μm, 15 μm, and 20 μm on top of polyimide are used. Metal width of 21 μm and diameter of 1 mm are used for the simulation.

90 nm cascode CMOS transistors with pad sizes of 30 μm × 30 μm [Fig. 1(b)] and distributed CPW transmission lines as matching networks. CPW transmission lines are preferred over lumped inductors at microwave frequencies as the distributed elements maintain their high quality factor and low losses at such frequencies. Inductors on the other hand suffer from self-resonating effects at high frequencies which results in the degradation of their quality factors. Additionally, CPW lines are easy to fabricate and provide excellent crosstalk suppression due to their well contained electromagnetic field.

Microwave frequency design requires active cells with reasonable power gain at high frequencies. For this reason, prefabricated cascode cells in 90 nm CMOS technology instead of common source transistors in 0.13 μm technology are used for the microwave amplifier design (Amp3). These cells do not have much parasitic capacitance between the two transistors as there is no pad or interconnect in between the two transistors. Moreover, at high frequencies, cascode cells inherently have higher gain, higher output impedance and better device isolation than common source transistors. Additionally, 90 nm transistors have very high cutoff frequency $f_T = 150$ GHz and maximum oscillation frequency $f_{max} = 200$ GHz, which facilitate the design of Amp3 at microwave frequencies. The prefabricated cascode pairs on each cell are 100 finger transistors with widths, $W = 150$ μm and lengths, $L = 0.08$ μm. On-chip prefabricated capacitors (2.5 pF) are utilized as matching and decoupling capacitor at the input port as well as bypassing the dc bias ports. To create an exact model of transistors in this 90 nm digital CMOS technology, a cascode pair with RF pads is separately fabricated and tested under various bias conditions to estimate its performance. Open-thru de-embedding technique on measured data is performed to remove the effect of RF pads and extract the S-parameters of the cascode pair under various bias conditions [29]. Simulated S-parameters of different CPW transmission line sections performed in HFSS are combined with the measured (and de-embedded) S-parameters of the cascode cells in a circuit simulator environment (Ansoft Designer) and the whole circuit is
optimized for optimum performance with a gain of \(\sim 20\) dB at 18 GHz center frequency.

VI. MEASUREMENT

The two lumped amplifiers (Amp1 and Amp2) are fabricated on top of 4 mm \(\times\) 4 mm 0.13 \(\mu\)m CMOS chips containing a 7 \(\times\) 8 array of identical common source transistors. Fig. 7(a) and (b) shows the micro-photographs of these circuits, respectively. As mentioned before both circuits are using the same active array chip and only the top metallization determines the RF performance of the circuits. Fig. 7(c) shows the micro-photograph of Amp3 fabricated on top of a 4 mm \(\times\) 4.8 mm 0.09 \(\mu\)m CMOS chip containing a 4 \(\times\) 5 array of identical cascode transistor cells and lumped capacitors.

2-port S-parameter measurements of the fabricated amplifiers are performed using Agilent 8722 Network Analyzer and on-wafer probing. Calibration is done using a SOLT standard substrate. The results are shown in Fig. 8 along with simulated data. The first amplifier (Amp1) shows a forward transmission gain \(S_{21} = 16.6\) dB at 5.52 GHz center frequency with a bandwidth of 500 MHz (9%). The second amplifier (Amp2) shows a \(S_{21}\) gain of 10.9 dB gain at 6.42 GHz center frequency and a bandwidth of 1.15 GHz (18%). The third amplifier (Amp3) achieves a high \(S_{21}\) gain of 18.7 dB at a center frequency of 18 GHz with a bandwidth of 2.55 GHz (14%). Fig. 8 also suggests that simulated and measured data match very well verifying the strength of EM simulators such as Sonnet and HFSS in combination with circuits simulators in capturing various high frequency effects such as conductive losses, couplings and radiations.

The significance of the thick 15 \(\mu\)m Parylene-N layer to achieve good overall performance from the RF amplifier has been experimentally investigated.

As shown in Fig. 9 the S-parameters of Amp1 fabricated on 15-\(\mu\)m-thick Parylene-N and Amp1 fabricated directly on top of the BEOL polyimide layer (no Parylene-N layer) are compared. The maximum forward transmission gain \(S_{21}\) of the amplifier with Parylene-N layer is 10 dB higher than that of the same amplifier without Parylene-N layer while the quality factor of the gain curve has increased by roughly 28% due the suppression of substrate coupling through using the Parylene-N layer. As adding the dielectric also changes its equivalent capacitor the gain peak occurs at a higher frequency.

VII. DISCUSSION

In the following applications, time to market and cost of this technology are analyzed and compared with those of conventional ASIC technology.

A. Multipurpose Array

In this integration technology inductors, transmission lines and RF interconnects are moved to the third dimension preventing their performance degradation by the lossy Si substrate. Creating multiple turn inductors and ground equalizing bridges for CPW transmission lines in this technology can be done by adding an additional dielectric and metal layers at the expense of higher fabrication cost and post processing complexity. An alternative approach which does not require additional metal/dielectric layers is to prefabricate rows and columns of short metal strips along with the active cells in every array element and utilize them as needed as underpass metallization for multi-turn inductors and ground equalizing bridges for CPW lines.

Although capacitors and resistors can be fabricated using a similar multilayer procedure, a more cost effective approach is...
Planarization is achieved by doing chemical and mechanical polishing and helps subsequent lithographic steps to achieve accurate alignment. On the other hand, in RF and microwave circuits, on-chip interconnect metallization paths require widths of at least several microns to achieve low conductor losses. Therefore, the minimum feature size for RF interconnects, inductors and transmission lines can be easily set to $1 \mu m$ without any performance loss. The integration process used here achieves the rather relaxed $1 \mu m$ feature size by using a standard low-cost optical lithography. As the integration technology relies on a simple one-step metallization and $1 \mu m$ feature optical lithography without a need for planarization, the fabrication time is reduced to few days rather than a few weeks needed for metal processes of standard CMOS process (a reduction by at least 5 times). If one assumes that about half of the fabrication time is allocated to fabricating transistors in an ASIC process and the other half to metallization processes, a 10 fold reduction in the total fabrication time is achieved in the Interconnect Programmable technology. In addition to fabrication time ($FT$), design ($DT$), revision ($RT$), and IC testing times $TT$ need to be considered. In a standard ASIC process, the time to market ($TTM$) is calculated according to

$$TTM_{ASIC} = FT_{ASIC} + DT_{ASIC} + RT_{ASIC} + TT_{ASIC}.$$  \hspace{1cm} (3)

Let us assume that both standard ASIC and the proposed interconnect programmable technology (IPT) require one revision cycle consisting mainly of a fabrication procedure. While the design and test times ($DT$ and $TT$) are not much affected by the choice of implementation, the time it takes to perform fabrication ($FT$) and a single revision ($RT$) are shortened by a factor of 10. Therefore, time to market for interconnect programmable technology ($TTM_{IPT}$) is reduced according to

$$TTM_{IPT} = \frac{1}{10}FT_{IPT} + DT_{IPT} + RT_{IPT} + TT_{IPT}$$

$$= \frac{1}{10}FT_{ASIC} + DT_{ASIC} + \frac{1}{10}RT_{ASIC} + TT_{ASIC}.$$  \hspace{1cm} (4)

### C. Cost

The overall manufacturing cost of integrated circuits is a function of Si area, production volume (throughput), design and testing complexity and the scaling of the technology [30]–[32]. The size of the array chip, in average, is 1.5–2 times larger than the Si area required for a conventional ASIC technology. As the cost of a chip is directly proportional to the Si area used, a prefabricated array of transistors with a fixed chip size in IPT technology costs 1.5–2 times higher than similar ASIC chip provided that they are fabricated with the same throughput (same volume). However, the fabrication cost of each chip is inversely proportional to the total throughput [33]. In IPT integration technology, the array chip is fabricated in large volume with minimum fabrication cost per chip. Let us assume that the array chip is fabricated in total throughput of $N$ and has twice the Si area used in the conventional ASIC implementation. Further assume that the array chip is fabricated using the same process as the conventional ASIC process, i.e., same metallization layers. This may not be necessary as the array chip does

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**Fig. 8.** Comparison between simulated and measured S parameters of (a) amplifier 1 (5.5 GHz), (b) amplifier 2 (6.4 GHz), and (c) amplifier 3 (18 GHz). All amplifiers are fabricated on top of 15 $\mu m$ Parylene-N as well as BEOL layers including 5 $\mu m$ polyimide, 5 $\mu m$ silicon dioxide and low resistivity Si. Amplifier 1 and 2 are fabricated using one turn spiral inductors and array of 0.13 $\mu m$ CMOS transistors and amplifier 3 is fabricated using CPW transmission lines and array of 90 $nm$ CMOS transistors. Solid lines: simulation, dashed lines: measurement.

**Fig. 9.** Measured S-Parameters of amplifier 1 with and without Parylene-N layer. Both fabricated chips have BEOL layers underneath the top Au metallization including 5 $\mu m$ polyimide, 5 $\mu m$ silicon dioxide, and low resistivity Si.

to include commonly used coupling capacitors (several pF) and matching resistors (50 $\Omega$ and 100 $\Omega$) as part of the array chip. The 18 GHz amplifier uses prefabricated 2.5 pF bypass and de-coupling capacitors as shown in Fig. 1(b).

In this rapid integration technology, which resembles circuit breadboards, the sizes of the transistors are fixed to predetermined values. Note that one can design several prefabricated transistors with different sizes [see Fig. 1(b)] as part of the array element. Circuit designers may not be able to choose transistors to the exact size of their simulations but can choose a close size from the available transistor sizes or combine transistor cells for higher current drive. This feature combined with low loss inductors, transmission lines and RF interconnects available in the process results in state of the art RF and microwave circuits with performances beyond what can be achieved in standard ASIC processes.

### B. Time to Market

Advanced CMOS and BiCMOS processes with feature size smaller than 0.25 $\mu m$ require deep submicron metallization with <50 nm alignments using deep UV light sources and especial masks. These processes also require planarization after each metal/dielectric layer deposition and patterning step.
RF and microwave integrated circuits often require one or more revisions to achieve their system specifications. In the first tape-out, chips are usually fabricated and tested in small throughput. As modification in design is often necessary revisions are implemented and chips are fabricated and tested for large market-sized throughputs. Considering the above factors and their contribution to the total cost of ASIC chips one can calculate the cost of an ASIC chip (\( C_{ASIC} \)) according to the following equation:

\[
C_{ASIC} = \frac{N_1 \times (FC_{ASIC} + DC_{ASIC} + TC_{ASIC})}{N_2} + RC_{ASIC} \tag{5}
\]

where FC is the fabrication cost of the first tape-out, DC is the design cost, TC is the test cost, RC is the revision cost and \( N_1 \) and \( N_2 \) are the throughputs for the first fabrication and revision, respectively. The design, test and fabrication cost of the first tape-out contribute to the final cost of each chip. Therefore, the first term in the right-hand side of (5) represents the normalized unit chip cost of the first tape-out and is added to the fabrication cost of each chip in the final throughput.

On the other hand the cost of a chip fabricated in IPT integration technology can be expressed as the following:

\[
C_{IPMA} = \frac{N_1(AC_{IPT} + FC_{IPT} + DC_{IPT} + TC_{IPT})}{N_2} + RC_{IPT} + AC_{IPT} \tag{6}
\]

where the additional array cost (\( AC_{IPT} \)) represents the cost of the array chip added directly to the cost of manufacturing. As mentioned this cost is constant and assumed to be about twice \( (AC_{IPT} = 2) \) the cost of conventional fabrication \( FC_{ASIC} \) at \( N \) throughput.

According to the international semiconductor technology roadmap, the largest cost in CMOS IC manufacturing is lithography [32]. The lithography step includes materials, masks, and inspection, as well as the exposure tool and other process costs. In the 2007 estimate, lithography costs are estimated to be 30%–40% of the total manufacturing cost of integrated circuits [32]. Lithographic costs increase as the technology scales down. As mentioned in the previous section, the utilized postprocessing integration technology does not require submicron lithography. Therefore, it is expected to be very low-cost compared to the processes used to fabricate the array chips.

In Fig. 10, a comparison between the cost of implementing ASICs in a conventional process and in the IPT integration process is made. The cost of each chip is shown as a function of final throughputs \( (N_2) \). The cost of the array chip is shown as a dashed line in the plot. Although other costs such as design, test and post processing costs contribute to the final cost of the IPT chip, it is expected that interconnect programmable technology provides lower cost than that of a standard ASIC chip for low and medium volumes. The cost of ASIC and IPT technologies become comparable at very large throughputs as shown in Fig. 10. At these large manufacturing volumes, it is more cost-efficient to implement ASICs using conventional fabrication technologies.

VIII. CONCLUSION

An interconnect programmable integration technology based on low-loss low-permittivity Parylene-N dielectric layer is presented. The configurability is achieved by fabricating high quality factor and low loss inductors, interconnects and CPW transmission lines on top of 90 nm and 0.13 \( \mu \)m CMOS prefabricated arrays that are coated with 15-\( \mu \)m-thick Parylene-N layer. The post-CMOS integration technology is used to configure the array chips to three proof of concept interconnect programmable narrow band amplifiers operating at 5.5, 6.4, and 18 GHz with 11–18.7 dB \( S_{21} \) gains and 9%–18% bandwidths. The 5.5 and 6.4 GHz amplifiers are implemented using one turn inductors on top of prefabricated transistor arrays in 0.13\( \mu \)m CMOS technology. The 18 GHz amplifier uses fabricated low loss CPW lines on top of an array chip in 90 nm CMOS process.

Low loss passive elements provide up to 10 dB increase in gain while the reconfigurability along with simple fabrication procedure offer reduction in both time to market and fabrication cost compared to the conventional ASIC implementation. The projected cost saving and shorter time to market demonstrate the superiority of this technology for the implementation of cost-effective high-performance RF and microwave configurable circuits. The disadvantage is that the reduction in cost is not applicable in very high throughputs. Additionally, this implementation is not completely independent of the array chip. The metallization are fabricated directly on top of the arrays which makes the two processes interdependent. The future direction points to fabricating the metallization on a separate wafer and bonding it to the array chip in an advanced flip chip technology more accessible for general circuit design.

REFERENCES


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