11-2009

On Backscattering and Mobility in Nanoscale Silicon MOSFETs

Changwook Jeong
Electrical and Computer Engineering, Purdue University, jeongc@purdue.edu

Dimitri Antoniadis
Massachusetts Institute of Technology

Mark S. Lundstrom
School of Electrical and Computer Engineering, Birck Nanotechnology Center, Purdue University, lundstro@purdue.edu

On Backscattering and Mobility in Nanoscale Silicon MOSFETs

Changwook Jeong, *Student Member, IEEE*, Dimitri A. Antoniadis, *Fellow, IEEE*, and Mark S. Lundstrom, *Fellow, IEEE*

***Abstract*—The dc current–voltage characteristics of an n-channel silicon MOSFET with an effective gate length of about 60 nm are analyzed and interpreted in terms of scattering theory. The experimental results are found to be consistent with the predictions of scattering theory—the drain current is closer to the ballistic limit under high drain bias than under low drain bias, and the ON-current in strong inversion is limited by a small portion of the channel near the source. The question of how the low- and high-$V_{\rm DS}$ drain currents are related to the near-equilibrium, long-channel mobility is also addressed. In the process of this analysis, theoretical and experimental uncertainties that make it difficult to extract numerically precise values of the scattering parameters are identified.**

***Index Terms*—Backscattering coefficient, mean free path, mobility, MOSFETs.**

I. Introduction

CONTINUALLY shrinking MOSFET channel lengths have led to a reexamination of traditional physics-based MOSFET models—both analytical and numerical. Natori's [1] ballistic model extended to treat quantum capacitance, 2-D electrostatics, and floating source boundary conditions [2] has been used to assess MOSFET performance against upper limits [3]. Silicon (Si) MOSFETs currently operate between the ballistic and diffusive limits; the scattering model provides a conceptual model for transport in this quasi-ballistic regime [4], [5]. It explains drain current saturation in submicrometer Si MOSFETs in the presence of strong velocity overshoot near the drain—the channel velocity saturates at the beginning of the channel, not in the high-field region near the drain. Scattering theory explains why a MOSFET's drain current is closer to the ballistic value under high drain bias where scattering in the channel increases than under low bias. According to the scattering model, the most important scattering occurs in the low-field region near the beginning of the channel. This provided an explanation for the experimental observation that the low-field near-equilibrium mobility was an important factor in determining a Si MOSFET's ON-current [6]. Finally, the scattering model helps explain why conventional MOSFET models based on drift-diffusion concepts continue to work surprisingly well for nanoscale channel lengths.

As channel lengths continue to shrink, it is important to reexamine the scattering model and its applicability to modern Si MOSFETs. Several numerical studies that support the model have been reported, e.g., [7]–[12], along with a number of careful experimental studies, e.g., [7], [13]–[21]. On the other hand, objections to the model have also been raised [22], [23]. The underlying theoretical uncertainties in the scattering model and in backscattering coefficient measurements have not yet been fully clarified. It is important, therefore, to carefully examine the theory against experimental data for modern Si MOSFETs. Our objective in this paper is to do so. We will show that down to 60 nm channel lengths, scattering theory provides a consistent (though not definitive) explanation for the measured current–voltage (I–V) characteristics of Si MOSFETs. In the process of analyzing and interpreting the data, we will also identify some key experimental and theoretical uncertainties that remain.

This paper is organized as follows. A brief review of the scattering theory of the MOSFET is presented in Section II. In Section III, experimental data are presented and interpreted conventionally using a new semiempirical model. In Section IV, the measured results are related to the ballistic limit, and the results are explained in terms of the backscattering coefficient R or, equivalently, the transmission T. We show that scattering theory provides a consistent description of the performance of n-channel Si MOSFETs and that two different ways of deducing T give similar results. In Section V, we discuss some of the uncertainties in extracting precise numbers for the backscattering parameters and identify some open questions that are becoming increasingly important as devices continue to shrink in size. Conclusions are summarized in Section VI.

II. Review of the Scattering Theory of the MOSFET

Scattering theory seeks to provide a concise description of the essential physics that controls the I–V characteristics of nanoscale MOSFETs [4], [5]. In this section, we present a brief review of the key features of the theory. In the Appendix, we also discuss the relation of scattering theory to conventional MOSFET theory [24]. The results show that although the formalism looks much different from conventional MOSFET theory, the two approaches are actually very closely related, which helps explain why conventional MOSFET models continue to be useful for nanoscale MOSFETs.

Manuscript received March 24, 2009; revised August 13, 2009. First published September 29, 2009; current version published October 21, 2009. The review of this paper was arranged by Editor C.-Y. Lu.

C. Jeong and M. S. Lundstrom are with the Network for Computational Nanotechnology, Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: jeong.changwook@gmail.com).

D. A. Antoniadis is with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139-4307 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2009.2030844

In a MOSFET, electrons are injected from the source into the channel at the virtual source (VS: top of the barrier) whose height is modulated indirectly by the gate voltage. A MOSFET is similar to a bipolar transistor, except that in a bipolar transistor the barrier height is directly modulated by the emitter–base voltage. This analogy between the bipolar transistor and the MOSFET is well known; it is often invoked below threshold, but it also applies above threshold [25].

Natori's [1] theory of ballistic MOSFETs highlights the importance of the source to channel barrier. An expression for the strong inversion drain current in the ballistic limit is readily derived as

$$I_D = WC_G\tilde{v}_T(V_{\rm GS}-V_T) \times\frac{\left[1-\mathcal{F}_{1/2}(\eta_{F1}-qV_{\rm DS}/k_BT)/\mathcal{F}_{1/2}(\eta_{F1})\right]}{\left[1+\mathcal{F}_0(\eta_{F1}-qV_{\rm DS}/k_BT)/\mathcal{F}_0(\eta_{F1})\right]} \quad (1)$$

where

$$\tilde{v}_T \equiv \sqrt{\frac{2k_BT}{\pi m^*}}\frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})} = v_T\frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})} \quad (2)$$

is the thermal injection velocity at the top of the barrier, $\eta_{F1}\equiv(E_{F1}-E_C)/k_BT$, and $\mathcal{F}_j(\eta_{F1})$ is the Fermi–Dirac integral of order j [26]. Equations (1) and (2) assume that a single parabolic subband with an effective mass of m^* is occupied. Rahman *et al.* [2] extended this model to include 2-D electrostatics and the semiconductor capacitance, thereby removing the assumption that the charge at the VS is $C_{\rm ox}(V_{\rm GS}-V_T)$. The ballistic model has also been extended to include self-consistent Schrödinger–Poisson electrostatics, occupation of all relevant subbands, and a tight-binding treatment of band structure that does not assume parabolic bands [27].

Carrier scattering in the channel reduces the current and can be described by a current transmission factor T (or, equivalently, by a backscattering parameter $R=1-T$). If we expand (1) for small drain bias and multiply the ballistic result by a transmission T, we find

$$I_D = WC_G(V_{\rm GS}-V_T)\frac{v_T}{(2k_BT_L/q)}\frac{\mathcal{F}_{-1/2}(\eta_F)}{\mathcal{F}_0(\eta_F)}T_{\rm lin}V_{\rm DS} \quad (3)$$

where $T_{\rm lin}$ is an appropriate average transmission under low drain bias. Under high drain bias, we must account for MOS electrostatics, which attempts to maintain a constant charge at the VS, and thus, we obtain [4]

$$I_D = WC_G(V_{\rm GS}-V_T)\tilde{v}_T\left(\frac{T_{\rm sat}}{2-T_{\rm sat}}\right) \quad (4)$$

where we have assumed that the velocities of the injected and backscattered fluxes are nearly equal. That assumption is well satisfied under low drain bias (3), but not as well satisfied under high drain bias (4) [8], [28]–[30]. For typical conditions, however, the resulting error in $T_{\rm sat}$ is rather small [29], [30]. It should also be emphasized that T is gate and drain voltage dependent, and that according to scattering theory, $T_{\rm sat}>T_{\rm lin}$. Calculating T requires detailed numerical simulation, but it has been argued that the same low-field scattering processes that determine the near-equilibrium mobility control the value of T under both low and high drain bias [4]. The relation of the scattering model to more conventional MOSFET models, like the VS model, is discussed in the Appendix.

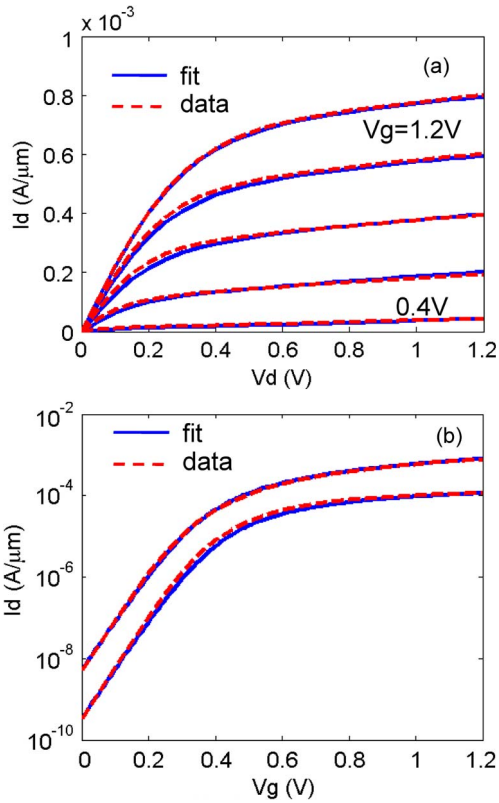


Fig. 1. Comparison of model current (lines) and data (dashed lines) with gate length $L_g=105$ nm. Device parameters: $S=81$ mV/dec; DIBL $=$ 81 mV/V; $I_{\rm ON}=0.80$ mA/μm; and $I_{\rm OFF}=5$ nA/μm. (a) Output I_d–V_d with maximum $V_{\rm GS}=1.2$ V and 0.2 V step. (b) Transfer characteristics at $V_{\rm DS}=0.05$ and 1.2 V. As explained in [35], $\beta=1.8$ is used for nFETs.

III. Results and Analysis

In this section, we will analyze the I–V characteristics of unstrained n-channel Si MOSFETs. The 130-nm CMOS technology (with no engineered Si strain) used for our analysis features a 2.2-nm-electrical effective oxide thickness nitrided gate oxide, a minimum physical gate length $(L_{\rm SEM})$ of 85 nm, a poly-Si gate doped at $\approx 2\times10^{20}$ cm^{-3}, and a $V_{\rm DD}$ of 1.2 V. Fig. 1 (dashed lines) shows the measured I–V characteristics of the MOSFET with $L_{\rm SEM}=105$ nm (equivalently, $L_{\rm eff}=$ 60 nm). Although shorter channels were available, we restricted our analysis to devices that were electrostatically "well-tempered," which sets the minimum effective channel length for the devices that we analyzed to be about 60 nm.

To analyze the results according to conventional MOSFET theory, we used a recently developed semiempirical model, namely, the "VS model," that has proven to be remarkably accurate in describing modern MOSFETs and a reliable way to extract a MOSFET's VS velocity and series resistance [35]. (In Section IV, we will relate this analysis to a scattering parameter analysis of the same device.) The VS model evaluates the drain current at the "VS," the top of the energy barrier between the source and the channel, according to

$$I_D/W = Q_{\rm ix0}v_{x0}F_s \quad (5)$$

where $Q_{\rm ix0}$ is the VS charge density, υ_{x0} is the velocity at the VS, which is a quantity that is always less than the unidirectional thermal (or ballistic injection) velocity as given by (2), and F_s is an empirical drain current "saturation function." The VS charge density is approximated by a semiempirical expression valid below and above threshold. Key fitting parameters in this expression are related to the subthreshold swing and drain-induced barrier lowering (DIBL). The drain current saturation function F_s is similar to the bulk velocity saturation function for Si and includes two parameters, namely, $V_{\rm DSAT} = \upsilon_{x0}\mu_{\rm eff}/L_{\rm eff}$ and β, a parameter that controls the sharpness of the transition. This model has proven to be very successful in fitting a wide range of Si MOSFET data as well as III–V HEMT data. It appears to offer a consistent and reliable way to estimate the VS velocity and the series resistance.

The VS model for this analysis uses only nine parameters. Of these, the following five parameters are directly obtainable from standard device measurements: 1) gate capacitance in strong inversion conditions; 2) subthreshold swing; 3) DIBL coefficient; 4) $I_{\rm OFF}$ at $V_{\rm GS} = 0$ V, and 5) high $V_{\rm DS}$ and gate length (L_g). The fitted physical parameters are low-field mobility $(\mu_{\rm eff})$, parasitic source–drain resistance $(R_{\rm SD}W)$, VS injection velocity (υ_{x0}), and the gate–source (or drain) overlap length $(L_{\rm ov} = (L_{\rm SEM} - L_{\rm eff})/2)$. All I–V and capacitance measurements were done at $T \sim 300$ K. Gate capacitance in strong inversion conditions was measured with a large-area device. $L_{\rm SEM}$ is the actual postetch poly size and is taken as L_g. Mobility was also independently extracted using the $dR_{\rm TOT}/dL$ method proposed by Rim *et al.* [36], with $L_{\rm ov}$ being fitted by the VS model.

Fig. 1 shows the measured and fitted I–V characteristics for nFETs with L_g of 105 nm, which is the minimum physical gate length with DIBL coefficient less than 100 mV/V. The semiempirical model provides a good fit to the measured data, as can be seen in Fig. 1. Table I summarizes the input parameters and the parameters extracted from the model. For this study, the parameters of most interest are given as follows: 1) the extracted series resistance and 2) the VS injection velocity. In Section V, we will discuss the uncertainties in these extracted parameters.

TABLE I
INPUT PARAMETERS AND THE PARAMETERS EXTRACTED FROM THE MODEL. EFFECTIVE MOBILITY WAS OBTAINED FROM THE $dR_{\rm TOT}/dL$ METHOD AND IS VERY CLOSE TO THE VALUE OBTAINED FROM THE VS MODEL

Input Parameters	Extracted Parameters
C_g = 1.55x10^{-6} F/cm^{-2}	υ_{x0} = 0.76x10^7 cm/s
DIBL = 81mV/V	$R_{SD}W$ = 220 Ω.μm
S = 81 mV/dec	μ_{eff}=260 cm^2/V.s
I_{off} = 5 nA/μm	L_{ov} = 22.5 nm
L_g = 105 nm	

IV. SCATTERING MODEL ANALYSIS

The most direct way to analyze the measured I–V characteristics in terms of the backscattering model is to compare the measured I–V characteristic to the expected ballistic characteristic and to interpret the difference in terms of scattering parameters. This approach necessarily entails simplifying assumptions in the ballistic model. Alternatively, several authors have directly extracted backscattering coefficients from terminal measurements [13]–[17]. In some cases, assumptions about the functional form of the scattering parameters are made—assumptions that we wish to avoid. Our approach, therefore, will be to directly compare the measured I–V characteristic to a theoretically computed ballistic characteristic and to deduce T without further assumptions. Scattering theory predicts that T is closer to 1 under high drain bias, when scattering increases, than under low drain bias. Our results confirm this prediction. Scattering theory also relates T to the low-field near-equilibrium mobility. We confirm this relation under low drain bias. Under high drain bias, a definitive test is more difficult, but we show that the measured results are consistent with scattering theory. Finally, we relate the results to the conventional analysis of Section III.

Computing the ballistic current for realistic 2-D bulk MOSFET geometry is a challenge. In a recent work [9], [10], [18], it was shown that multisubband population and the Fermi–Dirac statistics needs to be taken into account. Our approach, therefore, is based on the top of the barrier model with the self-consistent Schrödinger–Poisson electrostatics to determine which subbands are occupied [i.e., we do not use the simplified model summarized in (1) and (2)]. In this approach, Rahman *et al.*'s extension [2] of the Natori model [1] is used to treat the semiconductor capacitance and 2-D electrostatics. The ballistic I–V and the measured I–V characteristics for nFETs with $L_{\rm SEM} = 105$ nm (equivalently, $L_{\rm eff} = 60$ nm) are compared in Fig. 2. The plots compare the measured I–V characteristics, which include scattering in the channel and series resistance with a model that assumes a ballistic channel with the series resistance extracted from the semiempirical VS model added. Two quantities of interest are the ratio of the measured channel resistance at high $V_{\rm GS}$ of 1.2 V to the computed ballistic resistance (or measured intrinsic linear current to ballistic current) and the ratio of the velocity extracted from the VS model at high intrinsic $V_{\rm GS}$ and $V_{\rm DS}$ to the theoretical ballistic injection velocity. The extracted transmission under low and high drain bias are

$$B_{\rm lin} = T_{\rm lin} = \left.\frac{I_{\rm ON\_MEA}}{I_{\rm ON\_BAL}}\right|_{V_{\rm DS}=50\,\rm mV} = 0.20 \tag{6}$$

$$B_{\rm sat} = \frac{T_{\rm sat}}{2 - T_{\rm sat}} = \frac{I_{\rm ON\_MEA}}{I_{\rm ON\_BAL}} = 0.56 \rightarrow T_{\rm sat} = 0.72. \tag{7}$$

In agreement with the prediction of scattering theory, the current transmission is higher under high $V_{\rm DS}$ than for low $V_{\rm DS}$.

Scattering theory relates T to the mean free path under low and high drain biases. The near-equilibrium mean free path for backscattering in a long-channel transistor can be estimated

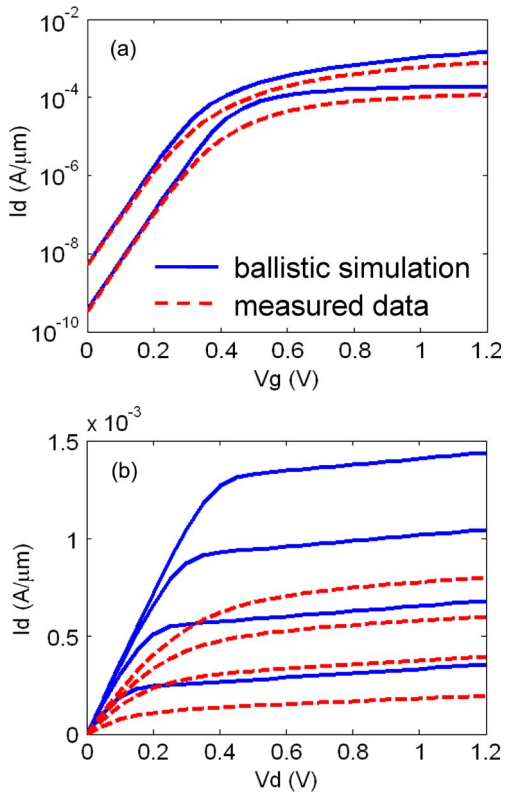


Fig. 2. Comparison of ballistic simulation current (lines) and data (dashed lines) with gate length $L_g = 105$ nm. (a) Transfer characteristics at $V_{\rm DS} = 0.05$ and 1.2 V. (b) Output I_d–V_d with maximum $V_{\rm GS} = 1.2$ V and 0.2 V step. Device parameters used to extract transmission ($T_{\rm lin}$ and $T_{\rm sat}$): $I_{\rm ON\_BAL} = 1.44$ mA/μm; $v_{\rm inj\_BAL} = 1.48 \times 10^7$ cm/s; $R_{\rm BAL}W = 43\ \Omega \cdot \mu$m; $I_{\rm ON\_MEA} = 0.80$ mA/μm; $R_{\rm TOT}W = 435\ \Omega \cdot \mu$m; and $R_{\rm CH}W = R_{\rm TOT}W - R_{\rm SD}W = 215\ \Omega \cdot \mu$m.

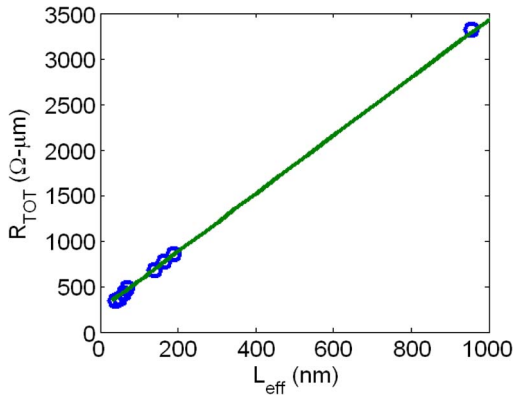


Fig. 3. Plot of $R_{\rm TOT}$ versus $L_{\rm eff}$. Mobility was extracted using $\mu_{\rm eff} = 1/W(\partial R_{\rm TOT}/\partial L)Q(0)$. A linear curve fitting of $R_{\rm TOT}$ versus $L_{\rm eff}$ ranging from 60 to 205 nm was used for analysis. Extracted $\mu_{\rm eff} = 260$ cm^2/V $\cdot$ s. This value was matched with mobility value from an empirical model. $Q(0)$ is obtained by C–V curve integration [21]. Gate drive is fixed about $V_{\rm OV} \sim 0.90$ V.

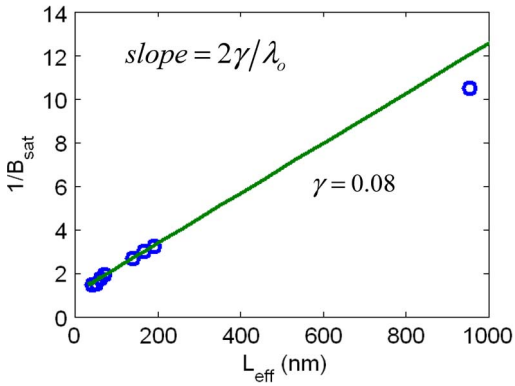


Fig. 4. Plot of $1/B_{\rm sat}$ versus $L_{\rm eff}$. A linear curve fitting of $1/B_{\rm sat}$ versus $L_{\rm eff}$ ranging from 60 to 205 nm was used for analysis. The very-long-channel data point was not included because a long-channel MOSFET will not be described by the short-channel models in this paper. Critical length is about 8% of channel length. Extracted critical length for nFETs with $L_{\rm eff}$ is 4.8 nm.

from the mobility assuming that only single parabolic subband is occupied

$$\mu_{\rm eff} = \frac{v_T \lambda_0}{2k_B T/q}\left[\frac{\mathcal{F}_{-1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})}\right]. \tag{8}$$

This assumption is reasonable because our Schrödinger–Poisson simulations show that 78% of electrons reside in the first subband. Mobility can be determined experimentally taking the derivative of $R_{\rm TOT}$ with respect to channel length, which eliminates the dependence of mobility on the parasitic series resistance, and the particular choice of $L_{\rm eff}$ definition does not affect the extraction [36]. As shown in Fig. 3, the extracted mean free path λ_0 is 14 nm. Scattering theory predicts that transmission in the linear region for nFETs with $L_g = 105$ nm and $L_{\rm eff}(= L_g - 2L_{\rm OV}) = 60$ nm is

$$T_{\rm lin} = \frac{\lambda_o}{\lambda_o + L_{\rm eff}} = 0.19 \tag{9}$$

which is very close to the value extracted from the current ratio (6).

Saturation analysis by scattering theory is based on the following two key assumptions: 1) the appropriate mean free path is approximately a near-equilibrium one and 2) the critical length is much less than the channel length. Under high drain bias, the mean free path and critical length cannot be determined independently because varying $V_{\rm GS}$ or temperature to vary the mean free path also causes the critical length to vary. In a recent work [19], the critical length was extracted using the near-equilibrium mean free path, and it was shown that the critical length varied with $V_{\rm GS}$ or temperature. Our approach is to assume that the appropriate mean free path is the measured near-equilibrium mean free path in a long-channel MOSFET and, then, to determine the critical length from a plot of $1/B_{\rm sat}$ versus channel length. The dependence of $B_{\rm sat}$ on the parasitic series resistance and the particular choice of $L_{\rm eff}$ definition does not affect this extraction. Assuming the critical length is linearly proportional to the channel length as $\ell = \gamma \times L_{\rm eff}$, the inverse of ballistic factor can be expressed as

$$\frac{1}{B_{\rm sat}} = 1 + \frac{2\ell}{\lambda_0} = 1 + \frac{2\gamma}{\lambda_0} L_{\rm eff}. \tag{10}$$

$B_{\rm sat}$ was extracted using (7), with DIBL being accounted for. As shown in Fig. 4, the observed linear relation of critical length with channel length supports our assumptions. This linear relation was also verified by a quantum corrected Monte Carlo simulation [37]. The ratio of the critical length to the channel

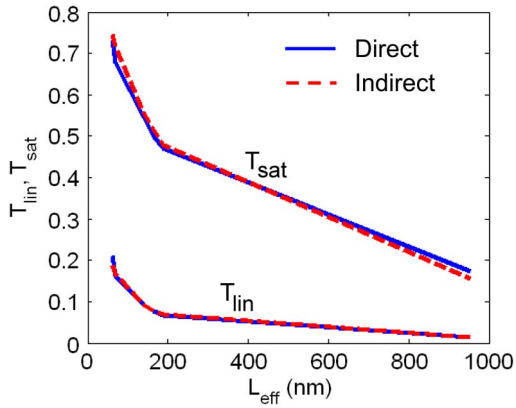


Fig. 5. Plot of $T_{\rm lin}$ and $T_{\rm sat}$ for transistors with different channel length. "Direct" represents evaluation of $T_{\rm lin}$ and $T_{\rm sat}$ according to (6) and (7), while "indirect" represents evaluation of $T_{\rm lin}$ and $T_{\rm sat}$ according to (9) and (11).

length is about 8% (or ∼4.8 nm), supporting the existence of a short critical region at the beginning of channel. A ratio of about 10% has also been reported for different types of devices such as double-gate SOI [37], [38] and bulk MOSFETs [19]. Using the critical length and the mean free path obtained from the near-equilibrium mobility, we can deduce the transmission in the saturation region for nFETs with $L_{\rm eff} = 60$ nm as

$$T_{\rm sat} = \frac{\lambda_o}{\lambda_o + \ell} = 0.74 \tag{11}$$

which is close to the value obtained from the current ratio as given by (7).

In summary, for nFETs with $L_{\rm eff} = 60$ nm, comparing measured currents to a computed ballistic model gives transmission with $T_{\rm lin} = 0.20$ and $T_{\rm sat} = 0.72$, which agrees well with the one with transmission $T_{\rm lin} = 0.19$ and $T_{\rm sat} = 0.74$, computed from the near-equilibrium mobility. In addition, the two approaches were used to evaluate of $T_{\rm lin}$ and $T_{\rm sat}$ for different transistors with channel lengths up to 1 μm, as shown in Fig. 5. The results show that the discrepancy between the two methods of is no larger than 5%. The fact that these two approaches give similar results supports scattering theory, but we mention again that we have not independently determined the mean free path and the critical length.

V. Discussion

The analysis presented in Section IV shows that this nanoscale Si MOSFET behaves as expected from scattering theory. It was necessary, however, to make several theoretical assumptions to generate the ballistic I–V characteristics against which we compared the measured results, and there are uncertainties in the experimental results themselves and in the parameters extracted. In this section, we briefly identify and discuss some of these issues. Finally, several issues arise as devices continue to scale, and some of those issues that, in our opinion, deserve additional study will be identified.

First, it should be pointed out that the assumption of parabolic energy bands in the ballistic model may overestimate the ballistic injection velocity—perhaps by 20% for electrons in unstrained Si [27]. Second, we should note that another assumption on which (3) and (4) are based is that at the top of the barrier, the average forward velocity (υ^+), and backward velocity (υ^-) are same and equal to the thermal velocity. This fact has been pointed out in [8] and [28]–[30] and has been examined by a quantum-corrected Monte Carlo simulation in [8], [29], and [30]. It turned out that $\upsilon^- \approx 0.7\tilde{\upsilon}_T$, and $R_{\rm sat}$ was overestimated by about 10% with this assumption (the error in $T_{\rm sat}$ is somewhat smaller.)

The scattering model also assumes that carriers injected into the channel from the source occupy states at the top of the barrier according to the Fermi level of the source (i.e., that no source starvation [23] occurs). To extract the inversion layer density at the VS, the VS model assumes that $Q_{\rm ix0} = C_G(V_{\rm GS} - V_T)$. This assumption is expected to be well-justified for well-tempered devices free of significant short-channel effects.

Computation of the channel transmission coefficient brings up additional issues. Under low drain bias, computing $T_{\rm lin}$ is straightforward with relatively few assumptions [39]. Computing $T_{\rm sat}$ under high drain bias, however, raises several issues [40]. It has been shown that the critical length is not the spatial extent of the k_BT_L/q potential drop, but that it depends on the shape of the profile and on the specific scattering mechanisms [8], [9], [11], [41]. The assumption that the appropriate mean free path is the near-equilibrium mean free path is clearly an approximation [41]. In very short devices, it has been suggested that the drain-end scattering becomes important [22], [42]. In a very recent study, however, it was found that the drain-end scattering is negligible due to inelastic scattering in the channel [8]. In spite of these uncertainties, however, scattering theory provides good quantitative explanation of measured data, as discussed in Section IV. As channel lengths continue to shrink, the issues discussed here may become more important. Nevertheless, the most important insight from scattering theory is a qualitative one—that low energy scattering processes appear to control the drain current of a nanoscale MOSFET even under high drain bias.

Experimental uncertainties mostly come from the evaluation of inversion charge. Integration of the C–V curves measured on a large-area device neglects the gate length dependence of the poly depletion [43], and the spread of C–V curves in short-channel devices [44]. In the direct measurement of inversion charge in short-channel devices recently proposed [20], the accuracy of effective channel length is of critical importance. Even if it is possible to obtain the inversion charge in the short-channel devices, it is hard to verify the common underlying assumption that the extracted inversion charge is the charge at the top of the barrier. These experimental uncertainties have also been pointed out in [45]. The extraction of the critical length assumes that the mean free path is the near-equilibrium one obtained from the low-field mobility, which brings in other uncertainties such as the effective channel lengths, depending on the extraction method. The sensitivity of the mobility to the definition of effective channel lengths is critical—particularly in the very-short-channel devices, as shown in [18].

In our approach for extracting transmission using the empirical VS model, there are also uncertainties in the series resistance. The series resistance variations affect $R_{\rm lin}$ [18] and

$R_{\rm sat}$ [16], [18], [21] and have more impact on the linear region than on the saturation region. We assume that the accuracy of our extracted series resistance is within $\pm 10\%$ (therefore, $R_{\rm SD}W = 220 \pm 22\ \Omega \cdot \mu$m), because the series resistance obtained by fitting the Berkeley Short-channel IGFET Model to the same experimental data is 200 $\Omega \cdot \mu$m. The variation in transmission due to the series resistance uncertainties are $T_{\rm lin} = 0.20 \pm 0.02(10\%)$ and $T_{\rm sat} = 0.72 \pm 0.01(2.5\%)$, indicating that the series resistance uncertainties in the linear region are more critical. For today's high-performance transistors, the parasitic series resistance is comparable to the channel resistance, but the gate–source potential drop due to the parasitic resistance under high drain bias is still about 10% of the supply voltage. This explains why the series resistance variation causes more uncertainties in the linear region than in the saturation region. Ballistic simulation results show that the injection velocity increases with increasing $V_{\rm GS}$ due to carrier degeneracy. However, the experimentally extracted injection velocity from the VS model does not show this behavior. We believe that surface roughness scattering may offset the effects of carrier degeneracy. Comparing the VS model extracted VS velocity to the theoretical ballistic injection velocity gives $T_{\rm sat} = 0.68$, which is about 5% lower than the value that we obtained in (7). This difference is attributed to the difference in the inversion charge at the top of the barrier between the ballistic simulation ($= 0.97 \times 10^{-6}$ C/cm^2) and the VS model ($= 1.07 \times 10^{-6}$ C/cm^2) for $V_{\rm DS} = 0$ and $V_{\rm GS} = 1.2$ V.

Measurements focus on $T_{\rm sat}$, for which there is no simple theoretical expression. Caution is therefore required when using measurement techniques that assume a specific functional form for $T_{\rm sat}$ (e.g., assuming that it depends on a critical length and that the critical length is the kT length). As devices scale down, it should also be noted that there are some additional theoretical issues that need to be carefully examined such as source starvation [23], long-range Coulomb interactions [46], and separation of the device into source and channel regions as the top of the barrier moves into the source [8], [38].

VI. Summary and Conclusion

The I–V characteristics of a nanoscale Si N-MOSFET have been analyzed in terms of conventional MOSFET theory and in terms of backscattering theory. The key conclusions of this paper are listed as follows.

1) The scattering model provides a consistent conceptual model for nanoscale Si MOSFETs with channel lengths down to about 60 nm in terms of the transmission and injection velocity or alternatively in terms of traditional MOSFET theory.
2) Extraction of precise numbers for transmission, ballistic efficiency, etc., is somewhat clouded by a number of theoretical and experimental uncertainties.
3) Consistent estimates of T in the linear and saturated regions are obtained by two different techniques, which support, but do not prove, the validity of scattering theory.
4) Modern Si MOSFETs deliver more than half of the ballistic ON-current and much less than half of the ballistic linear current.
5) Low energy scattering processes and the low energy portion of $E(k)$ are the most important factors in determining a nanoscale MOSFET's drain current under both low and high drain voltages.
6) Under high drain bias, a very short "bottleneck" near the source limits the drain current.
7) Measurement techniques that rely on an assumed functional form for T in the saturated region should be regarded with suspicion.

As MOSFET channel lengths continue to shrink, concerns about the validity of the scattering model arise. So far, there has been, to our knowledge, no clear experimental evidence of the breakdown of scattering theory, but as scaling continues, clear experimental tests are needed. In that regard, recent research on novel channel material MOSFETs [47], [48] provides us with an opportunity to examine our theoretical models for MOSFETs in regions of parameter space that are far removed from the traditional Si MOSFET.

Appendix

The expressions for drain current as given by scattering theory and conventional MOSFET theory look much different, but there is a close connection between the two approaches (which helps explain why the traditional MOSFET models continues to work so well for nanoscale MOSFETs). To see this connection, assume Boltzmann statistics ($\mathcal{F}_j(\eta_{F1}) \rightarrow e^{\eta_{F1}}$) so that(3) becomes

$$I_D = WC_G(V_{\rm GS} - V_T)\left(\frac{\upsilon_T}{2k_BT_L/q}\right)T_{\rm lin}V_{\rm DS} \qquad \text{(A1)}$$

where $T_{\rm lin}$ is the transmission coefficient $T_{\rm lin} = \lambda_0/(L_{\rm eff} + \lambda_0)$, with λ_0 being the near-equilibrium mean free path for backscattering. The ballistic current ratio ($B_{\rm lin} = I_{D\_{\rm MEA}}/I_{D\_{\rm BAL}}$) and transmission ($T_{\rm lin}$) are related as $B_{\rm lin} = T_{\rm lin} = 1 - R_{\rm lin}$. Under high bias, the drain current becomes

$$I_D = WC_G(V_{\rm GS} - V_T)\upsilon_T\left(\frac{T_{\rm sat}}{2 - T_{\rm sat}}\right) \qquad \text{(A2)}$$

where Boltzmann statistics has been assumed, and $T_{\rm sat}$ is the transmission coefficient $T_{\rm sat} = \lambda_0/(\ell + \lambda_0)$, with ℓ being the so-called critical length. The ballistic current ratio ($B_{\rm sat} = I_{\rm ON\_MEA}/I_{\rm ON\_BAL}$) and transmission ($T_{\rm sat}$) are related as $B_{\rm sat} = T_{\rm sat}/(2 - T_{\rm sat}) = (1 - R_{\rm sat})/(1 + R_{\rm sat})$.

To see how the scattering model is related to the traditional MOSFET model, we use the simple relation between the near-equilibrium mean free path for backscattering λ_0 and the diffusion coefficient D_n, $D_n = \nu_T\lambda_0/2$ along with the Einstein relation, so that (A1) becomes

$$I_D = \frac{W}{L_{\rm eff}}C_G(V_{\rm GS} - V_T)\left(\frac{1}{\mu_B} + \frac{1}{\mu_n}\right)^{-1}V_{\rm DS} \qquad \text{(A3)}$$

where $\mu_n = \nu_T\lambda_0/(2k_BT/q)$, and we define $\mu_B \equiv \nu_T L_{\rm eff}/(2k_BT/q)$ as the "ballistic mobility" [31]–[34]. It has been reported that the ballistic mobility explains partly [33] or fully [34] the apparent degradation of mobility in a

very-short-channel devices. The scattering model is, therefore, equivalent to the traditional model except that it includes the ballistic mobility, which becomes important for channel materials with very high real mobility such as III–V or for very-short-channel lengths.

Under high drain bias (using, again, the simple relation between the near-equilibrium mean free path for backscattering λ_0 and the diffusion coefficient D_n), (A2) becomes

$$I_D = WC_G(V_{\rm GS} - V_T)\left[\frac{1}{\upsilon_T} + \frac{1}{(D_n/\ell)}\right]^{-1}. \qquad \text{(A4)}$$

This expression is similar to the traditional velocity saturation model, except that channel velocity saturates at the beginning of the channel, not in the high-field region near the drain. The physical picture is that carriers diffuse across a short bottleneck near the beginning of the channel, and they are collected by the high-field portion of the channel. Carriers cannot diffuse faster than the thermal velocity, so the appropriate velocity is the slower of the ballistic injection velocity or the diffusion velocity D_n/ℓ. Just as the collector current in a Si bipolar transistor is typically limited by diffusion of carriers across the base, the ON-current of a nanoscale MOSFET is limited by the diffusion of carriers across the low-field bottleneck near the beginning of the channel. Key assumptions under high drain bias are that a very short bottleneck region at the beginning of channel exists and controls the drain current and that the low-field near-equilibrium mean free path λ_0 is the relevant parameter that controls the current. The following two key questions are considered: 1) How close is D_n to its near equilibrium value and 2) what is the magnitude of the critical length ℓ? We do not wish to push this model too far—full numerical simulations are needed to compute T from device and material parameters, but the analysis presented here suggests that this simple model describes the essential physics of the nanoscale MOSFET and that the close relation of the scattering model to the conventional MOSFET model helps explain why conventional MOSFET models based on drift-diffusion concepts continue to work surprisingly well for nanoscale channel lengths.

ACKNOWLEDGMENT

The authors would like to thank the Network for Computational Nanotechnology for the computational support, the Birck Nanotechnology Center for the electrical characterization, H. Takeuchi and Dr. J. Wetzel at SVTC for providing the MOSFETs analyzed in this paper, and R. Kim and E. Islam at Purdue University for the helpful discussions. D. A. Antoniadis and M. Lundstrom would like to thank the Materials Structures and Devices Center of the Semiconductor Research Center-Focus Center Research Program.

REFERENCES

[1] K. Natori, "Ballistic metal–oxide–semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76, no. 8, pp. 4879–4890, Oct. 1994.

[2] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1853–1864, Sep. 2003.

[3] F. Assad, Z. Ren, S. Datta, M. Lundstrom, and P. Bendix, "Performance limits of silicon MOSFETs," in *IEDM Tech. Dig.*, 1999, pp. 547–550.

[4] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul. 1997.

[5] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 133–141, Jan. 2002.

[6] M. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 293–295, Jun. 2001.

[7] G. Timp, J. Bude, K. Bourdelle, J. Garno, A. Ghetti, H. Gossmann, M. Green, G. Forsyth, Y. Kim, R. Kleiman, F. Klemens, A. Kornblit, C. Lochstampfor, W. Mansfield, S. Moccio, T. Sorsch, D. Tennant, W. Timp, and R. Tung, "The ballistic nano-transistor," in *IEDM Tech. Dig.*, 1999, pp. 55–58.

[8] P. Palestri, D. Esseni, S. Eminente, C. Fiegna, E. Sangiorgi, and L. Selmi, "Understanding quasi-ballistic transport in nano-MOSFETs—Part 1: Scattering in the channel and in the drain," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2727–2735, Dec. 2005.

[9] P. Palestri, R. Clerc, D. Esseni, L. Lucci, and L. Selmi, "Multi-subband-Monte-Carlo investigation of the mean free path and of the kT layer in degenerated quasi ballistic nanoMOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 1–4.

[10] K. Natori, "Ballistic MOSFET reproduces current–voltage characteristics of an experimental device," *IEEE Electron Device Lett.*, vol. 23, no. 11, pp. 655–657, Nov. 2002.

[11] R. Clerc, P. Palestri, and L. Selmi, "On the physical understanding of the kT-layer concept in quasi-ballistic regime of transport in nanoscale devices," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1634–1640, Jul. 2006.

[12] R. Clerc, P. Palestri, Q. Rafhay, M. Ferrier, G. Pananakakis, G. Ghibaudo, and L. Selmi, "Quasi ballistic transport in advanced MOSFET devices," in *Proc. SIMCND*, 2007, pp. 35–40.

[13] M.-J. Chen, H.-T. Huang, K.-C. Huang, P.-N. Chen, C.-S. Chang, and C. Diaz, "Temperature dependent channel backscattering coefficients in nanoscale MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 39–42.

[14] H. N. Lin, H. W. Chen, C. H. Ko, C. H. Ge, H. C. Lin, T. Y. Huang, and W. C. Lee, "Channel backscattering characteristics of uniaxially strained nanoscale CMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 676–678, Sep. 2005.

[15] K. Ang, H. Chin, K. Chui, M. Li, G. S. Samudra, and Y. Yeo, "Carrier backscattering characteristics of strained silicon-on-insulator n-MOSFETs featuring silicon-carbon source/drain regions," *Solid State Electron.*, vol. 51, no. 11/12, pp. 1444–1449, Nov./Dec. 2007.

[16] V. Barral, T. Poiroux, M. Vinet, J. Widiez, B. Previtali, P. Grosgeorges, G. Le Carval, S. Barraud, J. L. Autran, D. Munteanu, and S. Deleonibus, "Experimental determination of the channel backscattering coefficient on 10–70 nm-metal-gate double-gate transistors," *Solid State Electron.*, vol. 51, no. 4, pp. 537–542, Apr. 2007.

[17] Y. Tsai, S. Chung, P. Liu, C. Tsai, Y. Lin, C. Tsai, G. Ma, S. Chien, and S. Sun, "The channel backscattering characteristics of sub-100 nm CMOS devices with different channel/substrate orientations," in *Proc. Int. Symp. VLSI Technol., Syst. Appl.*, 2007, pp. 1–2.

[18] V. Barral, T. Poiroux, D. Munteanu, J. Autran, and S. Deleonibus, "Experimental investigation on the quasi-ballistic transport—Part 2: Backscattering coefficient extraction and link with the mobility," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 420–430, Mar. 2009.

[19] M. J. Chen, H. T. Huang, Y. C. Chou, R. T. Chen, Y. T. Tseng, P. N. Chen, and C. H. Diaz, "Separation of channel backscattering coefficients in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1409–1415, Sep. 2004.

[20] A. Tsuda and A. Uchida, "Intrinsic delay of nanoscale MOSFETs under ballistic transport," in *Proc. Ext. Abstr. Int. Conf. SSDM*, 2006, pp. 352–353.

[21] A. Lochtefeld and D. A. Antoniadis, "On experimental determination of carrier velocity in deeply scaledNMOS: How close to the thermal limit?" *IEEE Electron Device Lett.*, vol. 22, no. 2, pp. 95–97, Feb. 2001.

[22] A. Svizhenko and M. Anantram, "Role of scattering in nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1459–1466, Jun. 2003.

[23] M. Fischetti, L. Wangt, B. Yut, C. Sachs, P. Asbeckt, Y. Taurt, and M. Rodwell, "Simulation of electron transport in high-mobility MOSFETs: Density of states bottleneck and source starvation," in *IEDM Tech. Dig.*, 2007, pp. 109–112.

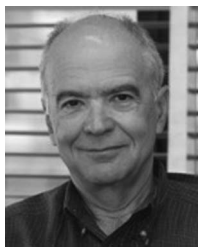
[24] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[25] E. O. Johnson, "The insulated-gate field-effect transistor—A bipolar transistor in disguise," *RCA Rev.*, vol. 34, pp. 80–94, 1973.

[26] R. Kim and M. Lundstrom, *Notes on Fermi-Dirac Integrals*, 3rd ed., 2008. [Online]. Available: http://nanohub.org/resources/5475
[27] Y. Liu, N. Neophytou, T. Low, G. Klimeck, and M. Lundstrom, "A tight-binding study of the ballistic injection velocity for ultrathin-body SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 866–871, Mar. 2008.
[28] K. Natori, "Scaling limit of the MOS transistor: A ballistic MOSFET," *IEICE Trans. Electron.*, vol. E84-C, no. 8, pp. 1029–1036, Aug. 2001.
[29] H. Tsuchiya, K. Fujii, T. Mori, and T. Miyoshi, "A quantum-corrected Monte Carlo study on quasi-ballistic transport in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2965–2971, Dec. 2006.
[30] V. Barral, T. Poiroux, J. Saint-Martin, D. Munteanu, J. Autran, and S. Deleonibus, "Experimental investigation on the quasi-ballistic transport—Part 1: Determination of a new backscattering coefficient extraction methodology," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 408–419, Mar. 2009.
[31] M. Shur, "Low ballistic mobility in submicron HEMTs," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 511–513, Sep. 2002.
[32] J. Wang and M. Lundstrom, "Ballistic transport in high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1604–1609, Jul. 2003.
[33] M. Zilli, D. Esseni, P. Palestri, and L. Selmi, "On the apparent mobility in nanometric n-MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 1036–1039, Nov. 2007.
[34] J. Lusakowski, W. Knap, Y. Meziani, J. P. Cesso, A. El Fatimy, R. Tauk, N. Dyakonova, G. Ghibaudo, F. Boeuf, and T. Skotnicki, "Electron mobility in quasi-ballistic Si MOSFETs," *Solid State Electron.*, vol. 50, no. 4, pp. 632–636, Apr. 2006.
[35] A. Khakifirooz, D. Antoniadis, and O. Nayfeh, "A simple semi-empirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674–1680, Aug. 2009.
[36] K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, J. Cai, I. Res, D. Center, T. Center, and Y. Heights, "Low field mobility characteristics of sub-100 nm unstrained and strained Si MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 43–46.
[37] S. Eminente, D. Esseni, P. Palestri, C. Fiegna, L. Selmi, and E. Sangiorgi, "Understanding quasi-ballistic transport in nano-MOSFETs—Part 2: Technology scaling along the ITRS," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2736–2743, Dec. 2005.
[38] M. Zilli, P. Palestri, D. Esseni, and L. Selmi, "On the experimental determination of channel back-scattering in nanoMOSFETs," in *IEDM Tech. Dig.*, 2007, pp. 105–108.
[39] S. Datta, *Electronic Transport in Mesoscopic Systems*. Cambridge, U.K.: Cambridge Univ. Press, 1997.
[40] M. Lundstrom, *Fundamentals of Carrier Transport*. Cambridge, U.K.: Cambridge Univ. Press, 2000.
[41] R. Kim and M. Lundstrom, "Physics of carrier backscattering in one- and two-dimensional nanotransistors," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 132–139, Jan. 2009.
[42] A. Mouis and S. Barraud, "Velocity distribution of electrons along the channel of nanoscale MOS transistors," in *Proc. ESSDERC*, 2003, pp. 147–150.
[43] C. H. Choi, P. R. Chidambaram, R. Khamankar, C. F. Machala, Z. Yu, and R. W. Dutton, "Dopant profile and gate geometric effects on polysilicon gate depletion in scaled MOS," *IEEE Trans. Electron Devices*, vol. 49, no. 7, pp. 1227–1231, Jul. 2002.
[44] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Improved split C– V method for effective mobility extraction in sub-0.1- μm Si MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004.
[45] A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling—Part 1: Historical trends," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1391–1400, Jun. 2008.
[46] M. Fischetti, T. O'Regan, S. Narayanan, C. Sachs, S. Jin, J. Kim, and Y. Zhang, "Theoretical study of some physical aspects of electronic transport in nMOSFETs at the 10-nm gate-length," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2116–2136, Sep. 2007.
[47] D.-H. Kim and J. del Alamo, "30-nm InAs pseudomorphic HEMTs on an InP substrate with a current–gain cutoff frequency of 628 GHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 830–833, Aug. 2008.
[48] G. Dewey, M. Hudait, K. Lee, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau, "Carrier transport in high-mobility III–V quantum-well transistors and performance impact for high-speed low-power logic applications," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1094–1097, Oct. 2008.

Changwook Jeong (S'09) received the B.S. and M.S. degrees in material science and engineering from Seoul National University, Seoul, Korea, in 1999 and 2001, respectively. He is currently working toward the Ph.D. degree in electrical and computer engineering in the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN.

From 2003 to 2007, he worked at Samsung Electronics Co., Ltd., the development of non-volatile high density memories such as Magnetoresistive RAM and Phase-Change RAM. His current research interests include nanosacle device physics and devices for energy conversion.



Dimitri A. Antoniadis (M'79–SM'83–F'90) was born in Athens, Greece. He received the B.S. degree in physics from the National University of Athens in 1970 and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1976.

He has been with the Microsystems Technology Laboratories, Massachusetts Institute of Technology (MIT), Cambridge, since 1978, where he is the Ray and Maria Stata Chair in electrical engineering. He is the Director of the multiuniversity Focus Research Center for Materials Structures and Devices centered at MIT. He is the author or a coauthor of more than 200 technical papers. His current research interests include the physics and technology of extreme submicrometer Si, silicon-on-insulator, and Si/SiGe MOSFETs.

Dr. Antoniadis is a Member of the National Academy of Engineering. He is the recipient of several professional awards.

Mark S. Lundstrom (S'72–M'74–SM'80–F'94) received the B.E.E. and M.S.E.E. degrees from the University of Minnesota, Minneapolis, in 1973 and 1974, respectively, and the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 1980.

From 1974 to 1977, he was with the Hewlett-Packard Corporation, Loveland, CO, working on integrated circuit process development and manufacturing support. In 1980, he joined the School of Electrical Engineering, Purdue University, where he is currently the Don and Carol Scifres Distinguished Professor of electrical and computer engineering and the Founding Director of the Network for Computational Nanotechnology. He currently serves as the Chairman of the Executive Committee. From 1989 to 1993, he served as the Director of Purdue University's Optoelectronics Research Center and from 1991 to 1994 as an Assistant Dean of Engineering. He also serves on the Leadership Council of the Focus Center on Materials, Structures, and Devices. His current research interests include the physics of small electronic devices, particularly nanoscale transistors, carrier transport in semiconductor devices, and devices for energy conversion, storage, and conservation.

Prof. Lundstrom currently serves as an IEEE Electron Devices Society Distinguished Lecturer and is an elected member of the IEEE Electron Devices Society Administrative Council. He is a Fellow of the American Physical Society and the American Association for the Advancement of Science. Over the course of his career, he has received a number of awards for his contributions to research and education, including the IEEE Cledo Bruneti Award in 2002, and was the inaugural recipient of the IEEE Electron Devices Society Education Award in 2006. He is a Member of the U.S. National Academy of Engineering.