On the validity of the top of the barrier quantum transport model for ballistic nanowire MOSFETs

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On the validity of the top of the barrier quantum transport model for ballistic nanowire MOSFETs

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Abstract— This work focuses on the determination of the valid device domain for the use of the Top of the barrier (ToB) model to simulate quantum transport in nanowire MOSFETs in the ballistic regime. The presence of a proper Source/Drain barrier in the device is an important criterion for the applicability of the model. Long channel devices can be accurately modeled under low and high drain bias with DIBL adjustment.

Keywords-component; nanowires; top of the barrier; MOSFET; ballistic transport model; DIBL; tunneling current; top-of-the-barrier; subthreshold-slope; Tight-Binding; Short channel effects.

I. INTRODUCTION

Continuous shrinking of channel length (Lc) in silicon CMOS devices to increase performance has led to the development of non-planar devices. Nanowire based Field-Effect-Transistors (FET) are an attractive candidate in this area due to better electrostatic gate control. Recently many experimental groups have demonstrated fabrication of silicon nanowire (SiNW) transistors of diameters even down to 3nm [1, 2, 3, 4, 5].

To understand the working of such small devices it is important to have proper theoretical model which encapsulates quantum transport mechanisms. A critical element in the model is the representation of the device in an atomistic Tight-Binding (TB) model [6], which understands the finite number of atoms in the structure, their local arrangement with details such as strain distribution and disorder [7, 8]. A full 3D atomistic quantum transport model [9, 10, 11] can provide the device characteristics, however, this model is computationally time consuming [12]. Recently, a 2D top of the barrier (ToB) atomistic quantum transport model [13, 14, 15] has been used for speedy simulation and analysis of SiNW FET device characteristics, which provides significant insight. However, to use the ToB model reliably, it is essential to understand the device regime where this model is valid.

In this work, the range of validity of 2D Top of the barrier atomistic quantum transport model is evaluated with a full 3D and atomistic model. Figure 1 shows that ToB inherently misses the channel length dependence; however, it can fetch accurate and fast results for long channel ballistic transistors. We observe a deviation in ToB vs. full 3D results as channel length is reduced. This difference is mostly attributed to the source/drain tunnelling current due to shrinking of the barrier width. Finally we also provide a rule of thumb for the valid simulation domain for SiNW FET devices where ToB model can be used faithfully. We also provide a comparison of compute times for the full 3D and the 2D ToB model.

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II. APPROACH

Simulation Procedure: First a full 3D atomistic ballistic simulation [9, 10, 11, 16, 17, 18] is performed for gate-all-around (GAA) rectangular n-type SiNW FETs with a given cross-section width (W) and height (H), keeping W/H = 1, (Fig.2a) using OMEN [17, 18] for different gate lengths (Lc). The channel orientation is also specified for the FETs. 3D I_D-V_G simulations are done for low and high drain biases (V_DS). From these I_D-V_G curves DIBL is extracted. Using this DIBL value 2D I_D-V_G are simulated for exactly the same devices, using the ToB model to account for different 'channel lengths' (Fig. 2b).

Simulation environment and devices: Square silicon nanowire FETs with cross-section size of 3.1 nm (W) X 3.1 nm (H) and Tox of 2nm are simulated using the 3D model for two different drain biases of V_DS = 0.05V (low) and 0.6V (high). Different channel lengths of 4, 7, 10, and 15 nm have been simulated with [100] and [110] channel orientations. The source/drain extension is 10nm with 1e20cm^-3 n-type doping. Exactly the same device structures are then simulated using the 2D ToB model.

III. RESULTS & DISCUSSION

Source/Drain tunnelling current: Figure 1 shows that I_D-V_G from ToB is in good agreement with the 3D OMEN result at low V_DS without any DIBL compensation, for Lc = 10nm. The deviation at shorter Lc can only be attributed to S/D tunnelling current [19, 20] under ballistic condition, which is not included in the ToB model. Fig.3a and table I shows that the sub-threshold swing (SS) becomes considerably larger than 60mV/dec (ideal ToB result) with decreasing Lc for both [100] & [110] SiNW, reflecting strong S/D tunnelling current in the OFF-state. Also [110] wires show larger SS compared to [100] wires [19], hence making them more scalable. Thus, increased S/D tunnelling current causes 2D ToB to deviate from 3D I_D-V_G results for reduced Lc devices.

Source to channel barrier (φ_sc) : Figure 4. and insets of Fig.5 and Fig.6 show that the source to channel barrier reduces as V_GS increases. This decrease is stronger for smaller Lc devices (Fig.4). ToB shows a strong deviation from 3D I_D-V_G results since the source to channel barrier becomes much smaller than the KT/q limit and causes an excessive S/D tunnelling current to flow. Thus, existence of proper source to channel barrier is important for ToB to match 3D results.

Longer Lc devices: To obtain the device regime where ToB provides reliable results, it is important to understand the effect of gate and drain electrostatics on the source to channel barrier. Figure 5 shows that ToB provides good agreement to 3D results for Lc = 15nm (long channel) in the OFF-state since the S/D barrier is well defined at low V_GS & high V_DS and also the tunnelling current is minimal due to longer Lc. However, in the ON-state ToB current is smaller compared to 3D under high V_GS and V_DS. As V_GS increases, the S/D barrier decreases, as a result carriers injected at the source side are no more reflected by the barrier. To ensure charge neutrality in the source, the electrostatic potential on the source side (φ_sc) decreases allowing more carrier injection causing an artificial increase in the ON-current. This is an artifact of the ballistic approximation that is not captured in ToB model and explains why the full 3D OMEN ON-current is larger at high V_GS (Fig.5 & 6).

Shorter Lc devices: As Lc decreases the drain bias starts to reduce the S/D barrier width (DIBT*) [20] (Fig.6 inset) causing...
excessive S/D tunnelling current to flow. For \( L_c = 4 \text{nm} \) (short channel), ToB results are not in good agreement with full 3D OMEN anywhere (Fig.5) since the S/D barrier is not well defined and is below the thermal KT/q limit (Fig.4). Absence of a clear S/D barrier makes ToB inapplicable to short \( L_c \) devices. As a quantitative estimate for tunnelling current rate (\( R_{\text{TUN}} \)) (in the OFF-state) eqn. 1 is used:

\[
R_{\text{TUN}} = 100 \times \frac{J_{\text{3D}} - J_{\text{TOB}}}{J_{\text{3D}}} \quad ---- \quad (1)
\]

where, \( J_{\text{3D}}, J_{\text{TOB}} \) are currents from 3D and ToB simulations, respectively. Figure 7 shows that at \( I_{\text{OFF}} \), tunnelling rate (\( R_{\text{TUN}} \)) increases dramatically with decreasing \( L_c \), with [110] devices showing worse short channel effects (SCE) compared to [100] devices [19].

\[\lambda = \frac{C_{\text{3D}}}{C_{\text{2D}}} \quad ---- \quad (3)\]

\[\lambda \approx 51\]

\[n_{\text{3D}} \approx 5.63\text{ (lin. fit)}\]

\[n_{\text{2D}} \approx 2.82\text{ (lin. fit)}\]
simulation. Also the memory storage needed for ToB device simulation is much smaller compared to 3D simulation.

IV. CONCLUSION & OUTLOOK

Two factors are important in defining the valid device regime for ToB, (a) the presence of proper source to channel barrier ($\phi_{sc} > KT/q$) and (b) a small source to drain tunneling current. Due to these reasons ToB compares well with 3D model for longer Lc devices. We find that for a ratio of Lc/W >= 5, that the ToB model can be used to obtain accurate 3D results. ToB is a suitable model for SiNW FETs where channel electrostatics is controlled mostly by the gate. In this regime, DIBL from experiments can be fed to ToB, to obtain accurate terminal characteristics. Computational speedup (Table II) as well as smaller memory storage requirements makes ToB a very attractive model for typical device simulation. The ToB model provides significant insight into the importance of atomistic bandstructure effects in nanowires [13,14]. [100] and [110] wire orientations show similar short channel effects (SCE) at sufficiently long channel lengths. Table I elucidates the SCE and the regimes where the ToB model is applicable. It is shown that [100] n-type SiNW FETs are more scalable compared to [110] wires (Table I). The full 3D OMEM transport model is now deployed on nanoHUB.org [18] and readers can duplicate our simulation results for small diameter silicon nanowire FETs. The ToB model used in this work is also released as a part of the existing Bandstructure Lab [21] on nanoHUB.org.

ACKNOWLEDGMENT

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REFERENCES


TABLE II. COMPARISON OF ACTUAL SIMULATION TIME FOR FULL 3D AND 2D MODEL WITH SPEED-UP ACHIEVED FROM 2D TOB MODEL FOR DIFFERENT CROSS-SECTION WIDTH (W) SiNW FETS WITH 1NM GAA OXIDE.

<table>
<thead>
<tr>
<th>W(width) [nm]</th>
<th>time[sec] (1 CPU)</th>
<th>Speed up ($\lambda \sim 51$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>103</td>
<td>66.65</td>
</tr>
<tr>
<td>2.1</td>
<td>4,080</td>
<td>410.13</td>
</tr>
<tr>
<td>3.1</td>
<td>35,200</td>
<td>1225.2</td>
</tr>
<tr>
<td>4.1</td>
<td>205,000</td>
<td>2688</td>
</tr>
</tbody>
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