

11-2009

Reconfigurable CMOS Tuners for Software-Defined Radio

Laleh Rabieirad

Purdue University - Main Campus

Saeed Mohammadi

School of Electrical and Computer Engineering, Purdue University, saeedm@purdue.edu

Follow this and additional works at: <http://docs.lib.purdue.edu/nanopub>



Part of the [Nanoscience and Nanotechnology Commons](#)

Rabieirad, Laleh and Mohammadi, Saeed, "Reconfigurable CMOS Tuners for Software-Defined Radio" (2009). *Birck and NCN Publications*. Paper 490.

<http://docs.lib.purdue.edu/nanopub/490>

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Reconfigurable CMOS Tuners for Software-Defined Radio

Laleh Rabieirad, *Member, IEEE*, and Saeed Mohammadi, *Senior Member, IEEE*

Abstract—A reconfigurable tuner is demonstrated by using a low-loss shielded coplanar waveguide transmission line periodically loaded with CMOS transistor switches in series with capacitors. The switch–capacitor combination is used to change the local impedance of the transmission line in a binary fashion. It achieves a higher capacitance ratio (by 60%), less transmission loss (by 40%), higher quality factor (by 100%), and subsequently wider bandwidth and better Smith impedance chart coverage compared to optimized CMOS varactors realized in the same technology. The 5–16-GHz tuner demonstrated here is implemented in a standard 0.13- μm CMOS technology and can be configured to 2^{20} different impedances through an integrated 20-bit shift register.

Index Terms—Matching network, programmable transceiver, reconfigurable circuit, software-defined radio, switch, tuner, varactor.

I. INTRODUCTION

TRANSCEIVERS of multistandard wireless communication systems need to instantaneously adapt to signals in different frequency bands with different bandwidths and modulation schemes. A number of switchable transceivers can be grouped together in a single wireless terminal to achieve a multistandard system at the cost of a complex power-hungry hardware that still needs to be revised for future wireless standards. On the other hand, a software-programmable and network-independent transceiver can be utilized to detect and decode signals from a wide range of modulation schemes, modes of operations, and frequency bands. Reconfigurable input and output matching networks can be used to implement such programmable transceivers. A reconfigurable tuner placed at the input of a low-noise amplifier can improve its noise figure, gain, or linearity by adjusting to the optimum matching impedance as frequency is varied [1], [2]. Both input and output tuners of a power amplifier can be tuned to their optimum impedance values to improve power gain, efficiency, or linearity as the frequency band, modulation scheme, or power level is varied [3]–[5]. Matching networks between the antenna and RF front-end can improve the power efficiency, linearity, as well as the input power level to the amplifier [6], [7].

Manuscript received February 02, 2009; revised July 30, 2009. First published October 20, 2009; current version published November 11, 2009. This work was supported by the National Science Foundation under Project ECCS 0802178.

The authors are with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: laleh@caltech.edu; saeedm@purdue.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TMTT.2009.2032464

Reconfigurable matching networks based on microelectromechanical systems (MEMS) have been previously reported [8]–[10]. Although MEMS devices provide high quality factors, high linearity, and extremely low loss, they cannot be easily integrated with a standard CMOS or BiCMOS processes, resulting in a high implementation cost. Additionally, MEMS devices require special packaging technology to achieve high reliability and cannot operate under extreme environments. Another approach to achieve high performance tunable matching networks is to use varactors as impedance tuning elements. Adaptive matching network based on high quality factor barium–strontium–titanate (BST) varactors [6], silicon-on-glass varactors [11], and GaAs varactors [12]–[14] have been reported. Although these varactor technologies provide low loss and good linearity performance, they cannot be integrated with a standard CMOS technology.

With continuous scaling of nanoscale CMOS technology with transistor cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) exceeding the 100-GHz mark [15], low quality factor and mediocre linearity of MOS varactors, and low quality factors of capacitors, spiral inductors, and transmission lines impede the implementation of high-performance CMOS reconfigurable circuits [16]–[18]. While shielding of inductors and transmission lines from the lossy Si substrate has improved their losses [19], [20], further process and layout optimizations are needed to improve the performance of varactors (both quality factor and linearity), inductors (quality factor), and transmission lines (loss). Loss of transmission lines and inductors can be minimized by utilizing a CMOS silicon-on-insulator (SOI) technology with a thick top metal interconnect on a high-resistivity Si substrate.

A reconfigurable matching network operating at frequencies below 1 GHz based on CMOS switched capacitors has been recently reported [21]. Additionally, a 4–11-GHz fully programmable tuner based on an array of CMOS varactors periodically loading a low-loss transmission line is demonstrated by the authors [22]. In this paper, using standard 0.13- μm transistor switches and vertical parallel-plate capacitors, a 5–16-GHz reconfigurable CMOS tuner with lower loss and larger Smith chart coverage compared to that reported in [22] is implemented.

II. TUNER BUILDING BLOCKS

A programmable CMOS tuner is formed by connecting a series of variable impedance elements such as varactors or switches through a network of distributed transmission lines.

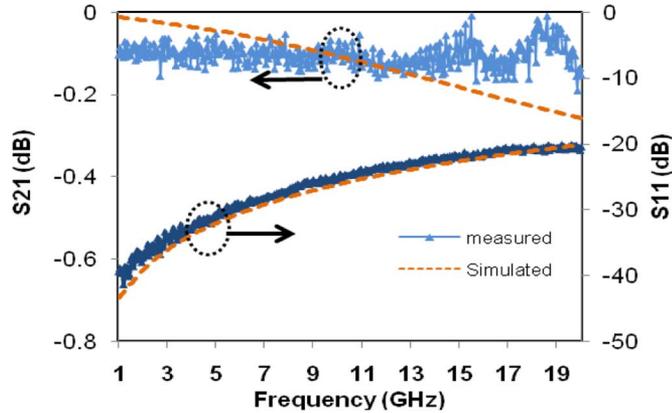


Fig. 1. Measured and simulated S -parameters of 0.5-mm-long shielded CPW line ($W = 10 \mu\text{m}$, $G = 23 \mu\text{m}$, shielding parameters: $d = 1 \mu\text{m}$, $g = 1 \mu\text{m}$).

A. Transmission Line Design

Standard transmission lines in CMOS technology suffer from high dielectric loss of low-resistivity Si substrate at high frequencies. To reduce the loss, and thus, achieve better tuner Smith chart coverage, an array of floating narrow metal strips shielding the electromagnetic field from penetrating into the lossy Si substrate is placed under the transmission line. The loss reduction is accompanied by wavelength reduction effect (slow-wave phenomena), which results in shorter physical lengths of transmission line elements [20]. In the 0.13- μm CMOS process used in this study, floating metal strips with 1- μm width and a 1- μm gap optimized by Ansoft's High Frequency Structure Simulator (HFSS) result in loss reduction as much as 70% at 20 GHz in a 0.5-mm-long shielded coplanar waveguide (CPW) transmission line. Fig. 1 shows the simulated and measured S -parameters of a 0.5-mm-long shielded CPW line. The wavelength reduction effect for the geometries used in this study shortens the length of each transmission line element by 6%. Shorter transmission lines translate into further loss reduction (by around 6% in decibels) and smaller chip area (by 6%–12%) compared to standard transmission line implementation on the CMOS substrate. The shielded line is fabricated in 0.13- μm CMOS technology with 1- Ωcm resistivity Si substrate and sits on top of a 5- μm silicon dioxide layer. The top of the transmission line is covered with a 5- μm polyimide passivation layer. The shielding metal strips use the lowest level of back end of line metallization between the silicon dioxide and Si.

B. Transistor Switches

NMOS transistors in 0.13- μm CMOS technology are used in this study as series switches and are optimized for their geometry to provide both low insertion loss in the on state and high isolation in the off states. 20-finger transistors with $W = 50 \mu\text{m}$ and $L = 0.13 \mu\text{m}$ show on-state insertion loss below 2.5 dB and isolation above 15 dB for frequencies up to 15 GHz and are used as switch elements throughout this study.

C. NMOS Varactors

As demonstrated in [22] and [23], varactors can be used in an impedance tuner structure. NMOS varactor optimization is de-

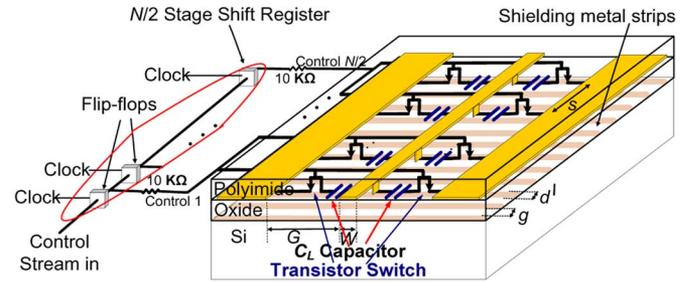


Fig. 2. Structure of the CMOS tuner based on switch-capacitors ($N = 40$, $s = 40 \mu\text{m}$, $W = 10 \mu\text{m}$, $G = 23 \mu\text{m}$, shielding parameters: $d = 1 \mu\text{m}$, $g = 1 \mu\text{m}$). Top metal is used for CPW line and the lowest metal level is used for shielding.

scribed in [24]. Optimization is performed using Cadence Virtuoso Spectre Circuit Simulator in order to get both high-capacitance ratio and high quality factor for tuner operation around 10 GHz. The optimized varactors are 2×1 array of 30 finger varactors with an overall size of $W = 30 \mu\text{m}$ and $L = 240 \text{ nm}$ and create the maximum and minimum capacitances of 110 and 50 fF, respectively.

III. TUNER TOPOLOGIES

A programmable CMOS tuner with varactors as variable impedance elements periodically loading a through transmission line has been previously reported by the authors [22]. Programming each of the varactor pairs to their minimum and maximum capacitance dynamically changes the characteristic impedance of the short length of the through transmission line around that pair and creates one of the 2^{22} impedance matching points. Structural symmetry in the design of the periodically loaded line forces most of these matching points to fall on each other on the Smith chart, but the parasitic asymmetry caused by the transmission line loss and the finite Q of varactors causes the impedance points to diverge from each other. The tuner achieves a 4–11-GHz bandwidth with modest Smith chart coverage [22].

In this paper, we first implemented a 2^{20} programmable impedance points varactor tuner based on [22] using the optimized 50-fF/110-fF varactors, which showed similar Smith chart coverage to [22]. We then replaced the varactor with a transistor switch in series with a capacitor C_L to obtain a new programmable tuner, as shown in Fig. 2. Similar to the previous configuration, a shielded transmission line is employed. A 10-k Ω series resistor connected to each gate control line eliminates the RF signal leak through the control line. The switch-capacitor pair creates a dual-state variable capacitor with both a high quality factor and high capacitance ratio. The structure is designed symmetrically with each node of the signal line connected to the ground plane through a switch-capacitor pair so that slot mode of the transmission line is not excited [25], [26].

In order to understand the performance of switch-capacitor tuner design and compare it with the varactor-based tuner design, let us contrast the performance of the CMOS varactors with that of the switch-capacitor pairs. The CMOS varactor is

a tunable thick oxide N -type field-effect transistor (NFET) capacitor in an N -well with $N+$ source and drain regions shorted together while body contact is floating. The variable capacitance is achieved by controlling the two junction capacitances through applying a gate bias to charge or discharge the channel from depletion to accumulation. When the channel is in accumulation mode, the capacitance between terminals is approximately the gate–oxide capacitance of WLC_{OX} , where C_{OX} is the thick gate–oxide capacitance density. On the other hand, in the depleted channel, the gate oxide is in series with the junction capacitances between bulk and shorted source and drain terminals. The two junction capacitance values are related to the control bias voltage according to the following equations [27]:

$$C_J = \frac{C_{JO}}{\left(1 + \frac{v_R}{\phi_j}\right) M_J} \quad (1)$$

$$C_{JSW} = \frac{C_{JSWO}}{\left(1 + \frac{v_R}{\phi_j}\right) M_{JSW}} \quad (2)$$

where C_J is the bottom junction capacitance per unit area, C_{JSW} is the sidewall junction capacitance per unit length, v_R is the reversed-bias voltage across the pn junction, ϕ_j is the built-in-potential, and M_J and M_{JSW} are grading parameters. For simplicity, assume that the grading parameters M_J and M_{JSW} are the same (M). The capacitance ratio of the varactors can be found according to the following equation:

$$\begin{aligned} \frac{C_{\max}}{C_{\min}} &= \frac{C_{OX}WL}{C_{OX}WL \left| 2(C_J A + C_{JSW} P) \right|} \\ &= 1 + \frac{C_{OX}WL}{2(C_{JO} A + C_{JSW_0} P)} \left(1 + \frac{v_R}{\phi_j}\right)^M \end{aligned} \quad (3)$$

where A and P are the source or drain area and perimeter, respectively. The contribution of the junction capacitance is doubled because source and drain terminals are shorted together. By substituting the parameters of 0.13- μm CMOS technology into (3), a maximum available capacitance ratio of 2.7 is achieved. The optimized CMOS varactors implemented in this technology with a minimum capacitance of 50 fF and a maximum capacitance of 110 fF achieves a capacitance ratio of ~ 2.2 , which is slightly smaller than the theoretical value of 2.7 calculated from (3). On the other hand, a switch in series with a capacitor C_L is another two-state variable capacitance. A high (low) bias voltage applied to the gate control line turns the switch transistor on (off) and sets the capacitance of this configuration to $C_{\max}(C_{\min})$. When the gate control voltage is low (switch off), C_L is essentially in series with the equivalent capacitance between drain and source of the transistor C_{ds}

$$C_{\min} = \frac{C_L C_{ds}}{C_L + C_{ds}} \quad (4)$$

On the other hand, when the transistor is on, it is modeled with a small equivalent resistor between source and drain R_{on} in series with C_L . The maximum capacitance of the switch–capacitor combination assuming small R_{on} is given by the following equation:

$$C_{\max} = C_L \quad (5)$$

The capacitance ratio of the switch–capacitor combination is given by

$$\frac{C_{\max}}{C_{\min}} = 1 + \frac{C_L}{C_{ds}} \quad (6)$$

For a capacitance ratio larger than that of the varactors, (~ 2.7) C_L should be larger than $1.7 C_{ds}$, which is easily achievable through using a large C_L .

In addition to a large capacitance ratio, an impedance tuner requires high quality factor programmable elements in order to have large Smith chart coverage. The quality factor of the capacitors in both on and off states can be calculated from the following equations:

$$Q_{C \min} \sim \frac{1}{C_{ds} \omega R_s} \quad (7)$$

$$Q_{C \max} = \frac{1}{C_L \omega R_{on}} \quad (8)$$

where $Q_{C \min}$ and $Q_{C \max}$ are the quality factors of switch–capacitor combination in minimum and maximum capacitance states, respectively, ω is the frequency in rad/s, R_s is a small (fraction of Ω) series parasitic resistor, and R_{on} is the series resistance of the switch in the on state. To achieve small R_{on} , a large-size switch is desirable, as R_{on} has an inverse relationship with the switch width W . On the other hand, the off-state capacitance (C_{ds}) is directly proportional to the width W of the switch transistor. Therefore, the larger the transistor width (W), the larger the on-state quality factor is, but also the larger C_{ds} and the smaller the capacitance ratio is. The tradeoff between the capacitance ratio and quality factor of the switch–capacitor combination in the on state is addressed by carefully optimizing the transistor dimensions using the Cadence Virtuoso Spectre Circuit Simulator to $W \times L = 50 \mu\text{m} \times 130 \text{ nm}$. As the quality factor depends not only on the resistance, but also on the value of the capacitance, the value of C_L in the switch–capacitor structure is chosen to be equal to the maximum capacitance of the varactor (110 fF) for a fair comparison between the two tuner structures.

Individual cells of varactor and switch–capacitor structures are separately fabricated in a standard 0.13- μm CMOS process and tested when biased for their maximum and minimum capacitances (C_{\max} and C_{\min}) using on-wafer S -parameter measurements. The effect of RF pads and interconnects leading to these structures are removed using an open and through deembedding technique described in [28]. Fig. 3 compares the measured capacitance value and capacitance ratio of the switch–capacitor pair and varactor. With similar C_{\max} for both structures, the switch–capacitor combination offers 1.5 times higher capacitance ratio compared to that of the CMOS varactor because of its lower C_{\min} value. Fig. 4 shows the measured quality factor of varactors and switch–capacitor combination versus frequency in both minimum and maximum capacitance states. It should be noted that because of relatively low quality factor of integrated capacitors, the quality factor of the switch–capacitor pair even in the off state is not high, but it is still higher than that of the varactor in both on and off states. As demonstrated in the following, higher capacitance ratio and quality factors translate into larger Smith chart coverage in the switch–capacitor tuner compared to

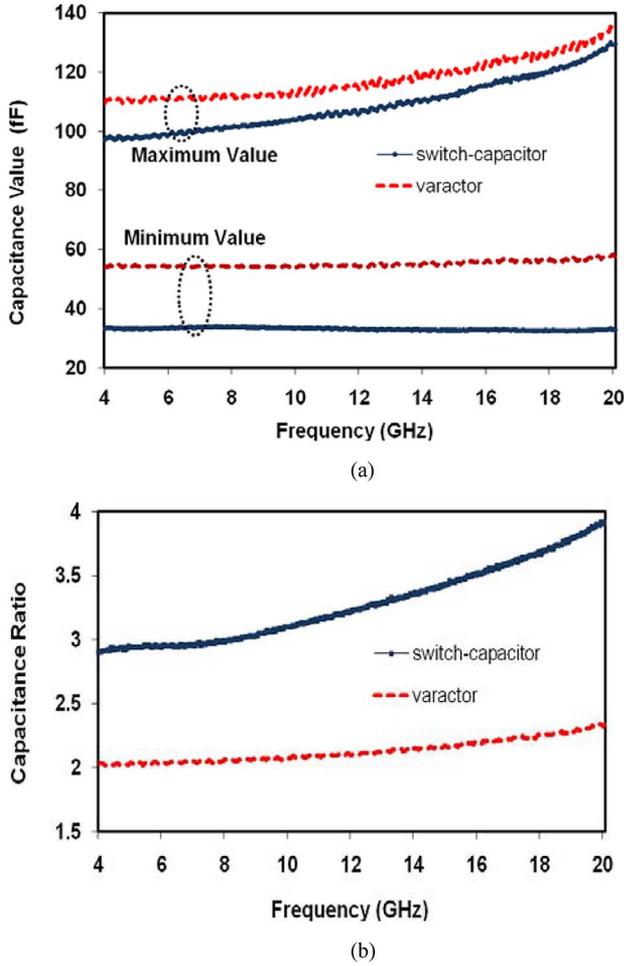


Fig. 3. Comparison between a CMOS varactor and a switch–capacitor pair. (a) Measured capacitance values. (b) Measured capacitance ratio.

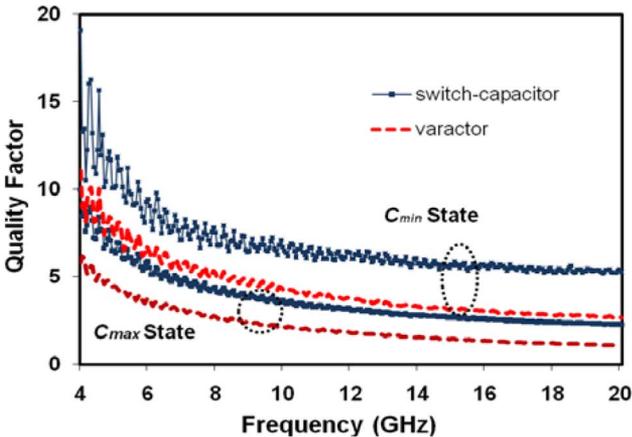


Fig. 4. Measured quality factor of switch–capacitor compared to varactor in maximum and minimum capacitance values (varactor size: $W = 30 \mu\text{m}$, $L = 240 \text{ nm}$ and $nf = 30$, $C_{\text{min}} = 50 \text{ fF}$, $C_{\text{max}} = 110 \text{ fF}$; transistor switches: $W = 50 \mu\text{m}$, $L = 0.13 \mu\text{m}$, and $nf = 20$; $CL = 110 \text{ fF}$; all in $0.13\text{-}\mu\text{m}$ CMOS technology).

the programmable tuner implemented based on the varactors introduced in [22].

The optimized switch–capacitor devices are distributed uniformly along a shielded coplanar transmission line with close

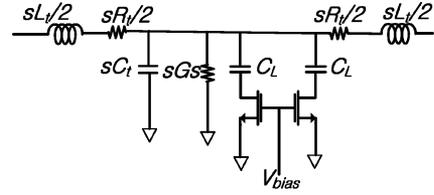


Fig. 5. Lumped-element model of loaded transmission line. For the coplanar transmission line with $W = 10 \mu\text{m}$, $G = 23 \mu\text{m}$, the value of the model parameters are $L_t = 750 \text{ nH/m}$, $C_t = 375 \text{ pF/m}$, $R_t = 250 \Omega/\text{m}$, $G_s = 1.25 \Omega^{-1}/\text{m}$; transistor size is $W = 50 \mu\text{m}$, and $L = 0.13 \mu\text{m}$; CL is 110 fF and length of line of 1.6 mm .

distance of $40 \mu\text{m}$ from each other. The short transmission line segment between two adjacent devices can be modeled by a set of lumped elements and a pair of switch–capacitors added to each segment, as shown in Fig. 5. The circuit model for the complete tuner is obtained by cascading these segments in Agilent’s Advanced Design System (ADS) design environment. The tuner is simulated and optimized for $N = 40$ switch–capacitor pairs placed uniformly across a 1.6-mm -long low-loss transmission line. The characteristic impedance of the unloaded line is optimized to 63Ω through adjusting the signal metal width to $W = 10 \mu\text{m}$, signal to ground gap to $G = 23 \mu\text{m}$, shielding metal strip width to $d = 1 \mu\text{m}$, and metal strip gap to $g = 1 \mu\text{m}$ (Fig. 2). Larger gaps and narrower signal width would result in higher characteristic impedances, but would cause significant attenuation of the coplanar mode. The switch–capacitor pair loads the short transmission line segment around it resulting in lowered characteristic impedances from the unloaded value of 63Ω to either Z_{min} or Z_{max} according to

$$Z_{\text{min}} = \sqrt{\frac{sL_t}{C_{\text{max}} + sC_t}} \quad (9)$$

$$Z_{\text{max}} = \sqrt{\frac{sL_t}{C_{\text{min}} + sC_t}} \quad (10)$$

where $Z_{\text{min}}(Z_{\text{max}})$ is the characteristic impedance of the short segment when the switch is on (off) and s is the length of the short segment shown in Fig. 2. By substituting the parameters of the programmable tuner designed in this study, loaded characteristic impedances of $Z_{\text{min}} = 7.6 \Omega$ and $Z_{\text{max}} = 11.73 \Omega$ are achieved.

To reduce the number of control lines, every two switch pairs are connected to the same control line with an insignificant effect on the Smith chart coverage confirmed through simulation. A 20-bit serial in–parallel out shift register integrated along the tuner programs 2^{20} possible impedance matching points. The desired combination of control voltages is programmed into the shift register through the serial-in and clock inputs.

Fig. 6(a) shows the Smith chart coverage of the tuner at 10 GHz for $50\text{-}\Omega$ termination. The coverage is better than what have been achieved for the varactor tuner [see Fig. 6(b)]. Additionally, the tuner with switch–capacitors while comparable in size with the varactor tuner has a $5\text{--}16\text{-GHz}$ bandwidth, which is a factor of 1.5 better than the varactor tuner; bandwidth is defined as frequency limits where the covered Smith chart area is half of the maximum area covered. At frequencies below 5 GHz , the capacitance values are too small to load the line,

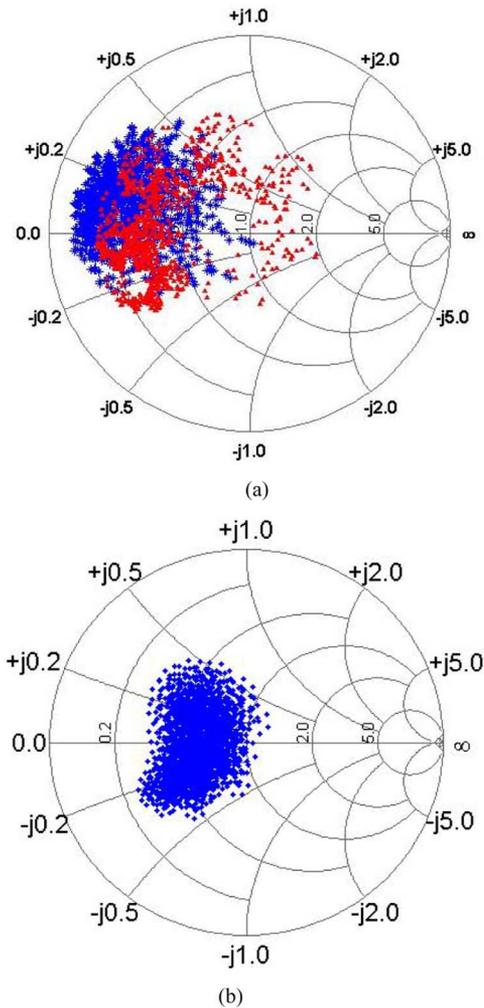


Fig. 6. (a) Smith chart coverage of switch-capacitor tuner with $50\text{-}\Omega$ termination at 10 GHz . Comparison between a tuner with $C_L = 110\text{ fF}$, 20 programmable control lines, and transmission line length of 1.6 mm (blue asterisks in online version) and a tuner with $C_L = 440\text{ fF}$, ten programmable control lines, and line length of 3.6 mm (red triangles in online version). Both tuners use transistor switches with $W_{trans} = 50\text{ }\mu\text{m}$ and are optimized for maximum Smith chart coverage at 10 GHz . (b) Smith chart coverage of equivalent varactor tuner with $50\text{-}\Omega$ load.

resulting in a very small coverage of the Smith chart. On the other hand, at frequencies above 16 GHz , tuner loss reduces the Smith chart coverage.

As the low quality factor of the switch-capacitors is one major drawback of this structure, reducing their number would reduce the losses with the expense of lower degree of programmability and lower capacitance values, but unlike varactors, in this structure, the minimum and maximum capacitance values can be adjusted independently to keep the bandwidth constant. Fig. 6 compares the Smith chart coverage of two tuners with 10 and 40 switch-capacitor pairs, one with $C_L = 440\text{ fF}$ and the other with $C_L = 110\text{ fF}$, resulting in capacitance ratios of 12.5 and 3.1 , respectively. The Smith chart coverage of the tuner with larger C_L is broader despite a longer length (3.6 mm , as opposed to 1.6 mm) and a lesser number of programmable elements. Reducing the number of programmable elements much further requires even larger

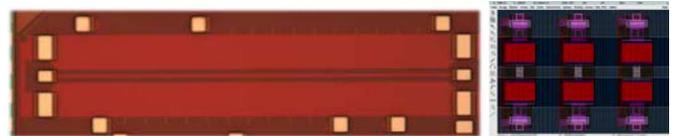


Fig. 7. Micrograph of the tuner with the switch-capacitor $C_L = 110\text{ fF}$ and 2^{20} number of impedance points with enlarged layout of loading switch-capacitor pairs. The inset shows the layout of transistor capacitor combination.

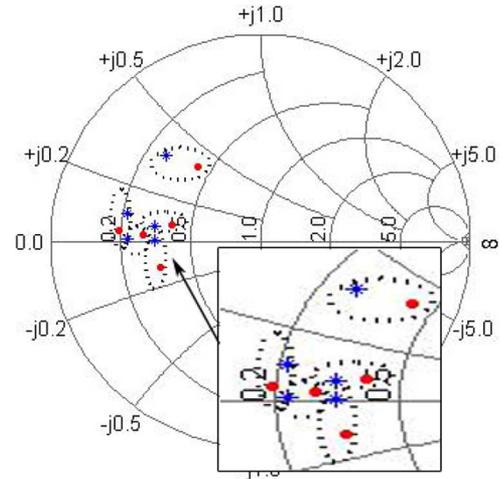


Fig. 8. Input impedance of the switch-capacitor tuner based on simulation and measurement for five different control configurations at $f = 13\text{ GHz}$. Output of the shift register attached to the control lines ($1 = 2\text{ V}$ and $0 = 0\text{ V}$) are a:11111111111111111111, b:11111111110000000000, c:00000000000000000000, d:00000000110000000011, e:11111100001111000011. Corresponding measurement (blue asterisks in online version) and simulation (red dots in online version) data are enclosed in the same circle.

capacitances with lower quality factors and larger area, which would increase the total loss again. It should be noted that if a CMOS SOI process is utilized, larger size transistors with smaller on-state insertion loss and higher off-state isolation can be implemented. This will result in an overall better performance of the programmable tuner in a CMOS SOI technology compared to a similar bulk CMOS process.

IV. MEASUREMENT

The switch-capacitor tuner with $C_L = 110\text{ fF}$ and 2^{20} programmable impedance points is implemented in a standard $0.13\text{-}\mu\text{m}$ CMOS technology with chip dimensions of $0.5\text{ mm} \times 1.8\text{ mm}$ (Fig. 7). A similar tuner based on ($110\text{ fF}/50\text{ fF}$) varactors and the structure reported in [22] was also implemented. To compare the switch-capacitor and varactor tuners, the following measurements are performed.

A. *S*-Parameter

On-wafer two-port *S*-parameter measurement is carried out using an Agilent 8722 Vector Network Analyzer. Calibration is done using a short-open-load-thru (SOLT) standard substrate. Due to a large degree of tuner programmability (2^{20}), only a few impedance points are measured. Fig. 8 compares the simulated and measured input impedance of the switch-capacitor tuner at five different control lines with $50\text{-}\Omega$ termination. A good match between the simulated and measured results indicates a reliable

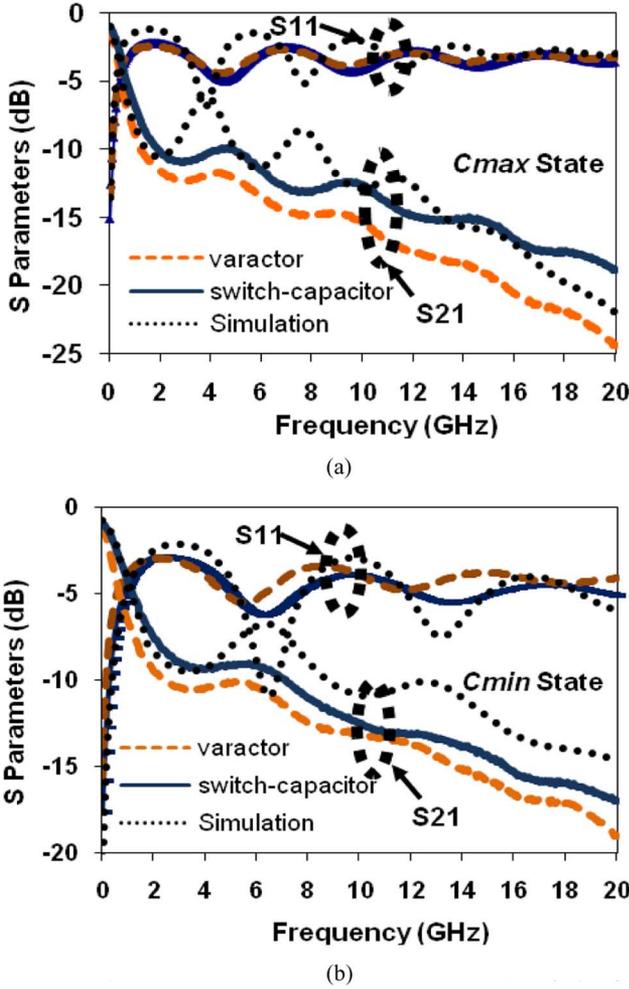


Fig. 9. Measured S -parameters of the tuners with varactors (110 fF/50 fF) or switch-capacitors ($C_L = 110$ fF) along with the simulated S -parameters of the switch-capacitor tuner. (a) All segments are at C_{max} state. (b) All segments are at C_{min} state.

simulation model used in creating the Smith chart coverage plots of Fig. 6. The Smith chart coverage using integrated CMOS components is about half of what can be achieved using high quality factor MEMS devices [8].

Measured S -parameters of the two tuners for two bias streams coinciding with minimum and maximum capacitance as a function of frequency are shown in Fig. 9. Both circuits are fabricated on the same $0.13\text{-}\mu\text{m}$ CMOS technology. Since the quality factor in the C_{max} state is lower than the C_{min} state (due to an additional resistance of the on-state switch transistor R_{on} or on-state channel in the varactor), the loss of both tuners with segments tuned to the C_{max} state is higher than tuners with segments tuned to the C_{min} state. The tuner with switch-capacitors not only achieves a 45%–60% higher capacitance ratio than the one with varactors, it also presents between 1–5-dB less loss in the frequency range of 5–11 GHz (common bandwidth of the two tuners).

B. Linearity

The linearity of the two tuners with varactors and switch-capacitors is measured using a single tone technique with a signal

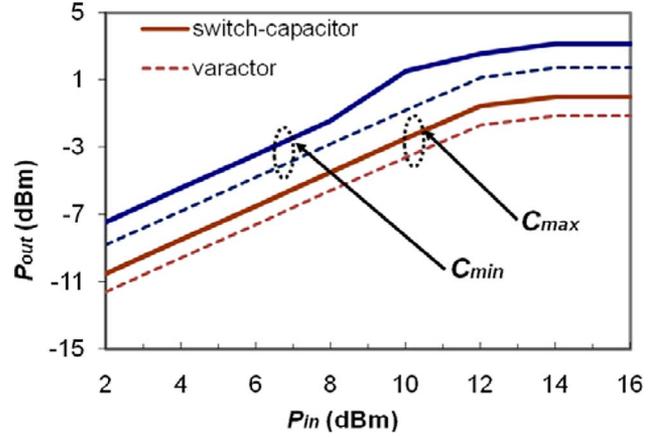


Fig. 10. Measured linearity at $f = 6.5$ GHz, C_{min} : All bias voltages are 0 V, C_{max} , and all bias voltages are 2 V. Varactors: 110 fF/50 fF, $C_L = 110$ fF, transistor switch $W = 50\ \mu\text{m}$. The two tuners have 220 impedance points on 1.6-mm shielded coplanar transmission lines. Signal line has dc voltage of 1 V.

source and a spectrum analyzer. Fig. 10 shows the output power of the tuners with respect to the input power at 6.5 GHz. For the switch-capacitor tuner, the 1-dB compression point for the C_{max} state is at $P_{out-1\text{ dB}} = -1$ dBm, while it is at $P_{out-1\text{ dB}} = 2.15$ dBm for the C_{min} state. On the other hand the varactor tuner has a lower 1-dB compression point for both states with a 1-dB compression point for the C_{max} state at $P_{out-1\text{ dB}} = -2.13$ dBm and at $P_{out-1\text{ dB}} = 0.72$ dBm for the C_{min} state. These measurement results show that the switch-capacitor tuner has better linearity performance than the varactor tuner. Although the linearity improvement in the switch-capacitor tuner is expected to be higher due to better linearity characteristic of the transistor switch compared to the CMOS varactor, large variation of the voltage on the signal line changes the operation mode of the switch transistor and results in excess nonlinearity under high input powers.

V. SUMMARY

CMOS transistor switches in series with capacitors are used as variable capacitance elements along a low-loss shielded transmission line to achieve a 5–16-GHz programmable tuner. The tuner is programmed to one of its 2^{20} programmable impedance points through an integrated 20-bit series-in parallel-out shift register designed along the tuner. Switch-capacitor combination used in this study has 1.5 times the capacitance ratio and up to two times the quality factor of optimized varactors in the same CMOS technology in both low- and high-capacitance states. As a result, the switch-capacitor tuner has larger bandwidth (5–16 GHz compared to 4–11 GHz for a varactor tuner), lower loss (1–5 dB lower loss in the common bandwidth of 5–11 GHz), and better linearity characteristics (higher output 1-dB compression point) compared to the CMOS varactor tuner implemented based on the design in [22]. Despite all these improvements in the switch-capacitor tuner, the high loss of the tuner impedes its application in high-performance programmable RF and microwave circuits. To partially address this problem, a CMOS SOI technology with a high-resistivity Si substrate can be utilized to improve the loss of the distributed transmission lines, as well as the performance of the switches.

As for the loss contribution of switch–capacitors or varactors to the overall circuit performance, we have shown that the possible solution is to reduce the number of programmable elements to eight to ten elements (256–1024 points on the Smith chart) to achieve lower overall loss, and thus, wider Smith chart coverage.

REFERENCES

- [1] K. F. Warnick and M. A. Jensen, "Optimal noise matching for mutually coupled arrays," *IEEE Trans. Antennas Propag.*, vol. 55, no. 6, pp. 1726–1731, Jun. 2007.
- [2] H. Kanaya, T. Nakamura, K. Kawakami, and K. Yoshida, "Design of coplanar waveguide matching circuit for RF-CMOS front-end," *Electron. Commun. Jpn.*, vol. 88, no. 7, pt. 2, pp. 19–26, 2005.
- [3] H. Zhang, H. Gao, and G.-P. Li, "Broad-band power amplifier with a novel tunable output matching network," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 11, pp. 3606–3614, Nov. 2005.
- [4] R. Negra, A. Sadeve, S. Bensmida, and F. M. Ghannouchi, "Concurrent dual-band class-F load coupling network for applications at 1.7 and 2.14 GHz," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 3, pp. 259–263, Mar. 2008.
- [5] T. Vähä-Heikkilä and G. M. Rebeiz, "A 4–18-GHz reconfigurable RF MEMS matching network for power amplifier applications," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 4, no. 4, pp. 356–372, Jun. 2004.
- [6] M. Schmidt, E. Lourandakis, A. Leidl, S. Seitz, and R. Weigel, "A comparison of tunable ferroelectric II- and T-matching networks," in *Eur. Microw. Conf.*, Oct. 2007, pp. 98–101.
- [7] K. R. Boyle, Y. Yuan, and L. P. Ligthart, "Analysis of mobile phone antenna impedance variations with user proximity," *IEEE Trans. Antennas Propag.*, vol. 55, no. 2, pp. 364–372, Feb. 2007.
- [8] Q. Shen and S. Barker, "Distributed MEMS tunable matching network using minimal-contact RF-MEMS varactors," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, pp. 2646–2658, Jun. 2006.
- [9] T. Vähä-Heikkilä, J. Varis, J. Tuovinen, and G. M. Rebeiz, "A reconfigurable 6–20 GHz RFMEMS impedance tuner," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2004, vol. 2, pp. 729–732.
- [10] Y. Lu, D. Peroulis, S. Mohammadi, and L. P. B. Katehi, "A MEMS reconfigurable matching network for a class AB amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 437–439, Oct. 2003.
- [11] K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X. Liu, and L. K. Nanver, "Low-distortion, low-loss varactor-based adaptive matching networks, implemented in a silicon-on-glass technology," in *IEEE Radio Freq. Integr. Circuits Symp.*, Long Beach, CA, Jun. 2005, pp. 117–120.
- [12] F. Ellinger, R. Vogt, and W. Bachtold, "Ultra compact, low loss, varactor tuned phase shifter MMIC at C-band," *IEEE Microw. Wireless Compon. Lett.*, vol. 11, no. 3, pp. 104–105, Mar. 2001.
- [13] I. J. Bahl and E. L. Griffin, "Low loss electronically tunable bandpass filters on the GaAs substrate," *Microw. Opt. Technol. Lett.*, vol. 5, no. 7, pp. 328–330, Jan. 2007.
- [14] M. G. Mcdermott, C. N. Sweeny, M. Benedek, J. J. Borell, G. Dawe, and L. Raffaell, "Integration of high-Q GaAs varactor diodes and 0.25 μm GaAs MESFET's for multifunction millimeter-wave monolithic circuit applications," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 9, pp. 1183–1190, Sep. 1990.
- [15] J. C. Guo, C. H. Huang, K. T. Chan, W. Y. Lien, C. M. Wu, and Y. C. Sun, "0.13 μm low voltage logic based RF CMOS technology with 115 GHz f_T and 80 GHz f_{MAX} ," in *Eur. Microw. Conf.*, Oct. 2003, pp. 683–686.
- [16] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
- [17] X. Wang, X. Zhao, Y. Zhou, X. Dai, and B. Cai, "Fabrication and performance of a novel suspended RF spiral inductor," *IEEE Trans. Electron Devices*, vol. 51, no. 5, pp. 814–816, May 2004.
- [18] D. Peroulis, S. Mohammadi, and L. P. B. Katehi, "High-Q integrated passive elements for high frequency applications," in *Silicon Monolithic Integr. Circuits in RF Syst. Top. Meeting*, Sep. 2004, pp. 25–28.
- [19] T. H. Lee, "CMOS RF: No longer an oxymoron," in *19th Annu. Gallium Arsenide Integr. Circuit Symp.*, Oct. 1997, pp. 244–247.
- [20] T. Cheung, J. Long, K. Vaed, R. Volant, A. Chinthakindi, C. Schnabel, J. o. Florkey, and K. Stein, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *Int. Solid-State Circuits Conf.*, 2003, vol. 1, pp. 396–401.
- [21] P. Sjöblom and H. Sjöland, "Measured CMOS switched high-quality capacitors in a reconfigurable matching network," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 10, pp. 858–862, Oct. 2007.
- [22] L. Rabeirad and S. Mohammadi, "A reconfigurable MEMS-less CMOS tuner for software defined radio," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2008, pp. 779–782.
- [23] R. B. Whatley, Z. Zhou, and K. L. Melde, "Reconfigurable RF impedance tuner for match control in broadband wireless devices," *IEEE Trans. Antennas Propag.*, vol. 54, no. 2, pp. 470–478, Feb. 2006.
- [24] H. Lee, T. Choi, S. Mohammadi, and L. P. B. Katehi, "An extremely low power 2 GHz CMOS LC VCO for wireless communication applications," in *Eur. Wireless Technol. Conf.*, Oct. 2005, pp. 31–34.
- [25] D. Mirshekar-Syahkal and J. Danneel, "Criteria for single mode operation of packaged coplanar waveguide circuits," *IEE Modeling, Design, Applicat. MMIC's Colloq.*, pp. 8/1–8/4, Jun. 1994.
- [26] M. Riazat, I. Zubeck, S. Bandy, and G. Zdasiuk, "Coplanar waveguides used in 2–18 GHz distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 1986, vol. 86, pp. 337–338.
- [27] D. Johns and K. martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997, pp. 34–35.
- [28] K. Schimpf, B. Benna, and D. Proetel, "A new approach to characterize substrate losses of on-chip inductors," in *Proc. IEEE Int. Microelectron. Test Structures Conf.*, Mar. 2001, vol. 14, pp. 115–118.



Laleh Rabeirad (S'04–M'09) received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 2008.

She is currently a Postdoctoral Fellow with the California Institute of Technology, Pasadena. During the summer and fall of 2006, she was a Student Intern with Freescale Semiconductors Inc., Tempe, AZ. Her research interests are microwave and RF reconfigurable circuits and integrated-circuit design.



Saeed Mohammadi (S'89–M'92–SM'02) received the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 2000.

He is currently an Associate Professor of electrical and computer engineering with Purdue University, West Lafayette, IN. His group is involved in research in RF devices and circuits, RF integration, and nanotechnology. He has authored or coauthored over 100 journals and refereed conference papers.

Dr. Mohammadi was an associate editor for the IEEE MICROWAVE AND WIRELESS COMPONENTS

LETTERS from 2006 to 2007.