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Generating integrated-circuit patterns via cutting and stitching of gratings

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Integrated-circuit patterns, such as those of transistor gates, usually consist of multivertex paths whose line segments are along two orthogonal directions. Such patterns are sometimes called “Manhattan structures” and are typically designed to achieve the highest packing density with a given linewidth. Owing to their arbitrary shapes, these patterns are predominantly generated via electron-beam lithography, a serial process which is inherently slow compared to parallel processes. Moreover, throughput is further reduced with the necessity of proximity correction in electron-beam lithography. On the other hand, interference lithography is a low-cost, parallel process that can achieve small linewidths and pitches, yet the achievable patterns are limited to gratings or other periodic structures. Here the authors propose to synthesize arbitrary Manhattan structures from regular structures such as gratings via cutting and stitching. They demonstrate the cutting and stitching of large-area, highly smooth gratings formed by interference lithography and orientation-dependent etch of silicon. Our method could significantly reduce the writing time in electron-beam lithography for pattern generation and requires no proximity correction. © 2009 American Vacuum Society. [DOI: 10.1116/1.3264677]

I. INTRODUCTION

Integrated circuits (ICs) are ubiquitous and are essential to a variety of applications ranging from computing, communication, to industry control, entertainment, etc. For high-throughput manufacturing of ICs, duplicating the circuit patterns on masks or templates via photons (e.g., optical projection lithography) or mechanical interaction (e.g., nanoimprint lithography¹) is preferred due to its ability to transfer billions of pixels in one exposure.² Meanwhile, patterns on masks and templates must be generated with a tool capable of placing a large variety of high-resolution features at arbitrary locations specified by the design. Such a process is typically serial and time consuming. The current state of the art for IC mask making is the electron-beam lithography (EBL), including both Gaussian-beam and variable shaped beam lithography systems, with the latter being applied in the manufacturing of application specific integrated circuits (ASICs). However, the decreasing feature sizes on the masks, as well as resolution enhancing techniques such as optical proximity correction, lead to more stringent requirements in placement accuracy and to larger amount of pixels to be exposed in serial fashion. Furthermore, proximity effects in EBL need to be corrected at every turn along the path and at the ends of the paths. This will require a beam step size smaller than the minimum linewidth and will further reduce the throughput of the electron-beam lithography.

The long pattern generation time and stringent pattern fidelity requirements in mask/template production translate to long turn-around time and high cost for IC masks/templates. While such cost can be amortized in large-volume productions, it is prohibitive for prototyping new device and circuit designs and also causes a significant cost disadvantage for

low-volume manufacturing of ASICs. In nanoimprint lithography, low-cost template generation is desirable even for high-volume production, as the templates may accumulate defects during imprint, and consequently having a low lifetime.²

It is therefore important, in parallel to maskless lithography, to develop a method that can reduce the turn-around time and cost of mask/template sets. This could significantly reduce the cost of small-volume ASICs and allow them to get access to latest integrated-circuit manufacturing technology. It could also allow rapid circuit prototyping, therefore reducing the time to market and avoiding costly circuit design flaws.

II. SYNTHESIZING ARBITRARY MANHATTAN STRUCTURES VIA CUTTING AND STITCHING GRATINGS

Here we propose and demonstrate an approach which explores the pseudoperiodic characteristic of Manhattan structures to achieve parallelism in template making and potential mask making. Fritze *et al.* explored the double exposure method in which the first exposure images high resolution dense gratings using maskless interference lithography, followed by second exposure using mainstream projection lithography to cut the gratings into geometries useful for complementary-metal-oxide-semiconductor fabrication.³ While it is possible to place most of the transistor gates along grating lines, it is also very important to have a mechanism to create line segments that are orthogonal to the grating teeth. This gives one the flexibility to connect line segments in different grating teeth and helps minimize the area of a specific design. Therefore, in addition to cutting, stitching the gratings at specific locations is highly desirable, even if the amount of “stitches” in a design is small.

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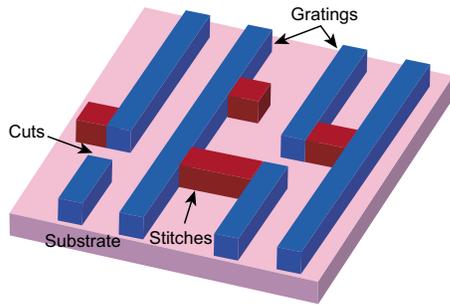


FIG. 1. (Color online) Illustration of the synthesis of arbitrary Manhattan structures from gratings. After the grating teeth are patterned, they are cut at specific locations and then connected together by stitches to form designed pattern.

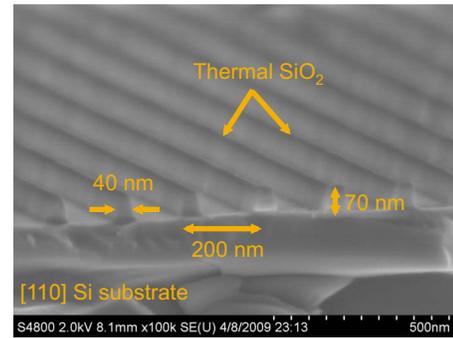
The strategy to generate arbitrary Manhattan structures from regular structures such as gratings is illustrated in Fig. 1. Gratings can be cut and then stitched together at designed locations. The areas to be cut or stitched can be significantly reduced when compared to the total area of grating teeth, cuts, and stitches. We will form highly smooth gratings by orientation-dependent etching of the [110] silicon. This could mitigate the issue of line-edge roughness in nanometer-scale transistors. Grating patterns will be patterned with high-throughput methods such as laser interference lithography, which significantly reduces the electron-beam time required for pattern generation.

III. ACHIEVING HIGHLY SMOOTH GRATINGS

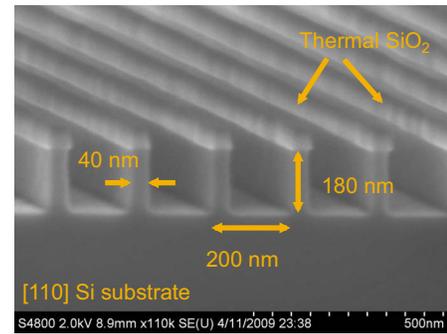
A [110] oriented silicon wafer was first oxidized in dry O_2 in a table-top furnace (Blue-M) at atmosphere to yield a 70 nm thick oxide. An antireflective coating layer (BARLi, from AZ Electronic Materials) of 150 nm was then spun on the oxide, followed by a 220 nm thick PFI-88 photoresist (from Sumitomo). 200 nm pitch gratings were exposed with laser interference lithography in a class-10 clean room. The interference lithography is a Lloyd's mirror setup⁴ with a continuous-wave He-Cd laser operating in single frequency mode at 325 nm as light source. Gratings were manually aligned along the [111] crystal orientation of the [110] Si wafer.

The BARLi was etched with photoresist as mask in a high-density plasma etching tool (Panasonic E620) with O_2 plasma. The selectivity between the PFI-88 and BARLi is about 1. Reactive ion etching with CHF_3 in the same tool transferred the grating into the oxide layer [Fig. 2(a)]. The slanted sidewall was primarily due to the low selectivity between the PFI-88 and BARLi.

When transferring the grating into silicon, we took advantage of the orientation-dependent silicon wet etching. In basic solutions, such as potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH), the etch rate of [111] plane in silicon is two order-of-magnitude slower than [100] or [110] planes.^{5,6} With the patterned oxide layer as etch mask, gratings with highly smooth sidewalls were achieved with 14% (in weight) KOH wet etching at 55 °C [Fig. 2(b)].



(a)



(b)

FIG. 2. (Color online) (a) Gratings etched into thermal oxide. The pattern was generated via interference lithography. Roughness is noticeable; (b) KOH etched Si gratings with highly smooth sidewalls.

This shows that we can tolerate relatively high line-edge roughness in the oxide mask layer due to the self-smoothing effect of orientation-dependent etching.

The period of gratings generated with our interference lithography setup is limited by the wavelength of the exposure light (325 nm). The minimum pitch obtained by this technique using our exposure system is around 170 nm, which is about half of the He-Cd laser wavelength when the exposure is done in air. Grating pitches of 44 nm or less have been generated with 157 nm laser source⁷ or synchrotron.⁸ Unfortunately such light sources are unavailable to us. For the purpose of demonstrating our technology, we used electron-beam lithography to generate the grating at 64 nm pitch. A negative-tone electron-beam resist, hydrogen silsesquioxane (HSQ) from Dow Corning Co. (Fox-12) was used. Upon exposure to an electron beam, HSQ undergoes cross-linking following the dissociation of the Si-H bond of the structure.⁹ The cross-linked area of the HSQ is insoluble to alkaline hydroxide developer¹⁰ and has etch mask properties similar to that of SiO_2 . A layer of 45 nm HSQ was spun on the [110] silicon wafer and soft baked at 175 and 220 °C for 2 min on hot plates, respectively, to remove the solvent. Then it was exposed by electron beam (Vistec VB6) at 0.6 nA beam current with 2 nm step size at 100 kV, followed by the development in TMAH for 1 min [Fig. 3(a)]. In order to enhance the etch resistance of HSQ, the sample underwent rapid thermal annealing at 1000 °C for 2 min in N_2 environment. Grating was then etched into Si at 30 °C in 7% (in weight) KOH, with megasonic agitation. Figure 3(b)

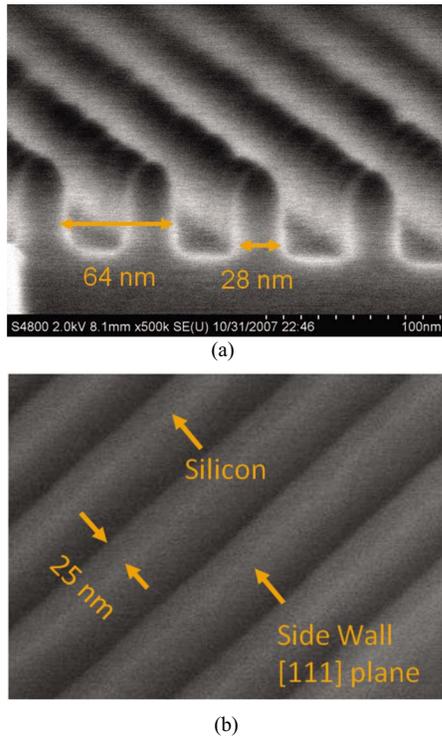


FIG. 3. (Color online) (a) Gratings in 45 nm thick HSQ at 64 nm pitch. Roughness is clearly visible; (b) KOH etched Si with highly smooth sidewalls.

shows the generated gratings with highly smooth sidewalls at 25 nm linewidth and 64 nm pitch, better than those generated directly with electron-beam lithography [Fig. 3(a)].

IV. CUTTING AND STITCHING OF THE GRATINGS

The design of an integrated circuit manifests itself through the interconnection between different line segments, which could be transistor gates or metal lines. The first step is to isolate the many line segments residing on a single grating tooth from each other. Figure 4(a) illustrates the process we adopted to cut the gratings. A layer of ZEP 520A resist (ZEON Corp.) was spun over the gratings at 3000 rpm for 50 s, followed by the soft baking at 170 °C for 2 min. This yielded a thickness of around 450 nm, which was significantly thicker than the depth of the trenches (180 nm) in the 200 nm pitch grating. ZEP 520A is a positive electron-beam resist and has been widely used due to its much better dry-etch resistivity than polymethyl-methacrylate. Lines orthogonal to the grating teeth were exposed with electron-beam lithography (VB6 from Vistec). The writing current was 1 nA and the beam step size was 2 nm. Development was first carried out in xylene for 40 s, then in methyl isobutyl ketone:isopropyl alcohol (IPA) (1:3) for 30 s, and finally rinsed in IPA before blow dry. After hard baking at 140 °C for 2 min, reactive ion etching was done in a high-density plasma tool (STS-ASE) with a mixture of SF₆ and O₂ to cut the gratings. A final O₂ plasma etching removed the remaining ZEP 520A. Figure 4(b) shows the trench cut across the

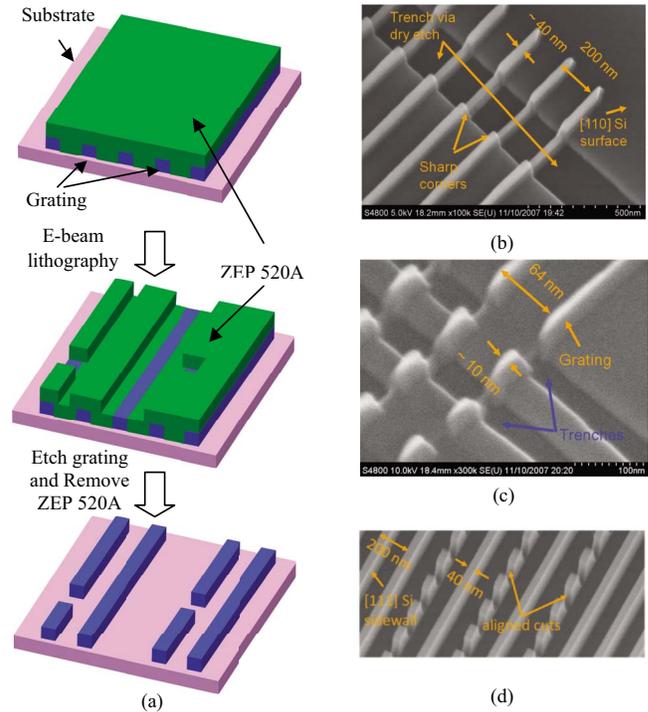


FIG. 4. (Color online) (a) Schematic of the cutting process. A thick photo-resist for e-beam lithography, such as ZEP 520A, is spun over the grating and exposed by EBL at designed locations. Grating teeth not protected by the ZEP 520A will be etched away by reactive-ion etch. Finally the resist is removed by oxygen plasma. (b) An orthogonal cut in 200 nm pitch grating formed by interference lithography and orientation-dependent etch. The grating pattern remained in the trench. However, it will not be duplicated in nanoimprint lithography if the cut is sufficiently deep. (c) Cutting gratings at 64 nm pitch. Grating line width is approaching 10 nm. (d) Aligned cuts in 200 nm pitch grating.

grating of 200 nm pitch. We note that the grating pattern remained in the trenches. However, when the structure is used as a mold for imprint lithography, the grating pattern inside the trench will not be transferred to the resist because it is recessed and will not touch the resist during the imprint process. We also note the sharp corners at the ends of the chopped grating teeth. Our exposed pattern in e-beam lithography was simply a straight line without any proximity correction. Therefore, the cutting process can help achieve sharp corners in e-beam lithography with no proximity correction. Figure 4(c) shows the cutting of grating at 64 nm pitch. Due to the shallower grating trenches at 64 nm pitch, the ZEP 520A was diluted to achieve a smaller resist thickness (150 nm). Rectangular dots of around 10 × 30 nm² have been achieved.

For any integrated-circuit pattern, alignment between the cuts and grating is crucial. To achieve that, square alignment marks for e-beam lithography was dry etched into the silicon wafer prior to the interference lithography or e-beam lithography. The alignment marks were placed away from the grating area to be cut and shielded from the lithography exposures. The cuts were then exposed with reference to the alignment marks. Figure 4(d) shows aligned cuts in grating

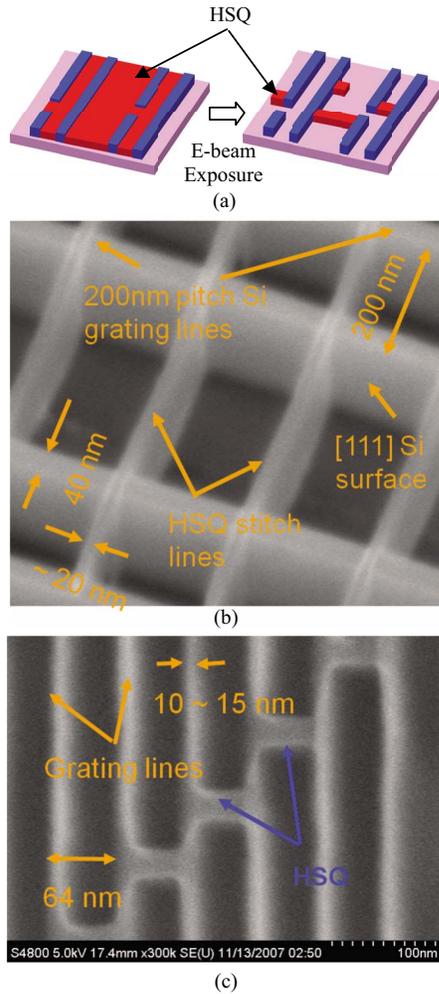


FIG. 5. (Color online) (a) Schematic of the stitching process. A negative e-beam resist, e.g. HSQ, is spun over the grating with cuts. The exposed HSQ forms the desired stitches. (b) Stitches formed in gratings generated by IL at 200 nm pitch; (c) Aligned stitches in grating of 64 nm pitch.

teeth. Notice the absence of any recess at the bottom of the grating trenches, an indication of high alignment accuracy and exposure dose control.

Certain circuit patterns can be formed by the cutting process only. However, to achieve optimal design, or to translate a previous design that was not optimized for grating-cutting technology, one needs to connect some grating segments after the cutting. We call this process “stitching” [Fig. 5(a)]. The material forming the stitches is HSQ, as it is a negative-tone resist and can be transformed into SiO_2 after EBL. HSQ was spin coated onto the grating that had gone through the cutting process. Contrary to the case of ZEP resist, the thickness of the HSQ was chosen such that little HSQ was on top of the grating teeth after spinning and baking. For a trench depth of ~ 180 nm as in the 200 nm pitch grating, the thickness of the HSQ was 220 nm, and for a trench depth of ~ 80 nm as in the 64 nm pitch grating, the thickness of HSQ was 90 nm. HSQ was baked at 175 and 220 $^\circ\text{C}$, respectively, before being exposed at 0.8 nA with 2 nm beam step size. The exposed or cross-linked areas have similar properties as

those of SiO_2 . Upon development in TMAH for 1 min, the exposed areas become the stitches that form the Manhattan patterns, while unexposed HSQ was removed, leaving the original gratings. Figure 5(b) shows the 20 nm wide HSQ stitches across 40 nm wide grating teeth. The grating teeth are horizontal and have a pitch of 200 nm. The middle grating tooth was removed by the cutting process. The grating trench was about 180 nm deep. Due to the thin resist above the grating teeth, there were little HSQ over the grating teeth even if the electron beam scanned through the area during the exposure. The resulting structure is therefore almost identical to those formed in one lithography process. Moreover, the rectangle structures in Fig. 5(b) have sharp corners, again without applying proximity correction in EBL. Figure 5(c) shows the aligned stitching for 64 nm pitch gratings.

We note that the stitches, formed by HSQ directly exposed by EBL, will have larger sidewall roughness than those generated with orientation-dependent etch. However, for integrated circuits, the critical transistor gates are usually along the grating teeth and the stitches typically are for local interconnects between the gates. Therefore, the slightly higher roughness of the HSQ stitches might not have a major impact on the performance of the circuits.

V. CONCLUSION AND OUTLOOK

We proposed and demonstrated a scheme to generate arbitrary integrated-circuit patterns (or Manhattan structures) via cutting and stitching of gratings. Gratings of 200 nm pitch were exposed with high-throughput laser interference lithography, while pitches down to 64 nm were achieved with electron-beam lithography. The gratings were formed in the [110] silicon wafers via orientation-dependent wet etch and were highly smooth. Both aligned cutting and stitching of grating were achieved for gratings down to 64 nm in pitch. Stitched gratings were almost identical to those formed in one lithography step. We also achieved sharp corners using our method without proximity correction in electron-beam lithography.

These formed Manhattan patterns are currently explored as the templates for duplication via nanoimprint lithography. The initial results showed that the structures stood well in thermal nanoimprint process even though the stitched structures are different from the grating teeth. Nevertheless, more work remains to be done in order to assess the damage threshold of stitched structures (in our case, HSQ) in comparison to the grating structure (in our case silicon). We note that the HSQ and silicon have different optical properties, thus making our structure unsuitable as an optical mask. However, a nanoimprint template can in principle be duplicated via nanoimprint lithography to form an optical mask, considering the high line-edge smoothness achieved in our structure. The goal of our method is to significantly reduce the time in pattern generation when compared to electron-beam lithography. Quantitative analysis of the time saved from direct electron-beam write is currently being carried out. We believe this scheme could potentially be a solution to

low-cost, fast turnaround manufacturing of low-volume ASICs.

We also envision that our technology could be used to repair templates used in nanoimprint lithography or to correct small circuit design errors. The cutting and stitching process can indeed be viewed as a repair procedure. To this end, it might also be possible to completely erase part of the template and replace it with some other design. Therefore several versions of the same circuit design, but with slightly different functionality could be conveniently implemented at the hardware level.

ACKNOWLEDGMENT

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