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Defect Analysis of Barrier Height Inhomogeneity in Titanium 4H-SiC Schottky Barrier Diodes

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Over 350 4H-SiC Schottky barrier diodes (SBDs) of varying size are characterized using current–voltage (I – V) measurements, with some also measured as a function of temperature. Devices display either a characteristic single-barrier height or atypical dual-barrier heights. Device yields are shown to decrease as device area increases. Molten KOH etching is used to highlight defects for analysis by optical microscopy and atomic force microscopy. The I – V characteristics are compared against the defect density. A positive correlation between effective barrier height and effective electrically active area of the SBDs is found. No correlation is found between threading dislocations and ideality factor or barrier height.

Key words: Silicon carbide, Schottky barrier diode, barrier height, threading dislocations, crystal defects

INTRODUCTION

Silicon carbide (SiC) is a promising material due to its superior intrinsic material properties over silicon. Comparatively, it has a higher thermal conductivity, larger breakdown potential, and better velocity saturation. However, SiC has problems related to growth defects which cause degradation of device performance.¹ For many years open-core dislocations, such as micropipes, have been cited as an important cause of poor device performance.² As time passed, new growth techniques emerged to reduce the number of micropipes to an insignificant amount.^{3,4} This brought other defects such as basal plane dislocations into consideration as causing poor bipolar device performance.^{5,6} More innovative growth techniques came along that allowed basal plane dislocations to be converted into threading dislocations.⁷ In chronological progression, now threading dislocations are being investigated. In this paper, the effects of threading edge and threading screw dislocations on Schottky barrier diode (SBD) electrical characteristics are analyzed.

EXPERIMENTAL PROCEDURE

Fabrication of SBDs began on a 4H-SiC n -type wafer from Cree with a 6- μ m epitaxial layer with doping of $2.3 \times 10^{16} \text{ cm}^{-3}$ as measured using C – V techniques. The substrate vicinal angle is 8 deg toward $\langle 11\bar{2}0 \rangle$ with the SBDs being fabricated on the Si-face. The samples were initially cleaned and polysilicon was deposited via low-pressure chemical vapor deposition as an implantation mask against boron for the formation of resistive edge terminations. At a substrate temperature of 400°C, boron was implanted at an energy of 30 keV with a dose of $1 \times 10^{15} \text{ cm}^{-2}$. The edge termination ring structures were patterned using standard photolithography techniques. The samples were then annealed at 1050°C for 90 min under high vacuum.⁸ This temperature avoids electrically activating the boron which maintains high resistivity of the edge termination.⁹ The large-area backside contact started with the e-beam evaporation of 150 nm of nickel under high vacuum. The backside was rapid thermal annealed for 2 min at 1000°C in an atmosphere of nitrogen. The backside was then capped by e-beam evaporation of a thin layer of titanium followed by a thicker layer of nickel. The surface of the samples was prepared for Schottky contacts by immersion in buffered oxide etch. The Schottky

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contacts were formed through the evaporation of 100 nm of titanium followed by a gold cap. The Schottky contacts remain unannealed and were of varying areas between $7.85 \times 10^{-5} \text{ cm}^2$ and $2.5 \times 10^{-1} \text{ cm}^2$. Surface passivation was then performed through a blanket plasma-enhanced chemical vapor deposition of SiO_2 . Contact windows were opened through standard photolithographic techniques and wet etching.

After fabrication, testing of devices was done using I - V measurements performed by using a probe station and a HP4156A semiconductor parameter analyzer. Over 350 diodes of varying sizes were measured and characterized with this technique, providing information on device performance and yield. Since the main purpose of this work is to analyze forward-bias inhomogeneities, no reverse-bias measurements are included in this paper. To further characterize selected SBDs, I - V data was measured with respect to temperature (I - V - T). A variable-temperature stage was used for I - V - T measurements and the diodes were measured between 293 K and 390 K at 20 K intervals. The temperature of the stage was measured with a Fluke 52II thermometer. There were 66 diodes selected for I - V - T characterization. The I - V - T technique allows for extraction of the effective barrier height and electrically active area of individual devices. The effective barrier height can be measured for devices that show either single- or dual-barrier heights. C - V measurements were performed using an HP4284A LCR meter at a frequency of 1 MHz and a voltage sweep of 1 V to -10 V. After all electrical measurements were completed, the surface passivation was wet-etched, the Schottky contacts

served as a reactive-ion etch mask to outline their presence on the epitaxial layer, and then the contacts were stripped via wet etching. The epitaxial layer was destructively etched using molten KOH in a nickel crucible at 520°C for tens of minutes to decorate defects for imaging by optical microscopy and atomic force microscopy.

RESULTS AND DISCUSSION

From I - V measurements, the SBDs demonstrate both ideal single-barrier height (homogeneous) and atypical dual-barrier height (inhomogeneous) features. This can be seen in Fig. 1, which shows the I - V curves of a total of 120 SBDs at four different device areas measured at room temperature. A poignant feature comparing device areas is the decrease in dual-barrier height devices as area decreases. This suggests that there is a correlation between device area and barrier height homogeneity. These barrier height features are not found to be a function of location on the wafers. In other words, dual-barrier height features do not show a tendency to cluster near other inhomogeneous devices. To extract device yield, the set of criteria for deciding whether a device performs successfully is based on showing a single-barrier height with an ideality factor of less than 2. The $7.85 \times 10^{-5} \text{ cm}^2$ area diodes have a yield of 96% whereas the largest diodes of area $2.5 \times 10^{-1} \text{ cm}^2$ have a yield of 40%. Figure 2 shows the yield of measured devices versus area.

From the entire data set of single-barrier height devices, I - V experiments exhibit an average ideality factor of 1.23 with an average barrier height of

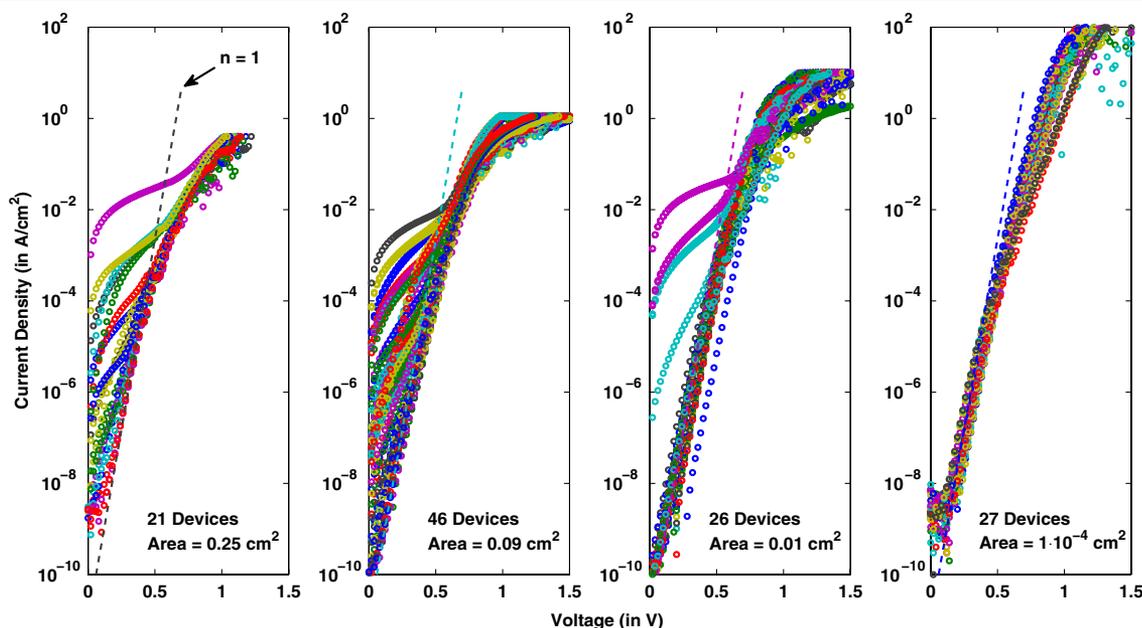


Fig. 1. I - V curves of 120 SBDs of various sizes measured at 293 K. Device area decreases from left to right, and correlates with increasing barrier homogeneity. The superimposed dashed line shows an ideality factor of 1.

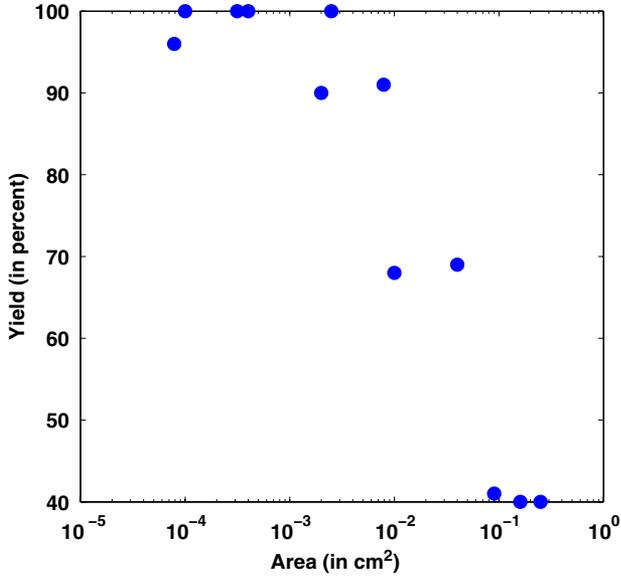


Fig. 2. Yield of the over 350 measured SBDs as a function of their area.

1.17 eV. The ideality factor is found using the ubiquitous method of taking the slope of the linear forward conduction region. The barrier height is then calculated by extrapolating the forward conduction region back to zero bias to determine the saturation current of the diode. Under the assumption of thermionic emission being the major forward current contribution, the diode current of a homogeneous device can be determined as

$$I = I_{\text{sat}} e^{\frac{q(V-IR_s)}{nkT}}, \quad (1)$$

$$I_{\text{sat}} = AA^* T^2 e^{-\frac{q\phi_b^0}{kT}}, \quad (2)$$

where V is the applied bias, R_s is the series resistance, q is the charge of an electron, n is the ideality factor, k is Boltzmann's constant, and T is temperature. Furthermore, I_{sat} is the saturation current, which depends on device area, A ; Richardson's constant is A^* ; and ϕ_b^0 is the zero-bias barrier height.¹⁰ As can be seen, when solving for the zero-bias barrier height it is necessary to know both temperature and device area. Temperature of the diodes can be controlled and measured, but device area is not as easily known. The use of a device's physical footprint on the substrate in the calculations can be misleading since using the entire device's area makes the assumption of barrier height uniformity. Regions that have higher barrier heights than the nominal height will serve to block current contributions and will be excluded in the I - V measurements. Any regions underneath the SBD that have a lower barrier height¹¹ than the nominal 4H-SiC barrier height, such as 3C-^{12,13} or 8H-SiC¹⁴ polytype inclusions, will lead to a higher

current contribution at lower bias regimes. Barrier heights below the nominal height can be lumped together to act as a single diode represented by their own respective area, average barrier height, and series resistance. This lower barrier height diode contributes current in parallel with the nominal barrier height regions. When there is sufficient current contribution from the lower barrier height diode, inhomogeneity is seen in the I - V curves.

To explain the inhomogeneity seen in Fig. 1, a hypothesis is presented. As will be demonstrated later in this paper, unclustered threading dislocations are the most prevalent defect found via KOH etching. Using the parallel conduction model, barrier height deviations caused by threading dislocations do not interact with the nominal device barrier height. This model allows a decoupling between the assumed larger regions of nominal barrier height and the regions of lower barrier height. If threading dislocations affect electrical characteristics, then defect density should affect both barrier height and ideality factor. An increasing amount of threading dislocations should correlate with a decrease in effective barrier height and an increase in ideality factor.

To find the effective barrier height, I - V curves can be measured against temperature. For a single-barrier height device, the I - V curves can be seen in Fig. 3a. At each temperature, the saturation current is extracted and an Arrhenius plot of I_{sat}/T^2 versus $1/kT$ can be created, such as in Fig. 3b. The slope of this plot is $-\phi_b^{\text{eff}}$ and the y-intercept yields $\ln(A^{\text{eff}}A^*)$, where ϕ_b^{eff} is the effective barrier height and A^{eff} is the effective electrically active area of the diode. The effective barrier height represents the averaged contribution of barrier heights throughout the device and has no dependence on device area. In calculating the effective barrier height, only the linear conducting portion of the nominal barrier height regime of the I - V curve is used. The lower barrier height region could not be fit by a linear regression due to the lack of a linear portion at low biases. In addition, at higher temperatures this lower barrier height region can become obfuscated by current conduction over the nominal barrier height region. This phenomenon can be seen in Fig. 4a. For the homogeneous devices, a mean effective barrier height of 0.829 eV with a standard deviation of 0.03 eV is found. Note that the theoretical barrier height of titanium on 4H-SiC is 0.83 eV. The average effective barrier height extracted from the inhomogeneous barrier devices is 0.53 eV with a standard deviation of 0.15 eV. This lower average barrier height is also exhibited in C - V measurements. The average C - V barrier height is 1.07 eV for homogeneous and 0.93 eV for inhomogeneous devices. Figure 5 shows the Arrhenius plot of SBDs with a device area of $4 \times 10^{-2} \text{ cm}^2$. There is a clear distinction in both slope and linearity between the devices that have a single-barrier height and those that have dual-barrier heights.

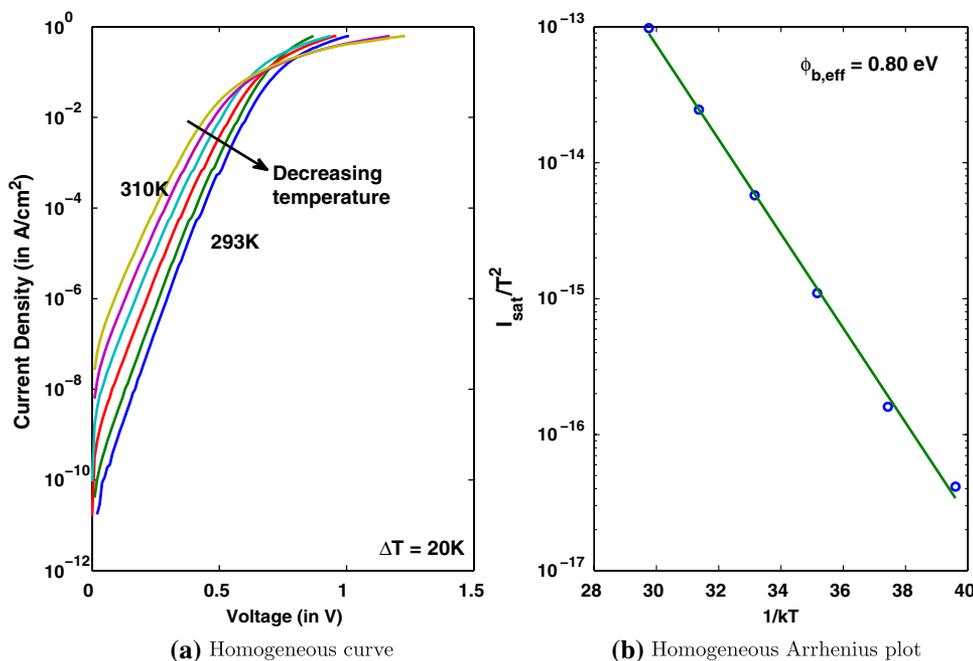


Fig. 3. (a) I - V - T curves showing the effect of temperature on a single SBD with a contact area of $1.6 \times 10^{-1} \text{ cm}^2$. (b) Arrhenius plot from which an effective barrier height of 0.80 eV is extracted.

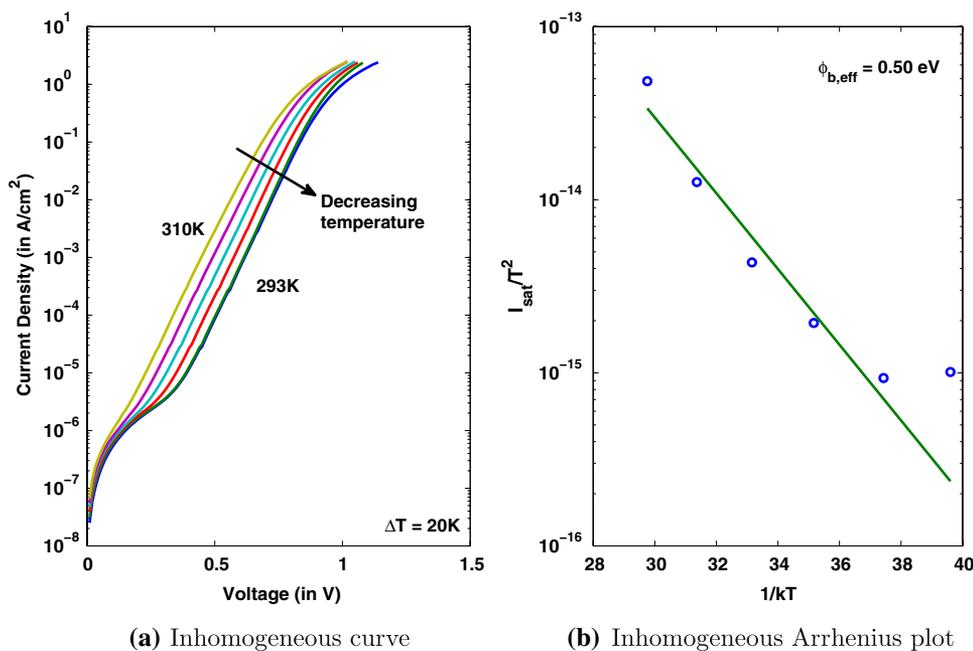


Fig. 4. (a) I - V - T curves showing the effect of temperature on a single SBD with a contact area of $4.0 \times 10^{-2} \text{ cm}^2$. (b) Arrhenius plot from which an effective barrier height of 0.50 eV is extracted with the outlying point at $1/kT = 39.6$ neglected.

Furthermore, the effective barrier height is plotted against the extracted effective electrical area that is extracted from the Arrhenius plots of the SBDs. As can be seen in Fig. 6, there is a very good linear correlation in the plot. The Richardson's constant used for extracting the effective electrical area is the theoretical value of $146 \text{ A cm}^{-2} \text{ K}^{-2}$. From

this value, the majority of the homogeneous devices have an extracted electrically active region that is 10% of the device's physical contact area. The exact value of Richardson's constant for SiC SBDs has been debated by Roccaforte et al.¹⁵ and Pirri et al.¹⁶ Using a lower Richardson's constant, as is common in the literature, would serve to increase the

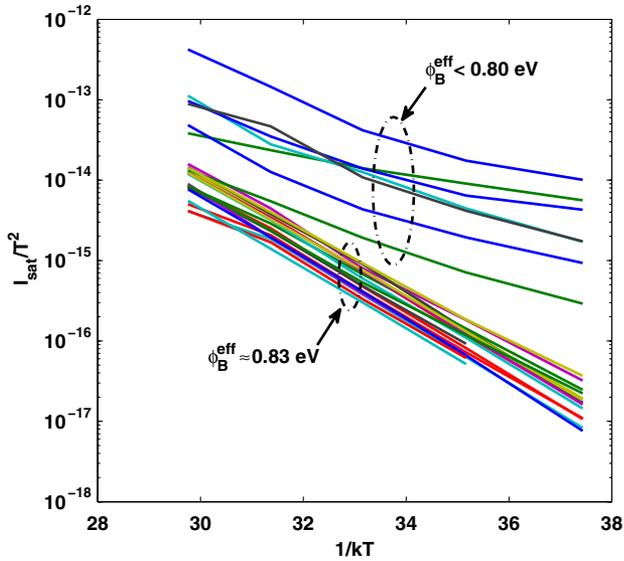


Fig. 5. Arrhenius plot of SBDs with an area of $4.0 \times 10^{-2} \text{ cm}^2$ showing lower effective barrier heights for devices exhibiting inhomogeneous characteristics.

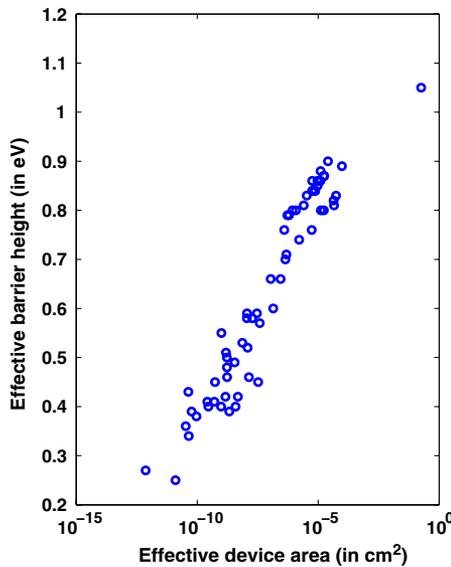


Fig. 6. Plot of effective barrier height measured against effective electrical area for multiple sized SBDs.

electrically active area. When comparing devices on Fig. 6, a change in the Richardson's constant only serves to shift all points horizontally and does not change their correlation with each other. Due to the Richardson's constant dispute and the fact that the points in Fig. 6 have been created by two sequential linear regression fittings, the exact value of the electrically active area of the devices is not precise. What is important is that the exact same linear regression methods are applied to create all of the data points. The variability in the linear regressions is averaged over 66 points, which means the trend of

the plot can be trusted even if the values along the x -axis are open to interpretation. From the shape of the plot, it can be seen that as barrier height decreases so does the electrically active area of the SBD. This implies that a SBD's effective barrier height is very much influenced by isolated regions. However, I - V - T data do not provide enough information to identify these regions. For this reason KOH etching was used to attempt to identify surface defects that may affect electrical performance and cause barrier height inhomogeneity.

The reasons behind barrier height inhomogeneity have not been elucidated yet. Skromme et al.¹⁷ demonstrated a correlation between the number of dark spots imaged via electron beam induced current (EBIC) and a SBD's ideality factor. Ewing et al.¹⁸ found that barrier height inhomogeneity is shown to happen where there is a large conglomerated area of defects and the defects relate to three specific centers in the 4H-SiC bandgap. However, EBIC alone is unable to show the exact type of defect that causes inhomogeneity. This is the benefit of using a molten KOH etch. The Si-face of a 4H-SiC epitaxial layer is etched preferentially at specific defect locations. In addition, the defect type leaves a characteristic signature in the substrate when it is etched. Oval pits are characteristic of basal plane dislocations, large hexagonal pits are caused by micropipes, medium-sized hexagonal pits occur from threading screw dislocations, while the smallest hexagonal pits form at threading edge dislocations.¹⁹

After stripping the Schottky contact, the devices were molten etched in KOH to produce telltale defect signatures with the intention of correlating them to device electrical characteristics. As can be seen in the optical microscopy image of Fig. 7a, multiple spots are decorated in the epitaxial layer. The vast majority of these spots are found to be either threading edge or threading screw dislocations. To help elucidate the shape of the threading dislocations further atomic force microscopy was performed, as shown in Fig. 7b. The number of visible threading dislocations averaged $2.37 \times 10^4 \text{ cm}^{-2}$.

Nitani et al.²⁰ have proven that EBIC imaging shows a direct correspondence to defects that are decorated by KOH etching. This is confirmation that threading screw and threading edge dislocations are electrically active. To determine their role in affecting SBDs, the threading dislocations are counted underneath each SBD's contact pad. The number of defects is divided by the device area to create a defect density that is used to compare devices of varying size. No micropipes were found and the number of basal plane dislocations was too small to estimate their density. Only the visible threading dislocations are counted toward the overall defect density. The defect size differences between threading and screw dislocations are noticeable, but there are many defects that fall in a size range between the largest threading screw

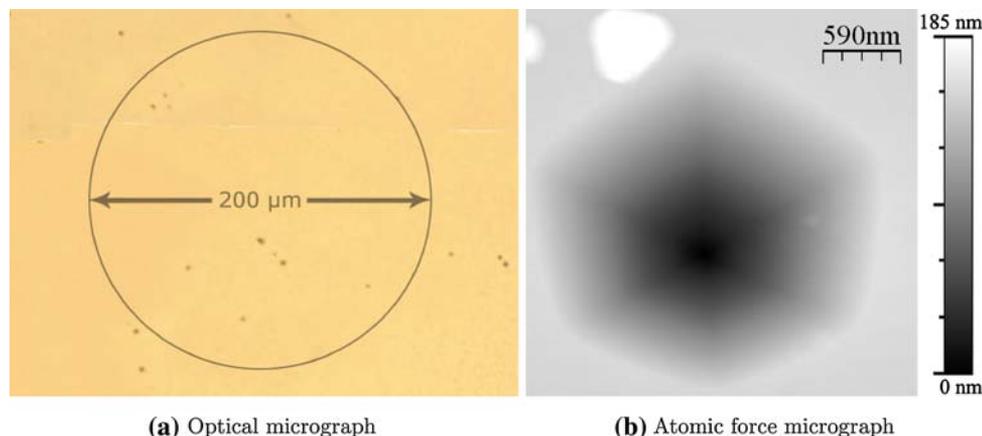


Fig. 7. (a) Optical microscopy image of threading dislocations decorated by molten KOH etching and (b) high-resolution atomic force image of one of the etch pits.

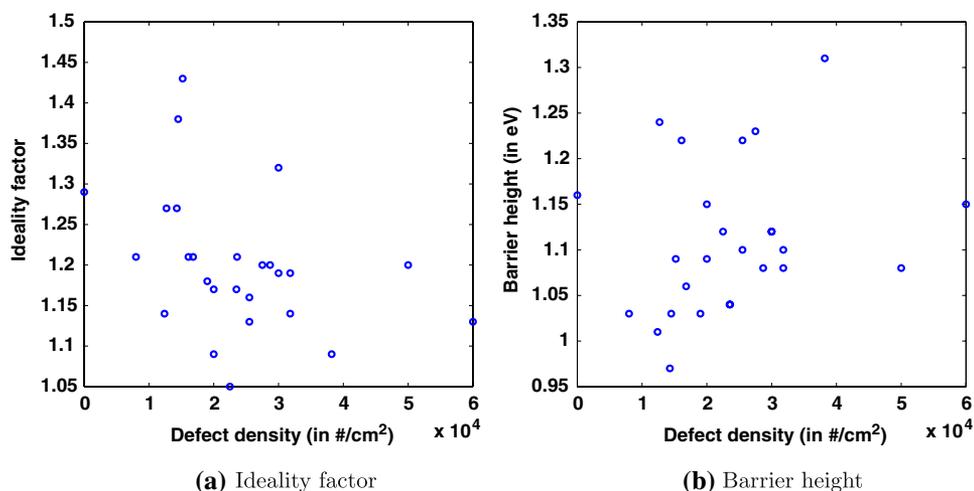


Fig. 8. Defect density of threading edge and screw dislocations found under SBD contact area plotted against corresponding device ideality factor and barrier height.

dislocation and the smallest threading edge dislocation. The average-sized defects could not be categorized definitively as screw or edge dislocations. It is for this reason that both threading edge and threading screw dislocations are combined to give a total defect density. To correlate dislocations to electrical characteristics, defect density is plotted against both device ideality factor and effective barrier height. The results are shown in Fig. 8. As can be seen, no correlation can be made with either ideality factor or barrier height. This suggests that threading dislocations *do not* significantly affect the electrical characteristics of the devices. Optical microscopy results show that the decorated defects are spread out far enough to prevent making a conclusion about whether clustering of threading dislocations affects electrical performance.

These results, in both range of extracted ideality factor and conclusion, are in good agreement with those found by Ewing et al.²¹ However, this does not agree with the results found by Skromme et al.,¹⁷

who found a linear correlation between the number of dark spots imaged via EBIC and a SBD's ideality factor. Since EBIC imaging highlights threading dislocations and molten KOH etching decorates threading dislocations, a direct comparison can be made in counting defects. As shown in Fig. 8, no correlation was seen between defect density and ideality factor. This demonstrates that there is no significant effect of threading dislocations on the electrical performance of the devices.

CONCLUSION

SBDs were fabricated on *n*-type 4H-SiC using unannealed titanium. Devices displayed either a characteristic single-barrier height or atypical dual-barrier heights in the *I-V* data. From *I-V-T* measurements, a correlation was found between effective barrier height and the effective electrically active area of the measured SBDs. When effective device area decreases, the effective barrier height

also decreases. This spurred interest in determining the reason for this correlation, which led to a molten KOH etch to decorate defects in the epitaxial layer of the SBDs. The highlighted defects were overwhelmingly either threading edge or threading screw dislocations. No micropipes were found and basal plane dislocations were inestimably minimal. In plotting the defect density of threading dislocations against the ideality factor and barrier height no correlation was found. Since there was no significant conglomeration of defects found clustered together, this leads to the conclusion that single threading edge and threading screw dislocations do not significantly affect the electrical characteristics of 4H-SiC SBDs.

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