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G Brammertz

IMEC VZW, B-3001 Louvain, Belgium

H C. Lin

Purdue University - Main Campus

K Martens

IMEC VZW, B-3001 Louvain, Belgium

D Mercier

IMEC VZW, B-3001 Louvain, Belgium

C Merckling

IMEC VZW, B-3001 Louvain, Belgium

See next page for additional authors

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Authors

G Brammertz, H C. Lin, K Martens, D Mercier, C Merckling, J Penaud, C Adelman, S Sioncke, W E. Wang, M Caymax, M Meuris, and M Heyns



Capacitance–Voltage Characterization of GaAs–Oxide Interfaces

G. Brammertz,^{a,*} H. C. Lin,^b K. Martens,^a D. Mercier,^a C. Merckling,^a
J. Penaud,^c C. Adelmann,^{a,*} S. Sioncke,^a W. E. Wang,^d M. Caymax,^{a,*} M. Meuris,^a
and M. Heyns^{a,e}

^aIMEC vzw, 3001 Leuven, Belgium

^bBirck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907-2057, USA

^cRiber, 95870 Bezons Cedex, France

^dIntel Assignee at IMEC, 3001 Leuven, Belgium

^eDepartment of Metallurgy and Materials Engineering, KU Leuven, 3001 Leuven, Belgium

We will shortly review the basic physics of charge-carrier trapping and emission from trapping states within the bandgap of a semiconductor in order to show that high-temperature capacitance–voltage (C - V) measurements are necessary for GaAs metal–oxide–semiconductor characterization. The midgap trapping states in GaAs have characteristic emission times on the order of 1000 s, which makes them extremely complicated to measure at room temperature. Higher substrate temperatures speed up these emission times, which makes measurements of the midgap traps possible with standard C - V measurements. C - V characterizations of GaAs/ Al_2O_3 , GaAs/ Gd_2O_3 , GaAs/ HfO_2 , and $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}/\text{Al}_2\text{O}_3$ interfaces show the existence of four interface state peaks, independent of the gate oxide deposited: a hole trap peak close to the valence band, a hole trap peak close to midgap energies, an electron trap peak close to midgap energies, and an electron trap peak close to the conduction band.
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In the past few years a growing interest in passivation of III-V surfaces has emerged again. Several problems exist, nevertheless, with the characterization of these interfaces, leading to some confusion in the literature. These problems have three main causes: First of all, these interfaces present very high densities of interface states, which leads to weak Fermi level pinning and Fermi level pinning behavior at the surfaces, phenomena rarely observed at Si surfaces.¹ Also the interface state distributions are quite different from the “U”-shaped Si interface state distributions.² Finally, the relatively larger bandgap of some III-V semiconductors as compared to Si leads to time constants of interface traps well above the usual time constants observed at Si interfaces, creating very long time constant phenomena, not observable with routine capacitance–voltage (C - V) characterization techniques.³ A possible solution to all of these problems is the photoluminescence intensity characterization technique,⁴ which is a fast measurement technique that has the big advantage of being sensitive to the integral of all interface states present at the III-V surface. Some disadvantages are the relative insensitivity of the technique in the range of 10^{13} – 10^{15} interface states/ cm^2 , a range in which the largest majority of III-V interfaces unfortunately reside, as well as the difficulty to extract energy distributions of interface state densities (D_{it}). In this contribution we apply a different technique, the conductance method,⁵ and we apply it at different temperatures, which allows the extraction of interface state density over the whole bandgap of GaAs or $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$. First, some general theory is presented, followed by the presentation of experimental measurements on different GaAs and InGaAs metal–oxide–semiconductor (MOS) capacitor samples with Al_2O_3 , Gd_2O_3 , and HfO_2 gate dielectrics.

Measurement Method

C - V measurements are made on MOS structures. The band diagram of a typical MOS structure is shown in Fig. 1, where a gate voltage (V_g) is applied between the metal and the semiconductor, which fixes the value of the surface Fermi level (surface potential). A hypothetical interface state distribution at the semiconductor–oxide interface is also shown on the band diagram. The C - V measurements consist in applying on top of the static gate bias voltage a small sinusoidal voltage with frequency f and amplitude of the order

of 30 mV. This small periodic gate voltage causes the bands and the surface potential in the semiconductor to periodically move up and down, causing the interface traps lying around the value of the surface potential to fill and empty. Only if the traps around the surface potential have a characteristic response time that is of the order of the measurement frequency f can they interact with the measurement ac signal and affect the total impedance of the MOS capacitor.

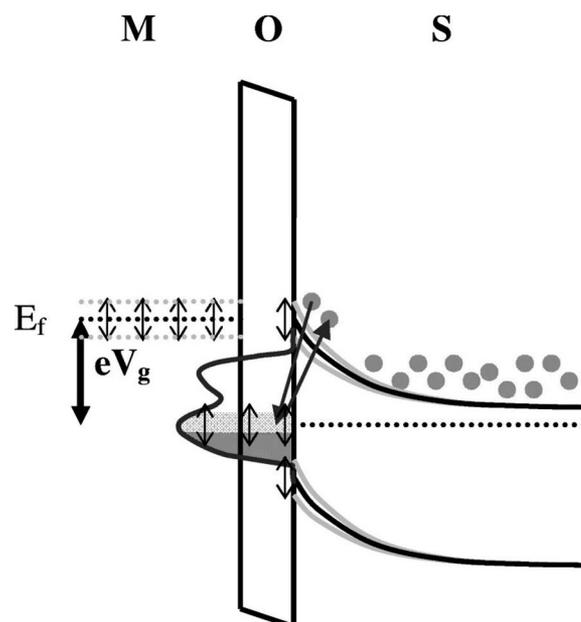


Figure 1. Band diagram of an n-type MOS structure with a bias voltage V_g applied between metal and semiconductor. A hypothetical interface state distribution is shown as well, with the interface traps filled up to the surface Fermi level (dark shaded region). A small ac voltage is applied on top of the gate bias, represented by the vertical arrows, which moves the semiconductor bands and surface Fermi level up and down, causing the traps within the oscillation amplitude (brighter shaded region) to periodically fill and empty. This filling and emptying of the interface traps allows for measurement of interface state distribution from C - V measurements.

* Electrochemical Society Active Member.

^z E-mail: Guy.Brammertz@imec.be

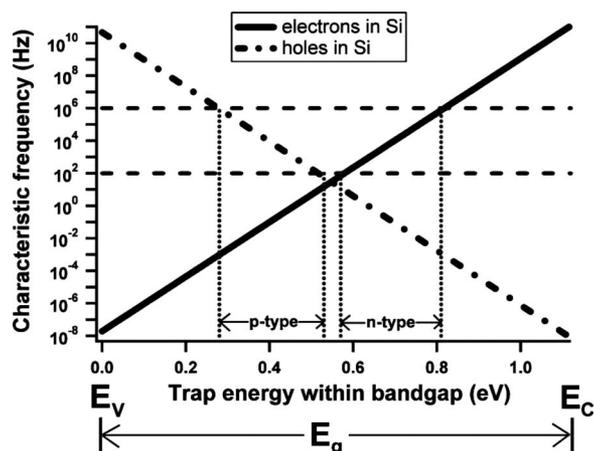


Figure 2. Characteristic emission frequencies of trapped charge carriers in Si at room temperature. The emission time for electrons (solid line) and holes (dashed-dotted line) is shown. The horizontal axis represents the position of the trapping state in the bandgap, where the origin of the axis is the valence band energy. The horizontal dashed lines show the usual frequency range of common LCR meters, 100 Hz to 1 MHz, representing the available measurement range. The vertical dotted lines represent the corresponding portions of the bandgap which can be measured with the mentioned measurement range.

Therefore, the characteristic times related to carrier trapping and emission are very important properties which should be studied in detail.

The characteristic time τ_e with which a trapped charge in a semiconductor is emitted from a trapping state of energy E_t can be determined from standard Fermi–Dirac statistics and is given by⁶

$$\tau_e = \tau_t \exp(\Delta E/kT) \quad [1]$$

where ΔE is the energy difference between the majority carrier band-edge energy and the trapping state energy E_t , k is the Boltzmann constant, T is the semiconductor temperature, and τ_t is the charge carrier trapping time constant, given by

$$\tau_t^{-1} = \sigma v_t N \quad [2]$$

here σ is the capture cross section of the trapping state, v_t is the thermal velocity of the majority charge carriers, and N is the density of states in the majority carrier band. From this characteristic emission time τ_e , one can derive the characteristic response frequency $f_e = 1/2\pi\tau_e$ of the corresponding trapping state. This equation shows that the characteristic emission frequency depends exponentially on the depth of the trapping state in the bandgap. The further the trap is away from the bandedge, the slower it will emit a trapped charge. Figure 2 shows the characteristic emission frequency of traps in Si as a function of the position of the trap in the bandgap. Both the emission times for electrons (solid line) and holes (dashed line) are shown in the figure. The valence band energy corresponds to the origin of the horizontal axis. Concerning the parameter values from Eq. 1, the thermal velocity and density of states are well-known and well-defined values for a specific semiconductor,⁷ whereas the trap capture cross section depends strongly on the nature of the trap.⁸ The capture cross section can take values varying from 10^{-12} to 10^{-20} cm². Even larger values than 10^{-12} cm² cannot be excluded. Nevertheless, the largest majority of trapping states has capture cross sections of the order of 10^{-14} cm²,⁸ which is the value that we adopted for the graph in Fig. 2. Possible deviations from this value will of course have an effect on the emission time, although the strongest dependency is still the exponential term. In the following, a capture cross section of 10^{-14} cm² is assumed in order to illustrate the effects of the characteristic emission time constant.

From Fig. 2 it becomes apparent that only small portions of the bandgap can be measured with common C - V measurement equipment, which usually measures in the frequency range

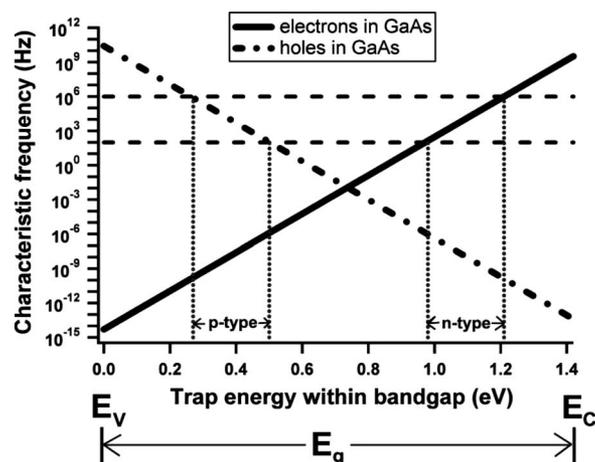


Figure 3. Characteristic emission frequencies of trapped charge carriers in GaAs at room temperature. The emission time for electrons (solid line) and holes (dashed-dotted line) is shown. The horizontal axis represents the position of the trapping state in the bandgap, where the origin of the axis is the valence band energy. The horizontal dashed lines show the usual frequency range of common LCR meters, 100 Hz to 1 MHz, representing the available measurement range. The vertical dotted lines represent the corresponding portions of the bandgap which can be measured with the mentioned measurement range.

100 Hz to 1 MHz. The traps at the majority carrier bandedges have characteristic frequencies which are way too fast to be measured with common C - V equipment, whereas the deeper traps are usually way too slow. In Si, nevertheless, we can see that the full midgap region can be measured with C - V measurements, the range 0.25–0.55 eV above the valence band with p-type MOS (p-MOS) capacitors and the range 0.55–0.8 eV above the valence band with n-type MOS (n-MOS) capacitors. Sweeping the gate bias voltage will sweep the position of the surface potential over the bandgap. When the surface potential meets a trap level with characteristic emission time equal to the measurement frequency, the capacitance and resistance of the traps at this particular position in the bandgap will be measured by the C - V equipment, thereby allowing the extraction of information on interface state density as a function of position in the bandgap. Whereas this works reasonably well for Si, where the full midgap region can be measured if one combines n- and p-type MOS measurements, this is not the case for higher bandgap materials, such as GaAs. Figure 3 shows the characteristic charge emission times from traps in the GaAs bandgap, assuming again a capture cross section equal to 10^{-14} cm². This time the situation is completely different from the Si case. Similar to Si, only small portions of the bandgap can be measured, but this time, because of the large bandgap of GaAs, the midgap trapping states cannot be measured, neither on p-type nor on n-type MOS capacitors. These midgap traps have characteristic emission frequencies on the order of 10^{-3} s⁻¹, which corresponds to characteristic times of the order of 1000 s. Once a charge carrier is trapped in such a midgap trap it can stay in the trap for several tens of minutes to hours. With our equipment that measures at frequencies of 100 Hz to 1 MHz, we will of course never be able to measure these extremely slow traps. We are completely blind to the trap density at these positions in the bandgap, as they lie completely out of the measurement range. They might just eventually show up in the measurements as hysteresis, which appears as the charge carriers very slowly detrap from the interface state, thereby reducing the charge at the interface.

One possible way to solve this problem and to still measure these GaAs midgap traps is to perform quasi-static C - V measurements but with extremely long integration times in excess of 1 s. A full quasi-static C - V measurement takes then about 1 h or longer. Such a low

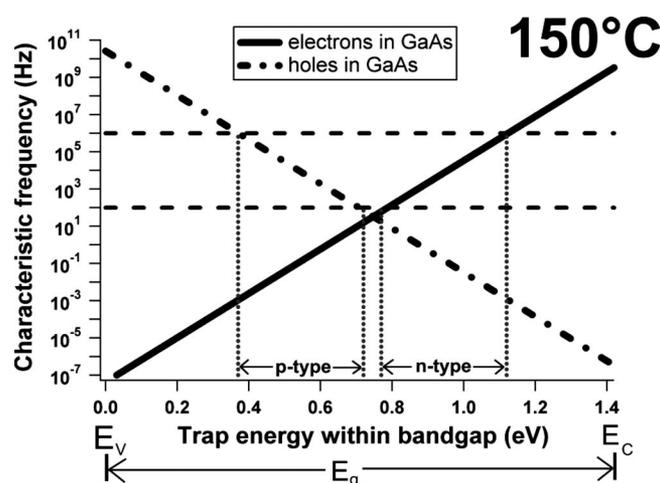


Figure 4. Characteristic emission frequencies of trapped charge carriers in GaAs at 150°C. The emission time for electrons (solid line) and holes (dashed-dotted line) is shown. The horizontal axis represents the position of the trapping state in the bandgap, where the origin of the axis is the valence band energy. The horizontal dashed lines show the usual frequency range of common LCR meters, 100 Hz to 1 MHz, representing the available measurement range. The vertical dotted lines represent the corresponding portions of the bandgap which can be measured with the mentioned measurement range.

voltage sweep rate will also allow the slow midgap traps to be emitted and captured by the measurement equipment. Nevertheless, such long measurements will require extremely low leakage currents, and successful measurements can only be made for very high quality gate dielectrics. If the voltage sweep rate for the quasi-static measurements is chosen to be faster than 1 mV/s, the midgap traps might not have enough time to be emitted and the measurement is again blind to the midgap traps, thereby artificially improving the measurement results. An additional comment regarding quasi-static measurements of GaAs MOS should be made here, as the appearance of an inversion response is a witness of a large midgap interface state density, being caused by the emission of trapped majority carriers from slow midgap trapping states. In a perfect GaAs MOS capacitor, inversion will never show up because of the extremely long minority carrier generation lifetimes, which are also strongly linked to the bandgap energy of the material.^{4,9} These minority carrier generation times will always be lower than typical leakage current times, which will drain away the minority carriers from the inverted surface.

In this contribution we focus on another possibility to measure the slow midgap states in GaAs, which is to thermally activate them with a more elevated temperature. The temperature in Eq. 1 gives us a handle on the emission time constants.^{3,4} Heating the semiconductor will strongly increase the characteristic emission frequencies. Figure 4 shows the characteristic charge emission times from traps in GaAs at a substrate temperature of 150°C, assuming again a capture cross section equal to 10^{-14} cm². The characteristic emission frequencies are now 4 orders of magnitude larger than at room temperature, and the situation is now similar to the Si case at room temperature, with the midgap traps having characteristic emission frequencies of the order of 100 Hz.

We therefore propose application of the conductance method for GaAs MOS at room temperature as well as at higher temperatures up to 150°C in order to be able to measure the interface trap distribution also around midgap energies. The conductance method⁵ relies on a measurement of the capacitance and the parallel conductance of the structure under testing (Fig. 5a). The measured values for capacitance C_m and conductance G_m contain all contributions from the measured MOS structure. The total MOS capacitor can be modeled by the diagram in Fig. 5c, showing the contributions from the oxide capacitance (C_{ox}), the capacitance of the depletion region

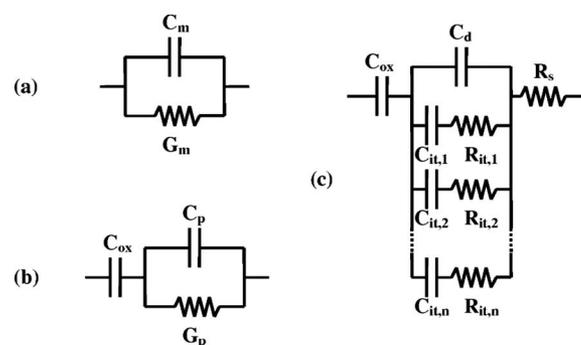


Figure 5. (a) Equivalent circuit of the capacitance (C_m) and parallel conductance (G_m) measured by the experimental equipment. (b) Equivalent circuit showing the oxide capacitance (C_{ox}) and the substrate capacitance (C_p) and parallel substrate conductance (G_p). (c) Equivalent circuit of the total MOS structure, showing the oxide capacitance, the depletion capacitance (C_d), the series resistance (R_s), and interface state capacitance ($C_{it,i}$) and resistance ($R_{it,i}$). The variation of the interface trap time constant $R_{it,i}C_{it,i}$ is represented by a series of n contributions in parallel with the depletion capacitance.

(C_d), the capacitances ($C_{it,i}$), and resistances ($R_{it,i}$) of the interface states of time constant $R_{it,i}C_{it,i}$, as well as the series resistance (R_s). The fact that the time constant varies strongly as a function of trap depth is modeled by putting a series of n trap capacitances and resistances in parallel. From the measured capacitance C_m and conductance G_m , one needs to extract the properties of the interface states. A first step to achieve this is to remove the effect of the oxide capacitance C_{ox} from the measured data by extracting the substrate conductance G_p (Fig. 5b) from the measured conductance G_m using the following equation⁵

$$G_p = \frac{G_m}{(G_m/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2} \quad [3]$$

It was shown that the maximum of $G_p/A\omega q$ as a function of measurement frequency f is proportional to the interface state density D_{it} at the position in the bandgap where the characteristic trap frequency is equal to the measurement frequency at which the maximum occurs⁵

$$D_{it}(V_g) \approx 2.5 \frac{(G_p)_{max}}{A\omega q} \quad [4]$$

Here A is the area of the MOS capacitor under testing, $\omega = 2\pi f$, and q is the charge of the majority charge carrier. Determining the maximum of $G_p/A\omega q$ as a function of frequency for different bias voltages, for which the device is in depletion, will provide us with a measure of the interface state density as a function of the position in the bandgap. This proportionality between D_{it} and $G_p/A\omega q$ holds only for interface state densities for which $G_p/\omega < C_{ox}$. For interface state densities where G_p/ω approaches C_{ox} , the value indicated by $G_p/A\omega q$ is only a lower bound of the true D_{it} .¹⁰

In principle, the conduction method relies on the extraction of the flatband voltage in order to position the interface state distribution in the bandgap relative to this flatband voltage position. One can then determine the capture cross section of the trap states. This flatband voltage extraction is nevertheless impossible for III-V devices with large interface state densities,¹⁰ so we have to rely on the assumption of a reasonable capture cross section if we want to position our interface state distribution in the bandgap. This leads to an uncertainty concerning the absolute position of the interface state positions in the bandgap. The error will be larger the further the real trap capture cross section is off with respect to our assumed value of 10^{-14} cm⁻².

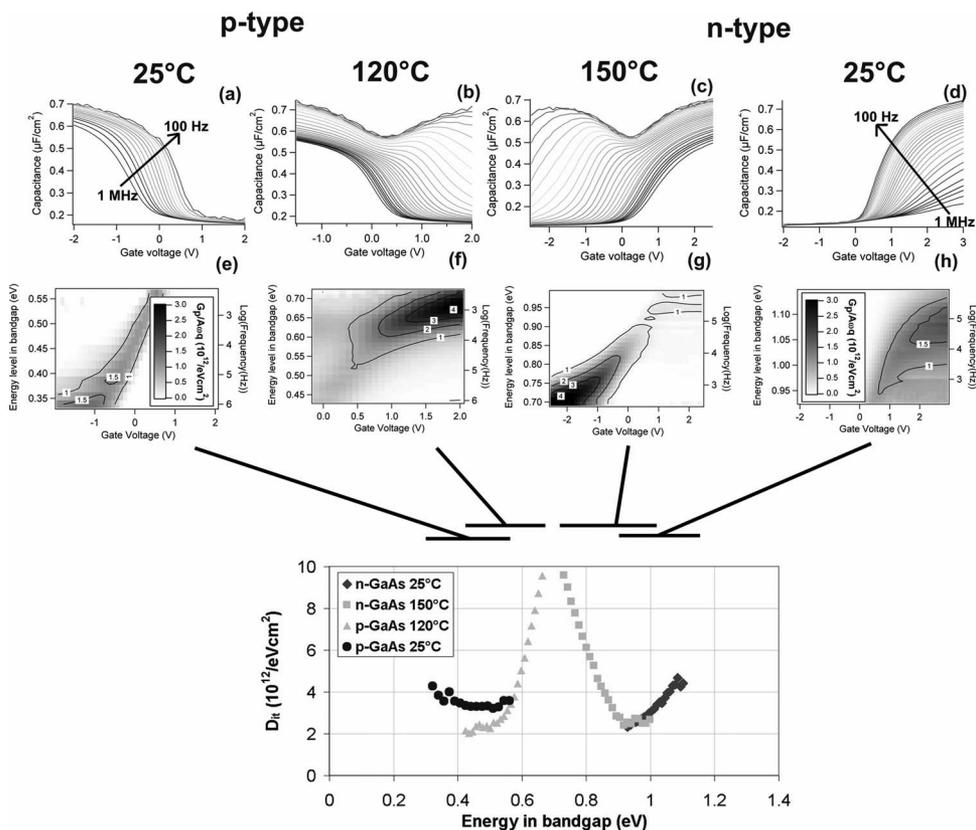


Figure 6. Capacitance– and conductance–voltage measurements on 200 μm diameter GaAs/Al₂O₃ MOS capacitors: (a) 25°C C - V curves of a p-type GaAs capacitor, (b) 120°C C - V curves of a p-type GaAs capacitor, (c) 150°C C - V curves of an n-type GaAs capacitor, (d) 25°C C - V curves of an n-type GaAs capacitor, (e) a 25°C $G_p/A\omega q$ map of a p-type GaAs capacitor, (f) 120°C $G_p/A\omega q$ map of a p-type GaAs capacitor, (g) 150°C $G_p/A\omega q$ map of an n-type GaAs capacitor, and (h) 25°C $G_p/A\omega q$ map of an n-type GaAs capacitor. The lower graph shows the GaAs–Al₂O₃ interface state distribution derived from the four conductance maps, the arrows indicating which measurement measures the interface state density in what portion of the bandgap.

Sample Preparation

Several GaAs samples were prepared on both $5 \times 10^{17} \text{ cm}^{-3}$ n-type doped substrates and on $5 \times 10^{17} \text{ cm}^{-3}$ p-type doped substrates. The In_{0.15}Ga_{0.85}As layers were deposited by metallorganic chemical vapor deposition and are 30 nm thick and also $5 \times 10^{17} \text{ cm}^{-3}$ n- and p-type doped. The HfO₂ and Al₂O₃ samples were treated with an HCl wet clean before being introduced into an ASM Pulsar atomic layer deposition reactor. Using alternating pulses of H₂O and trimethylaluminum or HfCl₄ as precursors, 10 nm of Al₂O₃ or HfO₂ were deposited at 300°C. The Gd₂O₃ samples were deposited by molecular beam epitaxy (MBE) by first preparing a 2×4 As stabilized surface by 400°C desorption of an amorphous As cap prepared in a III-V MBE reactor, followed by the evaporation of a Gd precursor in an atomic O atmosphere at 225°C. The back-side contact was formed using AuZn/Au or AuGe/Ni/Au multilayer deposition for p- or n-type, respectively, followed by a 30 s, 380°C forming gas anneal. On the front side Pt metal dots were deposited through a shadow mask.

Results

In order to get a good continuous picture of the movement of the surface potential and interface state distribution, we measured C - V curves with 25 frequencies varying logarithmically from 100 Hz to 1 MHz. Figure 6 shows all the C - V curves and $G_p/A\omega q$ as a function of frequency and bias voltage (conductance map) for the GaAs/Al₂O₃ samples. As explained in the previous section, for GaAs MOS interface characterization it is not sufficient to make room temperature measurements. For the characterization of the interface, 25 and 150°C measurements should be made on both n- and p-type MOS. Figure 6 shows the four different measurements. Every one of the four measurements probes a different region in the GaAs bandgap, as witnessed by the vertical axis of the conductance maps, which is directly expressed in bandgap energy. For clarity, the measurement frequency is shown on the right side axis of the conductance map. The bandgap energy is derived from the measurement

frequency through Eq. 1, assuming a capture cross section of 10^{-14} cm^{-2} . Deviations of the real capture cross section from this value will result in an energy shift of the features observed. We therefore have a relatively large uncertainty on the real energy position of the features we observe. Deep-level transient spectroscopy measurements are currently being made on these samples in order to determine the real value of the capture cross section. The four measurements show how the surface potential moves over the measurement range as the bias voltage is varied. What can be seen is how the conductance responses from different trap levels with different characteristic time constants are measured as the applied gate voltage sweeps the surface Fermi level over the bandgap. For the room temperature measurement of the p-type sample, the Fermi level can move over the full measurement range, as witnessed by the response which runs from about 0.3 eV above the valence band at $V_g = -1 \text{ V}$ to about 0.55 eV above the valence band at $V_g = 0.5 \text{ V}$. The high-temperature measurement shows a very large density of interface states around the mid-gap energy, nevertheless, which hinders the Fermi level from passing through this point. The interface state contribution becomes horizontal as a consequence, and large peaks in the depletion area of the MOS capacitor become visible which resemble an inversion response. Please note that it is very unlikely that this response is caused by minority carriers in GaAs. Simulations show that such a response can only be caused by minority carriers if the midgap trapping states have capture cross sections larger than 10^{-10} cm^{-2} , which are excessively large values. It is more likely that this response is indeed caused by a large midgap interface state peak. We are not able at the moment to make the distinction between the two experimentally, as this necessitates full conductance measurements on fully processed MOS field effect transistors,¹⁰ which we currently do not have available. This will be verified in the near future, though. Nevertheless, the fact that both n- and p-type GaAs have the surface Fermi level pinned at around midgap energies, as measured already uncountable times with all kinds of different surface configurations in the past 40 years,¹ makes

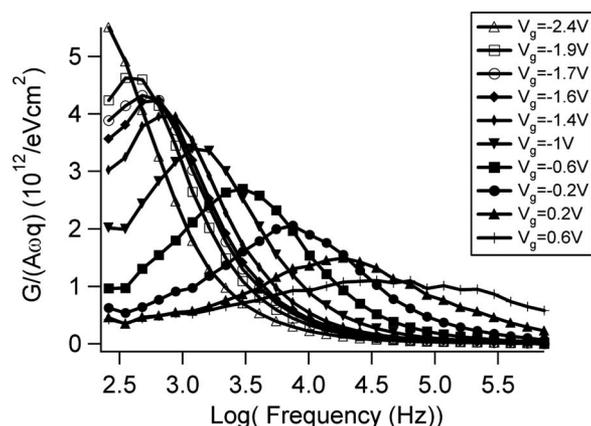


Figure 7. More standard G/ω vs ω plots which show a subset (selected bias voltages) of the data in the conductance map in Fig. 6g, representing the conductance data of the n-type GaAs–Al₂O₃ sample at a substrate temperature of 150°C. Variation of $G_p/A\omega q$ as a function of measurement frequency is shown for several bias voltages.

it very likely that the large peaks visible in the high-temperature C - V measurements are indeed majority carrier trap responses and not inversion responses.

A similar behavior can be seen in the 150°C measurements on the n-type sample, where a similar peak appears around midgap energies, which completely pins the Fermi level, i.e., blocks the movement of the Fermi level through this position. In order to help the reader understand the data in the conductance maps, Fig. 7 shows a subset (selected bias voltages) of the data in Fig. 6g in a more standard way of representing G/ω vs ω plots. This makes it clear that Fig. 6e-h represents many G/ω vs ω plots, plotted in a somewhat different way, which we believe to be a more intuitive representation as it directly allows the visualization of the surface potential movement as the bias voltage is varied. In the room temperature measurements on the n-type sample a somewhat smaller interface state peak, which blocks the passage of the Fermi level, can be identified at an energy of about 1.1 eV above the valence band. We suspect that a similar peak exists close to the valence band as well, which is not directly visible in Fig. 6, as it lies just slightly out of the measurement range. The onset of the peak can be identified though. By measuring the height of the conductance peak for every energy level (respectively, measurement frequency) of the conductance map and applying Eq. 4 we can determine the variation of interface state density over the bandgap of the semiconductor. Gathering all the data from the four conductance maps onto a single graph yields the interface state distribution as shown in the bottom of Fig. 6. In total, four different, rather localized interface state

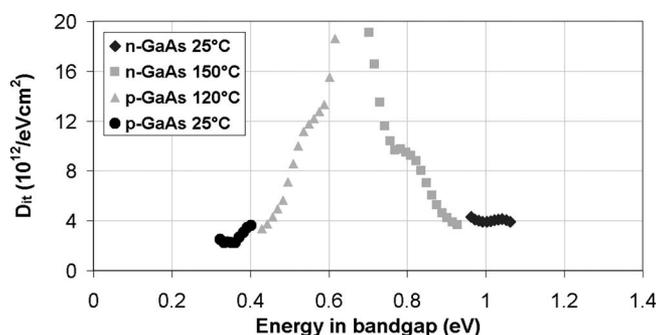


Figure 8. GaAs–Gd₂O₃ interface state distribution derived from four measurements made on both n- and p-type substrates at both low and high substrate temperature.

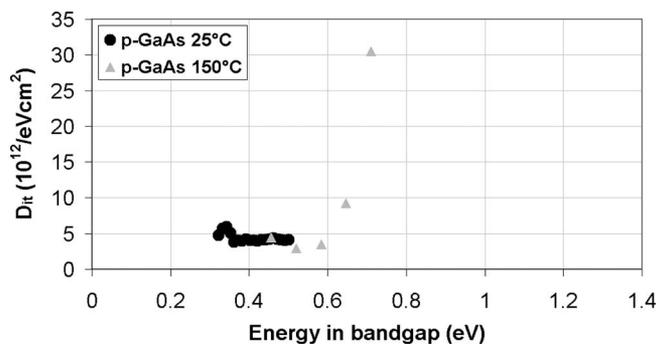


Figure 9. GaAs–HfO₂ interface state distribution derived from low and high substrate temperature C - V measurements on a p-type GaAs sample. In this case only five frequencies were measured at high temperature, leading to only five data points toward midgap energies.

peaks can be identified on top of a somewhat flat background: one hole trapping state at about 0.3 eV above the valence band, one hole trapping state at around midgap energy, one electron trapping state at around midgap energy, and one electron trapping state about 0.3 eV below the conduction band. The absolute height of the peaks cannot be derived from the measurements, as we are not able to move the Fermi level through the peaks and because the measured conductance is limited by the value of the oxide capacitance, as explained in the first section.

Figure 8 shows the interface state distribution as derived from similar measurements on GaAs/Gd₂O₃ samples, Fig. 9 shows D_{it} as measured on the GaAs/HfO₂ sample (unfortunately only p-type samples are currently available), and Fig. 10 is derived from In_{0.15}Ga_{0.85}As/Al₂O₃ samples. Although there are small differences visible in the exact number of interface states, the overall picture is in all cases the same and quite independent of the overlying oxide. It is therefore very likely that the defects are intrinsic GaAs defects, as proposed earlier in Ref. 2. Note that the interface state distribution as measured in this paper corresponds actually to the density distribution as proposed by the unified defect model (UDM) in Ref. 2, which also suggests a large hole trap peak at about 0.5 eV above the valence band and a large electron trap peak at about 0.75 eV above the valence band energy. This actually coincides with the two large peaks that we see in our measurements at around midgap energies. Please remember that we only assumed a value of the capture cross section, which leaves us with a rather large uncertainty on the exact energy position of the peaks in the bandgap. In addition to these two large peaks around midgap energies proposed in the UDM, we see two additional, much smaller peaks closer to the bandedges, which are actually the reason for the frequency dispersion observed in

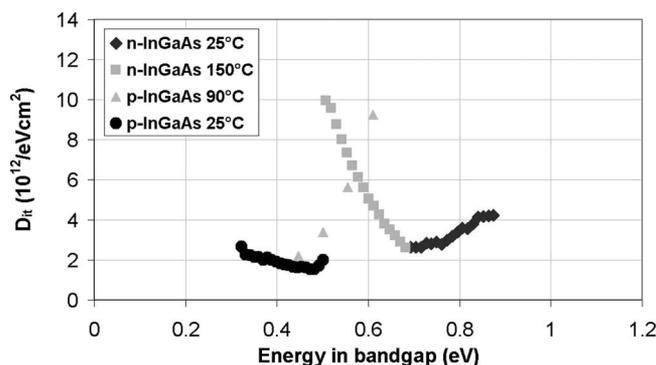


Figure 10. In_{0.15}Ga_{0.85}As–Al₂O₃ interface state distribution derived from four measurements made on both n- and p-type substrates at low and high substrate temperature.

room temperature C - V measurements because they lie pretty much exactly in the room temperature C - V measurement range. On the p-type sample the peak is slightly outside the measurement window, which explains the relatively better frequency dispersion observed on p-type samples as compared to n-type. We speculate that these interface state peaks close to the bandedges are derived from Ga (conduction band) or As (valence band) wave functions and would therefore be caused by As or Ga dangling bonds. This is yet to be confirmed at this point though.

A final observation which can be made concerning the $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ results is that the depth of the traps is actually not varied as In is introduced into the substrate material. Only the bands seem to approach each other, with the interface state peaks staying roughly at the same depth compared to the majority carrier band. The two peaks then actually start crossing each other, as observed in Fig. 9. Extracting these results to larger In contents would mean that at In concentrations close to 50%, the two very large peaks will actually shift into the valence and conduction bands, leaving a band-gap with a much smaller interface state density, which might be the reason for the inversion mode transistor results achieved on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ substrates.¹¹

Conclusions

We have shown how charge carrier trapping governs interface state characterization with C - V measurements. It was shown that 150°C C - V measurements are necessary in order to measure the very slow GaAs midgap trapping states. Conductance measurements on n- and p-type GaAs- Al_2O_3 , GaAs- HfO_2 , GaAs- Gd_2O_3 , and $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}-\text{Al}_2\text{O}_3$ MOS capacitors yield an interface state distribution which presents four large and rather localized peaks on top of a relatively flat interface state background. These peaks are one hole trap peak roughly 0.3 eV above the valence band energy, one hole trap peak around the midgap energy, one electron trap peak around

the midgap energy, and one electron trap peak around 0.3 eV below the conduction band energy. Whereas the midgap trapping states are likely caused by structural damage induced at the GaAs-amorphous oxide interface, in agreement with the UDM by Spicer et al.,² we speculate that the somewhat lower density trapping states close to the bandedges are caused by As or Ga dangling bonds.

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