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# 3-D integration of 10-GHz filter and CMOS receiver front-end

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# 3-D Integration of 10-GHz Filter and CMOS Receiver Front-End

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**Abstract**—A 10-GHz filter/receiver module is implemented in a novel 3-D integration technique suitable for RF and microwave circuits. The receiver designed and fabricated in a commercial 0.18- $\mu\text{m}$  CMOS process is integrated with embedded passive components fabricated on a high-resistivity Si substrate using a recently developed self-aligned wafer-level integration technology. Integration with the filter is achieved through bonding a high- $Q$  evanescent-mode cavity filter onto the silicon wafer using screen printable conductive epoxy. With adjustment of the input matching of the receiver integrated circuit by the embedded passives fabricated on the Si substrate, the return loss, conversion gain, and noise figure of the front-end receiver are improved. At RF frequency of 10.3 GHz and with an IF frequency of 50 MHz, the integrated front-end system achieves a conversion gain of 19 dB, and an overall noise figure of 10 dB. A fully integrated filter/receiver on an Si substrate that operates at microwave frequencies is demonstrated.

**Index Terms**—CMOS RF front-end, embedded passives, evanescent-mode cavity filter, heterogeneous integration, packaging, receiver.

## I. INTRODUCTION

THE EXPANDING wireless communication market demands RF systems with higher data rate, lower cost, and higher levels of integration than what is available today. While it is attractive to implement the entire system on a single chip to make the system compact, this leads to increased cost. The higher cost is mainly due to the integration of large area passive components such as inductors and capacitors on expensive Si or GaAs chips, as well as the requirement for heterogeneous integration. Integrated RF components suffer from degraded performance due to high loss and high dielectric constant of Si as the integration substrate. Some passive components, such as high- $Q$  RF inductors, large valued capacitors, high- $Q$  filters, and antennas are best integrated on the package rather

than the active chip. While passive devices demonstrate their best performance on the package, wafer-level batch fabrication of passive components and interconnects is still desired. Wafer-level integrated passives eliminate the assembly cost and reliability issues associated with hybrid packaging.

In standard Si technologies, the quality ( $Q$ ) factor of integrated spiral inductors is limited to 5–30 due to the inherent losses of low-resistivity Si substrate. While the  $Q$  of these passive components can be improved using unconventional fabrication technologies that are often not compatible with integrated circuit (IC) processing [1], [2], their size still remains large. Antennas and filters are other examples that do not operate optimally when integrated on silicon due to the fundamental trade-offs between size, loss in Si substrate, and performance [3]. If these passive components can be removed from the IC and yet tightly integrated with transistors, the area of the chip and, thus, the cost, can be significantly reduced. By implementing these passives on high-resistivity Si and/or low-loss dielectric substrates as the packaging media, better system performance may be achieved.

Current RF and microwave systems are implemented either in a system on a chip (SOC) approach where the entire system is integrated on one chip or in a system in a package (SIP) approach where various chips and passive components are flip chipped or wire bonded on a common packaging substrate such as a ceramic or a laminate, and recently, new packaging technologies such as redistributed chip packaging (RCP)<sup>1</sup> and integrated passive device (IPD) technology<sup>2</sup> have been introduced. We have recently developed a heterogeneous integration technology [i.e., self-aligned wafer-level integration technology (SAWLIT)] that combines batch fabrication capability, high interconnect density, high integration level, and compactness of the SOC approach, while system cost, time to market, and passive performance are comparable with the SIP approach [4], [5].

In this paper, we have utilized this unique integration approach to integrate a 10-GHz filter/receiver. A novel integration concept for RF and microwave receivers using a 3-D integration technology is demonstrated. This technology allows planar and nonplanar passive components to be compactly integrated with the IC, and which results in a potential impact on future implementations of RF and microwave systems. The receiver is designed and fabricated as a standalone chip in a commercial 0.18- $\mu\text{m}$  CMOS process. The chip is integrated inside an Si carrier substrate using a minute amount of polymers. Embedded

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<sup>1</sup>[Online]. Available: <http://www.freescale.com/webapp/sps/site/overview.jsp?nodeId=01210053720980>

<sup>2</sup>[Online]. Available: [http://www.sychip.com/PUB/6102\\_IPD\\_Brief\\_v1.6.pdf](http://www.sychip.com/PUB/6102_IPD_Brief_v1.6.pdf)

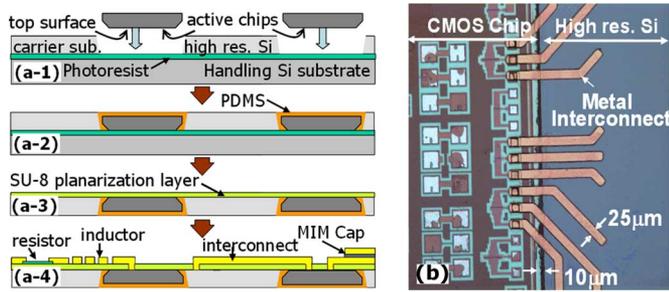


Fig. 1. (a) Step-by-step SAWLIT fabrication process. (a-1) Carrier substrate and disparate chips are placed on the handle substrate upside down. (a-2) PDMS is applied and polymerized to fill the gaps. (a-3) Handle substrate is detached and SU-8 is deposited on the top surface for planarization. (a-4) Standard microfabrication process is used to add high-density chip-to-package interconnects and embedded passives. (b) CMOS chip integrated inside high-resistivity Si. Interconnects as narrow as  $25\ \mu\text{m}$  are used, while the polymer gap is approximately  $10\ \mu\text{m}$ .

passive components and interconnects are added through a batch fabrication process. A high- $Q$  evanescent-mode cavity pre-select filter is then integrated on the Si carrier wafer and interconnected to the RF receiver. The filter is placed very close to the active circuit to prevent loss of signal power and demonstrates the use of the host silicon as an integration platform for cavity-based high- $Q$  components. The integration scheme presented has the benefit of dense integration of relatively high- $Q$  filters with Si circuitry. This integration technology can be utilized to implement integrated antennas, transmitter chips, and IF stages to make a tightly integrated RF transceiver system.

Section II presents the SAWLIT. Design and simulations of the 10-GHz CMOS IC are discussed in Section III, while design and measurement results of the high- $Q$  evanescent-mode cavity filter are discussed in Section IV. In Section V, the integration of the IC with embedded passive devices and the filter is presented and performance characterizations of the entire system are provided. Section VI summarizes the results obtained in this study.

## II. INTEGRATION TECHNOLOGY

The details of SAWLIT with high interconnect density and embedded passives are presented elsewhere [4], [5]. In SAWLIT, various heterogeneous chips are placed in a carrier substrate with a seamless transition between each chip and the substrate maintaining a flat surface for lithographic processes. In this integration scheme, instead of using wire bonds or flip-chip bumps to make a chip-to-package connection, lithographically defined interconnects with very narrow ( $\sim 25\ \mu\text{m}$ ) footprints, as shown in Fig. 1, are utilized. I/O pads on the chip with current dimensions of  $25\ \mu\text{m} \times 25\ \mu\text{m}$  occupy a smaller area than the pads for flip chip or wire bond (state-of-the-art  $35\ \mu\text{m} \times 35\ \mu\text{m}$ ).

Using SAWLIT, bulky passive components such as inductors and capacitors used in RF and mixed-signal circuits can be removed from the active chips and placed on the carrier substrate. By using a low-loss carrier substrate such as high-resistivity Si, quartz, or ceramics, the  $Q$  factor of the inductors or transmission lines can be improved, resulting in better performance of RF modules. At the same time, since the bulky inductors and

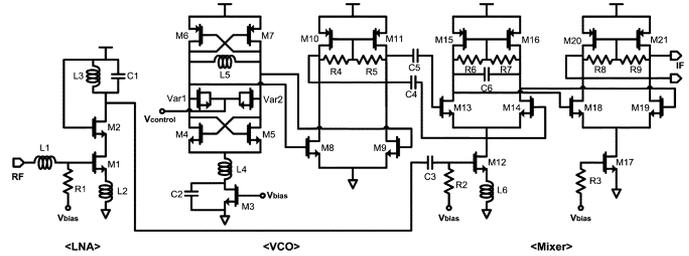


Fig. 2. Schematic of LNA, mixer, and VCO.

TABLE I  
PARAMETERS OF DEVICES

M1, M2	160 / 0.18	M13, M14	80 / 0.18
M3	960 / 0.6	M17	160 / 0.18
M4, M5	40 / 0.18	M18, M19	160 / 0.18
M6, M7	80 / 0.18	C2	18 pF
M8, M9	30 / 0.18	L4	0.78 nH
M12	80 / 0.18	L5	0.37 nH

capacitors are relocated from the active chip to the carrier substrate, the size of active RF chips are significantly reduced.

The SAWLIT integration process starts with etching a high-resistivity Si wafer with holes slightly larger than the chips to be integrated. The etch goes all the way through the wafer using a deep etch reactive ion etcher (DRIE). The size of the holes are approximately  $10\ \mu\text{m}$  larger on each side of the diced chips, allowing the chips to be self-positioned in the holes with a few micrometer misalignment. After etching, the wafer is attached to a handling substrate and, as shown in Fig. 1(a-1), diced chips are inserted in the gaps upside down. The gap is filled with poly-dimethyl-silicone (PDMS), as shown in Fig. 1(a-2). After PDMS polymerization, the carrier substrate and the chips are detached from the handling substrate and a  $6\text{-}\mu\text{m}$  SU-8 (a photo-curable polymer) is spun for planarization [see Fig. 1(a-3)]. Standard microfabrication steps including photolithography, etching, and liftoff are used to add chip-to-substrate interconnects and passive components. Fig. 1(b) shows a minimum trace width of  $25\text{-}\mu\text{m}$  interconnect lines and a gap of  $10\ \mu\text{m}$  between the chip and substrate achieved in this process.

## III. CIRCUIT DESIGN

The focal point of the SAWLIT process demonstration is a receiver circuit fabricated in six-metal  $0.18\text{-}\mu\text{m}$  CMOS technology (IBM 7RF). The front-end IC consists of a low-noise amplifier (LNA), a mixer with an IF buffer, and a voltage-controlled oscillator (VCO). The VCO also has a buffer to drive the mixer without degrading the performance. The design and performance of each of these are detailed below. The schematic of the circuit is shown in Fig. 2, and the values of components are shown in Table I.

### A. LNA Design

A cascode structure with inductive degeneration is used in the LNA, as shown in Fig. 2. The inductive degeneration allows easy input matching to a  $50\text{-}\Omega$  source, and helps increasing linearity. The isolation between the output and input

ports can be improved by the cascode structure. The size (width of  $160\ \mu\text{m}$ ) of transistors (M1 and M2) is decided by considering the tradeoff of minimum noise figure, gain, and power consumption. The transistor is also biased such that the transconductance is power efficient. As the gate bias voltage increases, the transconductance and, thus, the gain increase. However, after a certain gate bias voltage, the transconductance does not follow the increase of the bias current. As a result, the bias current of the transistor is decided at the point where the ratio of transconductance over power consumption is still high, although this bias point may not provide the maximum transconductance value. Since the inductors needed in high frequency are small, all of the inductors have inductance values less than  $1\ \text{nH}$ . The degeneration inductor is implemented with an inductive line, which also helps to reduce the chip area. Cadence simulation of the optimized LNA provides a gain of  $12\ \text{dB}$  and a noise figure of  $2.6\ \text{dB}$ .

### B. Mixer Design

A single balanced mixer with an optimized nMOS transistor width of  $80\ \mu\text{m}$  and inductive degeneration is implemented, as shown in Fig. 2. The inductive degeneration improves the linearity of the mixer, which was found to be the limiting factor of overall linearity from the simulations. For low IF operation, the load of the mixer is implemented with pMOS transistors with a width of  $300\ \mu\text{m}$ .  $2.4\text{-k}\Omega$  resistors provide the bias for these transistors. A differential IF buffer implemented with nMOS transistors with a width of  $160\ \mu\text{m}$  and pMOS active loads with a width of  $600\ \mu\text{m}$  are added to drive the  $50\text{-}\Omega$  output. Cadence simulation of the mixer shows a conversion gain of  $12\ \text{dB}$  at the RF frequency of  $10\ \text{GHz}$  and the IF frequency of  $50\ \text{MHz}$ .

### C. VCO Design

A detailed description of the VCO design and characterization is provided in [6]. The schematic of the VCO is also depicted in Fig. 2. A complementary cross-coupled differential structure is used to achieve higher transconductance for a given bias current, thus resulting in faster switching. The differential structure provides a symmetric output waveform [7]. The output of the VCO core is directly connected to the input of the buffer, which drives the mixer.

An nMOS current source transistor is placed below the cross-coupled nMOS pair to control the bias current of the VCO core. An inductor (L4) between the nMOS pair and current source and a capacitor (C4) in parallel with the current source eliminate the noise around the second harmonic, which results in reduced phase noise [8]. To increase the self-resonance frequency, a horseshoe-type one-turn inductor is used in the LC tank. This structure also provides symmetry to the two output nodes of the VCO core. The inductor is simulated with Sonnet electromagnetic (EM) simulation software. The expected inductance and  $Q$  factor at  $10\ \text{GHz}$  are  $0.38\ \text{nH}$  and  $15$ , respectively.

Besides the inductor of the tank, the varactor is also a key element in determining the performance of the VCO. In the technology used in this study, for small horseshoe-type inductors operating in X-band, the  $Q$  factor of the inductor increases as the frequency increases. On the other hand, the  $Q$  of the varactor decreases in the same frequency range. Thus, there is an

optimum value for the inductance and capacitance of the varactor in the tank circuit to achieve a maximum tank  $Q$  factor. In our configuration, two nMOS varactors are used in the tank for tuning purpose. The gate length of the varactor is kept at a minimum to maintain the capacitance and the  $Q$  factor at high frequency.

## IV. HIGH- $Q$ EVANESCENT-MODE CAVITY FILTER ON SILICON

A high- $Q$  pre-select filter prior to the LNA in the front-end receiver is critical to limiting the intermodulation induced through nonlinearities in the system. Adding the filter helps with distortion-free operation, while the total noise figure is degraded by the loss through the filter. The insertion loss of a filter is directly related to  $Q$  and inversely proportional to the bandwidth, therefore having the  $Q$  as high as possible is essential for making narrow pre-select filters. Planar distributed filters have  $Q$ 's limited to  $100\text{--}300$ . Larger components, such as high- $Q$  cavity-based resonators, can be vertically attached to the Si carrier substrate to achieve a compact 3-D integrated RF system.

Previous demonstrations of integrated cavity resonators and filters have utilized Si micromachining to define a cavity with and without capacitive loading posts [9], [10]. This process requires Au/Au thermo-compression bonding at  $350\ ^\circ\text{C}$  for  $1/2\ \text{h}$ , which is beyond the thermal budget of  $0.18\text{-}\mu\text{m}$  CMOS transistors. Alternatively, cavity resonators and filters have been demonstrated using a polymer layer by layer stereolithography fabrication [11]. This technique employed in this study allows for cavities integrated inside of multiple layers of polymer.

In general, the unloaded  $Q$  of a resonator is dependant on the dielectric, metal, and radiated losses. For an air-filled cavity, the dielectric and radiated losses are eliminated. The drawback of air-filled cavity filters is that they are large, typically the order of a half-wavelength. The size of the air-filled cavity can be reduced by loading it with a capacitive post, which causes the electric field to condense above the post without unduly changing the magnetic fields. This reduces the resonance frequency of the cavity without greatly sacrificing the unloaded  $Q$  factor of the resonator [12]. By varying the loading of the capacitive post, the size of the filter can be reduced, approaching lumped-element sizes at the cost of lower  $Q$ . Alternatively, the size can be maintained to be fairly large, keeping the distributed nature of the cavity and its high  $Q$ . The amount of capacitive loading, i.e., the distance between the capacitive post and the top of the cavity, determines this size versus  $Q$  tradeoff. In this tradeoff, an optimized filter size with relatively high  $Q$  can be identified, significantly higher than any planar resonator.

### A. Filter Design

As the first step, an empty rectangular cavity resonator is designed to resonate at a frequency higher than the targeted system frequency  $f_o = 10.3\ \text{GHz}$ . The unloaded cavity is  $11.48\ \text{mm} \times 11.48\ \text{mm} \times 3.1\ \text{mm}$  and has a center frequency of  $18.5\ \text{GHz}$  and an unloaded  $Q$  of  $3000$ . Cavity filters with unloaded  $Q$ 's of this magnitude have been recently demonstrated using the same fabrication technique [11]. A capacitive post is then included in the cavity that is  $3.0\ \text{mm} \times 3.0\ \text{mm} \times 2.36\ \text{mm}$ , covering  $6.8\%$  of the cavity top-down area, and is  $76\%$  of the height of the cavity. The choice of the height and the cavity area is not unique.

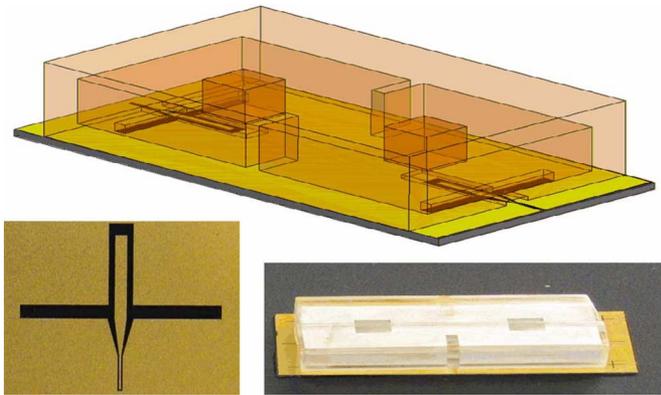


Fig. 3. Filter HFSS model, CPW feed, and fabricated filter. The dimensions of the filter are 25.2 mm  $\times$  15.1 mm  $\times$  5.4 mm.

Adding the capacitive post, the frequency is brought down to 10.3 GHz, which is a 44% reduction. The unloaded  $Q$  is reduced by 40% to 1800, while the area is reduced by 71%. While this is a large reduction in  $Q$ , it still represents a very high  $Q$  factor for a condensed package. The intercoupling is designed to give a bandwidth of 4%, representing a typical pre-select filtering requirement. Fig. 3 shows the designed filter, as well as the actual fabricated filter. The feed to the filter is a coplanar waveguide (CPW) to slot coupling with an open  $\lambda/4$  stub. This is designed to magnetic field couple into the evanescent-mode filter. The CPW line is designed to match the 150- $\mu\text{m}$  pitch 50- $\Omega$  measurement probes. The line is tapered from 125 to 520  $\mu\text{m}$  that extends into the slot, maintaining a 50- $\Omega$  impedance up to the slot. A magnetic field surrounds the current along the line and couples to the corresponding mode of the cavity filter through a 600- $\mu\text{m}$ -thick slot in the cavity walls. The slot is manually optimized with respect to the simulated return loss in order to achieve desired external coupling. The  $\lambda/4$  stub creates the necessary isolation for the dc biasing and is an alternative design to a more standard decoupling capacitor. Using a full-wave model Ansoft HFSS finite-element simulation with both cavities coupled together and both external feeds, the length of the stub and the size of the slot are manually optimized by looking at the behavior of the return loss and the flatness of the insertion loss in the passband. The optimization compensates for any parasitic effects introduced by the surrounding geometry. Final slot dimensions are 8.6 mm  $\times$  0.6 mm and the final stub length is 3.14 mm. The feed is shown in Fig. 3.

The filter is designed to be bonded on top of the feed and in order to prevent contact between the filter walls and the CPW feed line, air housing is designed above the feed. Multilayer features, such as this CPW housing, is easy to incorporate due to the layer-by-layer nature of the stereolithography process. The housing is chosen to be 1.5 mm, 460  $\mu\text{m}$  wider than the total width of the 520- $\mu\text{m}$  center line and the two 260- $\mu\text{m}$  gaps on either side. This housing equalizes both sides of the ground of the CPW line while shielding radiation.

### B. Filter Fabrication

The simulated filter is exported from HFSS into AUTOCAD using an ACIS file format. AUTOCAD has the ability to export into a stereolithography file format (.stl). That file is then sliced

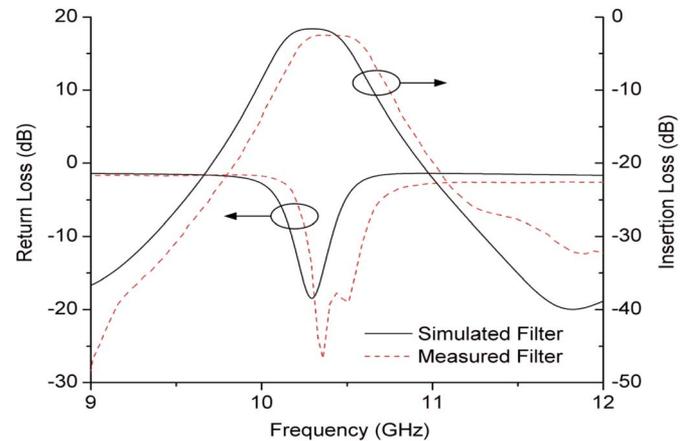


Fig. 4. Simulated and measured response of the filter.

into 50- $\mu\text{m}$  2-D layers, which are then built using a Viper HR stereolithography machine from 3DSystems. The entire filter and the corresponding support structure require 383 layers of cured polymer, which are rapidly deposited. The polymer filter needs to be built in two parts in order to metallize the internal cavities; the seam of the filter is chosen to be parallel to the direction of the current to avoid introducing any discontinuities. Once the filter is built, it is metallized with 500/4500  $\text{\AA}$  of sputtered Ti/Pt as adhesion seed layers and electroplated with 50- $\mu\text{m}$  copper.

### C. Filter Characterization

Filter measurements are performed on a filter bonded to an Si substrate with input and output feeding lines. The characterization is done using an Agilent 8510C network analyzer and Cascade probes with 150- $\mu\text{m}$  pitch. The filter is laid out horizontally for ease of probe testing on the same layer. Vertically integrated filters have also been previously demonstrated with much more compact size [11]. The measured results are compared to the simulated results in Fig. 4. The filters are in good agreement; the measured filter exhibits the same behavior as seen in simulation. The overall bandwidth is the same with a 1.35% frequency shift. The input matching of the filter is good over the entire passband, as can be seen from the 20-dB return loss. The insertion loss in the passband is constant and the slope of the attenuation in the stopband is as expected down to -40 dB/GHz. The slight variations in the isolation can be attributed to the measurement setup. The measured filter exhibits more broadband loss throughout the measured frequency range of the filter, both in the passband and stopband. This out-of-band loss indicates that there is overall more loss in the feeding to the cavity filter than the simulation. This additional 0.3-dB loss per feed could be due to variation in the low-temperature attachment material, slight plating variations over the 3-D cavity, or regions not readily coated using the relatively nonconformal sputtering technique. Even though sputtering is conformal by its nature, in this case, there is a large aspect ratio difference between the horizontal and vertical coating surfaces, which may result in a nonconformal coating of the seed layer for the electroplating.

There is a 1.35% frequency shift between theory and experiment that can be attributed to the sensitivity of the capacitive

loading post height; every 10- $\mu\text{m}$  change causes a 60-MHz frequency shift, determined from a series of HFSS full-wave model simulations. This correlates to an 11.6- $\mu\text{m}$  difference between the fabricated and simulated filter. This difference is caused by tolerances in the mesoscale fabrication employed for the multi-layer cavity filter. These tolerances in the filter size are due to variations in the copper thickness caused by high-current electroplating and inaccuracies in the beam size of the layer-by-layer stereolithography (75  $\mu\text{m}$ ). For probing purposes, the silicon feed designed for this experiment is 3.77-mm long, which adds to the total loss of the filter sample. This broadband loss is evident in the measured return loss in the stopband of the filter, as shown in Fig. 4. Accounting for the feed line length, the filter itself has only 0.64-dB insertion loss.

## V. INTEGRATION

Prior to the integration, the RF integrated circuit (RFIC) is characterized by on-chip probing. The reflection coefficient of the input RF port is measured with an Agilent 8722ES network analyzer, and measured  $S_{11}$  is  $-9.6$  dB at 10.3 GHz. An Agilent E4448A spectrum analyzer is used to measure the conversion gain of the front-end. For the LO frequency of 10.25 GHz, the maximum conversion gain is 21 dB, which is close to the simulated value of 24 dB in Cadence. This measurement is limited by the low end of the tuning range of the VCO. Since the parasitic capacitance and varactor capacitance are slightly overestimated, the measured center frequency of the VCO is higher than the target frequency of 10 GHz. The noise figure of the receiver is also measured based on the output noise power measurement technique [13]. A double-sideband noise figure of 9.4 dB at an RF frequency of 10.3 GHz and an IF frequency of 50 MHz is measured. This value is approximately 4 dB higher than the simulated value.

We have also fabricated and characterized the VCO block [6]. The output frequency, power, and phase noise of this block are measured with the Agilent E4448A spectrum analyzer equipped with a phase noise measurement option. A 180° hybrid coupler is used to convert the differential output signal of the VCO to the single-ended input to the spectrum analyzer. The phase noise of the VCO at 1-MHz offset from the carrier frequency at 10.3 GHz is measured to be  $-125.3$  dBc/Hz. A tuning range of 20.1% from 10.2 to 12.48 GHz is achieved. The VCO gain is estimated at 1 GHz/V.

Using SAWLIT, the CMOS IC is integrated with an input matching network embedded on a high-resistivity silicon carrier substrate with a size of 11.5 mm  $\times$  42 mm. Effective use of SAWLIT can move most of the passive components from the receiver chip to the carrier substrate without degrading performance. Only small inductors or capacitors that need to be very close to the active device (such as the inductor in the LC tank of the oscillator used here) may remain on the chip. Fig. 5(a) shows the layout of the package. The RF input port and interface to the filter are implemented with top metal.

In order to improve the input matching and overall conversion gain of the receiver front-end, a combination of a series inductor and a shunt capacitor is added to the input of the LNA. Fig. 5(b) shows the fabricated system. An aluminum layer that is fabricated below the SU-8 works as the bottom plate of the metal-insulator-metal (MIM) capacitor, while the top plate of

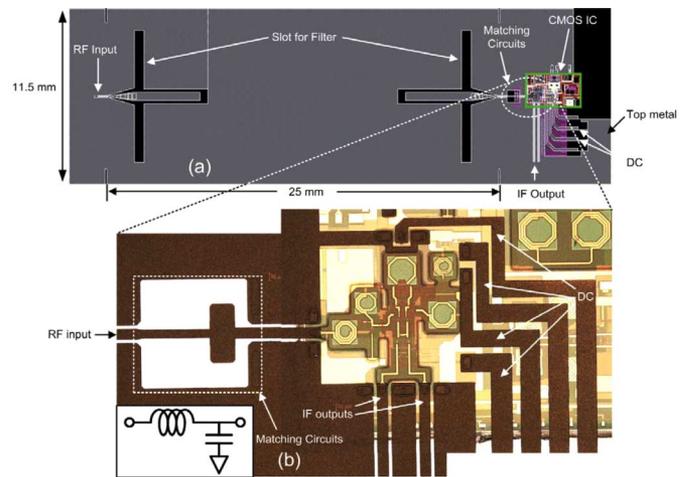


Fig. 5. (a) Layout for the integrated receiver. (b) Integration of the 10-GHz CMOS receiver with embedded passive components using SAWLIT.

the capacitor is implemented using the Au interconnect metal. The metal coverage over the PDMS is very smooth due to the SU-8 planarizing layer used in this technology.

By adding the embedded passives, namely, a series inductor (0.6 nH) and shunt capacitor (0.28 pF), the input matching at 10.3 GHz improves from  $-9.6$  to  $-26$  dB. The conversion gain at 10.3-GHz input RF frequency improves from 21 to 23 dB, while the double-sideband noise figure of the receiver improves slightly from 9.4 to 9.0 dB at 10.3 GHz.

After adding the embedded components, the Si substrate is bonded with the filter using 118-09A/B-187 screen printable conductive adhesive from Creative Materials, Tyngsboro, MA. This epoxy material is loaded with 85% silver, has a conductivity of  $2 \times 10^6$  S/m, and is screen printed on the silicon feed and aligned using a FINEPLACER A4 "PICO" pick-and-place system. The epoxy is then cured at room temperature. The conductive adhesive provides both a solid connection between the ground plane on the silicon and the metallized filter, and a solid mechanical bond between the two dissimilar materials. The low-temperature conductive epoxy with relatively high loss can be used since the connection between the Si carrier wafer and copper-plated polymer is over a broad area and the feed is designed to not have a large current density over any one location. The feed current density on the gold signal line of the carrier wafer feed is six orders of magnitude greater than the current density at the epoxy-gold junction. The 3-D fabrication allows for the high-Q cavity to be removed from the high-loss connection, greatly reducing the effect of the low-temperature attachment to the silicon host. The low-temperature processing allows for post placement of the cavities on Si, while maintaining high-Q performance.

Fig. 6 shows the final package. The simulated and measured conversion gains of the receiver before integration, with the embedded passives, and with the embedded passives and filter are shown in Fig. 7. The measurement results are close to the simulation results with 1.5–3-dB difference at the RF frequency of 10.3 GHz. The conversion gain improves by 2 dB when the embedded passives are integrated with the chip and decreases to approximately 19 dB at 10.3 GHz once the filter is added. The extra loss is

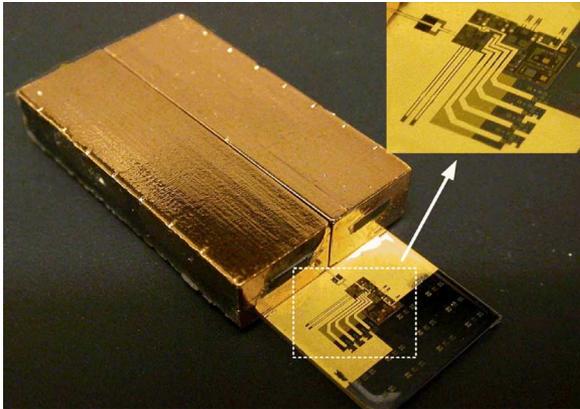


Fig. 6. Final front-end package.

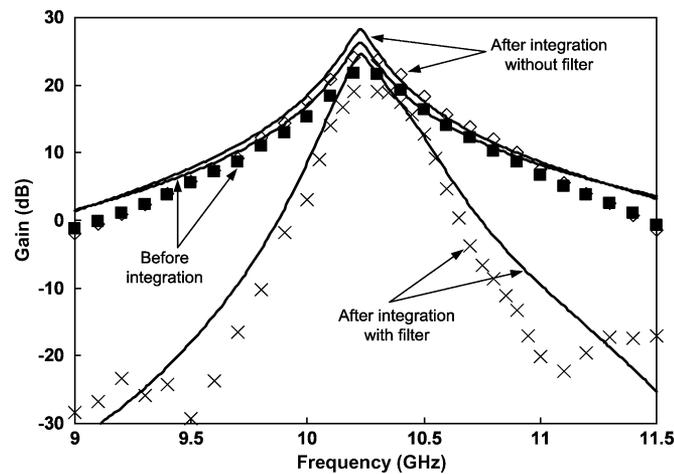


Fig. 7. Simulated and measured conversion gain of the IC and package (solid lines: simulation results; points: measured results).

due to slight loss in the filter and 1.2-mm CPW lines connecting filter to its two ports, as well as the slight frequency shift between the filter and the receiver, which happens to level off the gain peak of the response. The slope of the out-of-band conversion gain for the filter/receiver module is approximately  $-60$  dB/GHz, which demonstrates the isolation characteristic of the pre-select filter and tuned receiver from out-of-band interferers. The rejection is better than 40 dB at 6% away from the passband.

The simulated and measured noise figure of the IC before and after integrating embedded passives and with the filter and embedded passives are shown in Fig. 8. The simulation and measurement results have 2.2–4-dB difference at the RF frequency of 10.3 GHz. At the passband, the measured noise figure is between 9–10 dB. It is increased by 1–1.5 dB at the passband after integrated with the filter due to the insertion loss of the filter. At the stopband, the noise figure significantly increases due to the rejection of the filter. The separately fabricated LNA shows a measured noise figure of 5.5 dB. The high noise figure of the receiver is attributed partially to the difference between the actual transistor and the BSIM3v3 transistor model that does not include the induced gate noise. Additionally, the parasitic capacitance seen at the source of the cascode transistor is partially responsible for increase in the noise figure [14].

Fig. 9 depicts the input third-order intercept point (IIP3) of the IC before and after integration with the embedded passives

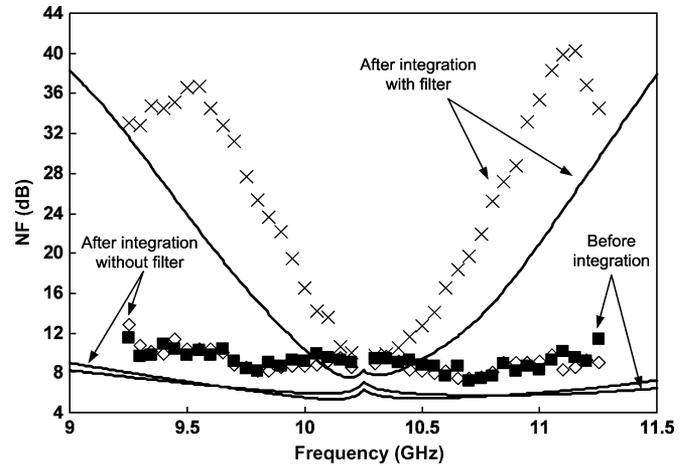


Fig. 8. Simulated and measured noise figure of the IC and package (solid lines: simulation results; points: measured results).

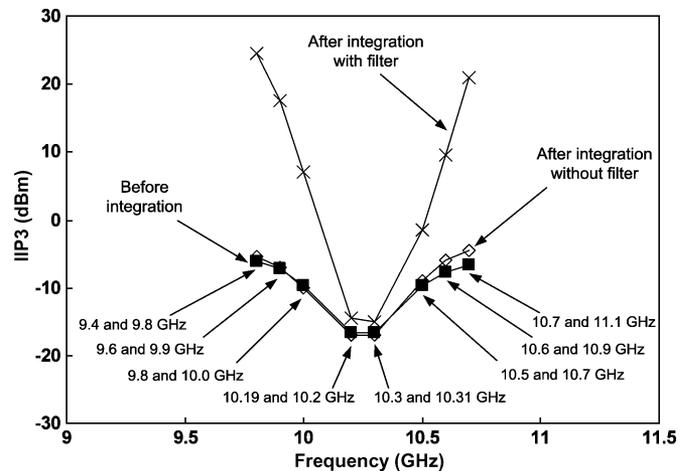


Fig. 9. Measured IIP3 of the IC and package.

TABLE II  
PERFORMANCE OF FRONT-END PACKAGE

Power Supply	2.2 V
LNA and Mixer power consumption	42 mW
VCO power consumption	50 mW
RF frequency	10.3 GHz
Conversion gain	19 dB
Input referred 1 dB compression point	-25.5 dBm
VCO Tuning range	10.2 ~ 10.48 GHz
Phase noise of VCO at 1MHz offset	-125.3 dBc/Hz
IC technology	0.18 $\mu$ m CMOS

and the filter. To measure the IIP3 at a local oscillator (LO) frequency of 10.25 GHz, two different tones are selected such that the third-order intermodulation falls on 10.2 GHz when the two tones are lower than LO, and 10.3 GHz when the two tones are higher than LO frequency. Due to the rejection of the filter, the third-order intermodulation is significantly reduced at the stopband, implying the advantage of adding a pre-select filter to the receiver.

The performance of the front-end package is summarized in Table II. Overall, the integration of the chip with an embedded input matching network integrated on the carrier substrate have

resulted in better input matching, higher gain, and better noise figure. Once the filter is added to this combination, the conversion gain and noise figure have slightly degraded, but the linearity is improved due to the rejection of out-of-band interferers by the pre-select filter.

## VI. SUMMARY AND CONCLUSION

SAWLIT is a wafer-level integration technique, which provides the flexibility of hybrid circuit/heterogeneous design with the integration density of a planar circuit (SOC). By placing the passive components on the carrier substrate, SAWLIT allows the designer to modify the passive components of the design without changing the active chips, reducing design cycle time while allowing for optimal performance. The use of a coplanar host substrate in SAWLIT allows for the integration of passives alongside the circuit, as well as provides a platform for 3-D integration of much higher quality components, such as the high- $Q$  filter demonstrated herein and antenna elements. Although the high-resistivity Si wafers are more expensive than CMOS grade Si wafers, the cost per unit area of the high-resistivity carrier wafer is considerably less than that of the fabricated IC. By relocating bulky passive components from the IC to the carrier wafer, the size of the IC and the cost of the system are significantly reduced. Additionally, the integration technology is a batch fabrication process that allows many modules to be integrated at the same time, resulting in further cost reduction compared to standard SOP/SIP implementations. In this study, a fully integrated 10-GHz receiver with preselect filtering is used as a vehicle to demonstrate the integration technology. With the adjustment of the input matching of the receiver IC by utilizing the embedded passives fabricated on the Si substrate, the return loss, conversion gain, and noise figure of the front-end receiver have been improved. A high- $Q$  evanescent-mode filter has been demonstrated on a silicon carrier wafer and is integrated with the 10-GHz RF front-end. The fabricated bandpass filter matches simulation well, with a bandwidth of 4% and a total insertion loss of 0.64 dB. The pre-select filter, embedded passives, and CMOS receiver are all integrated on an Si carrier substrate to show the possibility of a compact integrated multilayer RF system.

For the first time, an  $X$ -band CMOS RF front-end with embedded passive components and a high- $Q$  pre-select cavity filter are tightly integrated on an Si wafer. Using the integration technologies discussed in this study, RF and microwave systems can be tightly integrated on a single Si substrate to achieve minimum loss and maximum performance. The fact that the integration technology allows one to integrate most of the passive components after the active chips are separately fabricated translates into smaller and less expensive active chips compared to standard designs. The integration of high- $Q$  passive components including cavity filters, which is not possible on the SOC approach, combined with the tight integration through SAWLIT, which results in very small interconnect loss, as opposed to the SIP approach, results in low-loss high-performance system functions unique to this technology.

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