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# Electrical Characterization of NlPlN Structuresin 6H-Sic

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#### **CHAPTER 1- INTRODUCTION**

# 1.1 Need for High Operation Temperature Semiconductor

In recent years, the need for electronic devices capable of prolonged high temperature operation has increased. Possible applications include but are not limited to instrumentation within engines, space platforms, satellites, deep well drilling instrumentation, and nuclear reactor instrumentation and control as well as military applications. In some of these instances operating temperatures in excess of 850 K can be reached. This is well beyond the maximum operating temperature of 600 K for Si devices where maximum temperature is the temperature above which the semiconductor becomes intrinsic [1,2,3].

Looking at GaAs, the material presently used for applications beyond the temperature scope of Si, we see that it's maximum operating temperature is around 760 K. Thus the limitations of both Si and GaAs are well below the desired operation temperature of 850 K. This fact has helped to instigate the search for and development of higher temperature semiconducting materials, one of which is silicon carbide. The larger the **bandgap** of the semiconductor the higher the maximum operating temperature. Taking this into consideration, the maximum operating temperature of SiC can be obtained relative to Si by multiplying the maximum operating temperature of silicon (600 K) by the ratio of the bandgaps. By doing this, maximum operation temperatures of 1200 K and

Table **1.1** Comparison of properties of semiconducting materials. From references [2, **4**].

Material	Bandgap (eV)	Maximum Operating Temp °C	Physical Stability	Carrier Mobility	Thermal Conduct- ivity	Break- down Field
Si	1.1	327	Good	Good	Good	Good
GaAs	1.4	487	Fair	Excellent	Fair	Good
GaP	2.3	875	Fair	Fair	Fair	Good
β-SiC	2.2	927	Excellent	Fair	Very Good	Excellent
6H-SiC	2.9	1307	Excellent	Fair	<b>Very</b> Good	Excellent
Diamond	5.5	1100	Very Good	Good(?)	Excellent	Excellent

1580 K are obtained for β-SiC and 6H-SiC. Another important property of SiC is that it is a very stable ceramic up to temperatures of 2073 K [2,4]. Table 1.1 shows a comparison between silicon carbide and other potential candidates for high temperature semiconducting material. Also included in the comparison is silicon. Diamond goes through a phase change at 1100 °C resulting in a maximum operating temperature lower than that of 6H-SiC.

At this point it is worthwhile to mention an unusual property of SiC. It has a crystal structure that exhibits a form of one dimensional polymorphism called polytypism. SiC has many polytypes differing from one another only in the stacking layers of Si and C atoms. The two most common are  $\beta$ -SiC which is a cubic structure and 6H-SiC which has a hexagonal crystal structure.[2] These two crystal structures have different electrical properties. 6H-SiC has a bandgap of 2.9 eV while  $\beta$ -SiC has a bandgap of 2.2 eV, thus the difference in maximum operation temperatures given previously.

With all the advantages seen in table 1 for SiC, one would wonder about lack of incorporation of SiC technology into electronic systems. The main reason for this void has been the lack of SiC single crystal substrates of suitable size and quality for device fabrication purposes.

# 1.2 Emergence of High Quality SiC Substrates

Early SiC research was done on crystals that were a by-product of the industrial sublimation process for making sandpaper grit in which SiC is formed at 2500 °C by the reaction of silica and coke. In 1955 Lely developed a laboratory version of this industrial sublimation process, suitably called the Lely process. He was able to produce rather pure SiC crystals. This fueled research

into development of SiC semiconductor devices during the sixties. By the seventies the Lely process had not progressed to the point where large-area high quality reproducible crystals could be grown. It could still only produce small irregular-shaped SiC crystals, and work on SiC declined [4].

As mentioned earlier, the need in recent years for electronic devices capable of prolonged high temperature operation has helped to breathe new life into SiC research. During the 1980's much work was done in growing 3C-SiC on single-crystal Si substrates, but these films were unsuitable for device fabrication purposes because of a large defect density caused by the 20% lattice mismatch between SiC and Si. Focus turned to the development of a process known as the modified sublimation process. From it, large-single crystal SiC boules are grown from which wafers are sliced. This modified sublimation process was pioneered by Tairov and Tsvetkov in Russia in 1978. The outline of the process is as follows. A SiC seed crystal is located at one end of the cylindrical growth cavity and upon it nucleation takes place. A temperature gradient is established across the growth cavity with the polycrystalline SiC at 2700 K and seed crystal at 2500 K. The SiC sublimes from the polycrystalline material and condenses onto the seed crystal. The growth takes place in an atmosphere of argon at 200 Pa at rates of up to 4 mm/h [2].

Cree Research, Inc has developed processes for bulk and epitaxial growth, and can now produce 1-inch diameter 6H-SiC of high electrical quality. The study of n-i-p-i-n capacitors built on this material is the basis of this report.

#### CHAPTER 2 - N-I-P-I-N CAPACITOR THEORY

#### 2.1 Introduction

This chapter deals with a storage capacitor in SiC that could possibly be incorporated into a SiC DRAM cell. The main issue consists of the theoretical storage time of the capacitor and its limiting factors. The capacitors under study are not MOS devices as seen in Si technologies, but are bipolar structures similar to those currently under study in GaAs and AlGaAs where the depletion regions of two reverse biased pn-junctions are used to store charge [5-9].

## 2.2 p-i-n Diode

The SiC structures to be studied in this report are two back to back p-i-n diodes. The p-i-n diodes differ from a pn diode in that there is a thin undoped intrinsic layer inserted between the p and n regions of the diode. This intrinsic region lowers the magnitude of the electric field within the depletion region.

# 2.2.1 p-i-n Diode Electrostatics

The charge stored on a p-i-n junction capacitor is equal to the ionized dopant sites uncovered by the increased depletion region width from equilibrium.

$$Q = qN_A[x_p - x_{po}] = qN_D[x_n - x_{no}] = q\frac{N_AN_D}{N_A + N_D}[W - W_o]$$
(2.1)

where Q is the amount of charge stored per unit area,  $N_A$  and  $N_D$  are the acceptor and donor concentrations, W,  $x_p$ , and  $x_n$  are the reverse bias depletion widths, and  $W_0$ ,  $x_{po}$ , and  $x_{no}$  are the equilibrium depletion widths. It can be seen from (2.1)that an expression for the depletion widths is needed in order to obtain the charge stored by a p-i-n junction .

# **2.2.2** Development of Expressions for W, $x_p$ , and $x_n$

#### 2.2.2.1 Electric Fields

Figure 2.1 shows the basic electrostatic parameters of a pin junction. Figure 2.2 displays the band diagram for a p-i-n junction with a reverse bias  $V_A = V_R$  applied across it. The electrostatics of this device can be obtained by first considering Poisson's equation [10]:

$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\epsilon_s} = \frac{q}{\epsilon_s} [p - n + N_D - N_A]$$
 (2.2)

where  $\boldsymbol{\mathcal{E}}$  is the electric field, n and p are the hole and electron concentrations respectively, and  $\boldsymbol{\in_s}$  is the semiconductor dielectric constant.

Let x=0 be the metallurgical junction between the i and n regions. Let region I be the depletion region contained within the n-doped region of the diode. In this depletion region  $n=p=N_A=0$ , therefore Poisson's equation becomes:

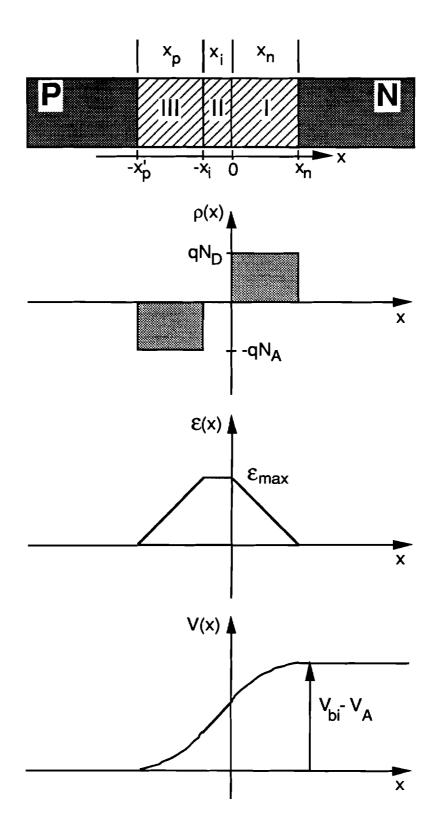


Figure 2.1 Basic electrostatics of a p-i-n junction.

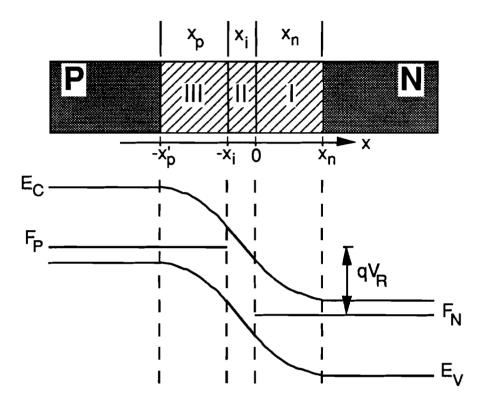


Figure 2.2 Band diagram for a reverse biased p-i-n diode.

$$\frac{\mathrm{d}\mathbf{\mathcal{E}}}{\mathrm{dx}} = \frac{\mathrm{q}}{\mathrm{\epsilon}_{s}} \,\mathrm{N}_{\mathrm{D}} \tag{2.3}$$

The above equation can be evaluated using the boundary condition that the electric field is equal to zero in the bulk.

$$\int_{\mathcal{E}(x)}^{0} d\mathcal{E} = \int_{x}^{x_{n}} \frac{q}{\in s} N_{D} dx$$
(2.4)

and thus:

$$\mathcal{E}(x) = -\frac{q}{\epsilon_s} N_D(x_n - x) \qquad 0 \le x \le x_n$$
 (2.5)

Since region II is undoped, the following is obtained:

$$\frac{\mathrm{d}\mathbf{\mathcal{E}}}{\mathrm{dx}} = 0 \tag{2.6}$$

Realizing that the electric field must be continuous at x=0, the above equation can be solved using the boundary condition:

$$\mathcal{E}(0) = -\frac{q}{\epsilon_s} N_D x_n \tag{2.7}$$

to give:

$$\mathcal{E}(x) = -\frac{q}{\epsilon_s} N_D x_n \qquad -x_i \le x \le 0$$
 (2.8)

Considering region III:

$$\frac{d\mathcal{E}}{dx} = -\frac{q}{\epsilon_s} N_A \tag{2.9}$$

Using the boundary condition that the electric field is equal to zero in the bulk,  $(x < -x'_p)$ , (2.9) can be solved to get:

$$\mathbf{E}(x) = -\frac{q}{\epsilon_s} N_A(x + x'_p) \qquad -x'_p \le x \le -x_i$$
 (2.10)

#### 2.2.2.2 Potential

Using the relation:

$$\frac{dV}{dx} = -\mathcal{E} \tag{2.11}$$

and (2.5), (2.8), and (2.10), the potential drop across each of the regions in Figure 2.1 can be obtained. These are:

$$V_{I} = \frac{qN_{D}}{2 \in s} x_{n}^{2} \qquad 0 \le x \le x_{n}$$

$$(2.12)$$

$$V_{II} = \frac{qN_D}{\epsilon_s} x_n x_i \qquad -x_i \le x \le 0$$
 (2.13)

$$V_{III} = \frac{qN_A}{2 \in s} x_p^2 \qquad -x'_p \le x \le -x_i$$
 (2.14)

# 2.2.2.3 Relation Between $x_p$ and $x_n$ (Charge Neutrality)

A direct relationship between the depletion widths  $x_p$  and  $x_n$  as defined in Figure 2.1 can easily be obtained. Since there is no sheet charge at  $x=-x_i$  the electric field must be continuous at this point. Taking this into consideration, (2.8) and (2.10) can be evaluated at  $x=-x_i$  and set equal to each other to obtain:

$$N_D x_n = N_A (-x_i + x'_p) = N_A x_p$$
 (2.15)

Therefore:

$$x_{p} = \frac{N_{D}}{N_{A}} x_{n} \tag{2.16}$$

giving a direct correlation between  $\mathbf{x}_{\mathbf{p}}$  and  $\mathbf{x}_{\mathbf{n}}$ .

# 2.2.2.4 Expressions for $\mathbf{x_n}$ and Total Depletion Width W

Using (2.16), (2.14) can be rewritten as:

$$V_{III} = \frac{qN_A}{2 \in s} \left[ \frac{N_D}{N_A} x_n \right]^2 \tag{2.17}$$

Realizing that the sum of the potential drops across the diode is equal to the built in potential  $V_{bi}$  minus the applied bias  $V_{A}$ , the following is obtained:

$$V_{I} + V_{II} + V_{III} = V_{bi} - V_{A}$$
 (2.18)

Next, substituting (2.12), (2.13), and (2.17) into (2.18):

$$\frac{qN_D}{2\in s}x_n^2 + \frac{qN_D}{\in s}x_nx_i + \frac{qN_A}{2\in s}\left[\frac{N_D}{N_A}x_n\right]^2 = V_{bi} - V_A$$
(2.19)

Rewriting (2.19):

$$\frac{qN_{D}}{2 \in s} \left[ \left[ 1 + \frac{N_{D}}{N_{A}} \right] x_{n}^{2} + 2x_{i}x_{n} + \frac{2 \in s}{qN_{D}} \left[ V_{A} - V_{bi} \right] \right] = 0$$
(2.20)

The above quadratic equation can easily be solved for  $\boldsymbol{x}_n$  to give:

$$x_{n} = \frac{-x_{i} + \left[x_{i}^{2} - \frac{2 \in s}{q N_{D}} \left[1 + \frac{N_{D}}{N_{A}}\right] \left[V_{A} - V_{bi}\right]^{\frac{1}{2}}}{1 + \frac{N_{D}}{N_{A}}}$$
(2.21)

 $\mathbf{x}_{\mathbf{p}}$  can now easily be obtained from (2.16) and (2.21) if needed.

The total depletion width, W, is given by:

$$W = X_n + X_i + X_p \tag{2.22}$$

Using (2.16) and (2.21), (2.22) can be rewritten as:

$$W = \left[x_i^2 - \frac{2 \in s}{qN_D} \left[1 + \frac{N_D}{N_A}\right] \left[V_A - V_{bi}\right]^{\frac{1}{2}}$$
(2.23)

#### 2.2.3 Built in Potential V<sub>bi</sub>

If a semiconductor is **non-degenerately** doped then the built in potential of the p-n junction is **easily** obtained from the **relation [10]**:

$$V_{bi} = \frac{kT}{q} \ln \left[ \frac{N_D N_A}{n_i^2} \right]$$
 (2.24)

However, computation of  $V_{bi}$  is more complicated if the semiconductor is degenerately doped. For this case, the Fermi level is contained within 3kT of either the conduction or valence band edge. The built in potential is given by the relation:

$$V_{bi} = \frac{1}{q} [E_G + kT[\eta_V + \eta_C]]$$
 (2.25)

where E<sub>G</sub> is the bandgap of the semiconductor and [11,121

$$\eta = \frac{\ln \left[u\right]}{1 - u^2} + \frac{\left[3\sqrt{\pi} \, \frac{u}{4}\right]^{\frac{2}{3}}}{1 + \left[0.24 + 1.08\left[3\sqrt{\pi} \, \frac{u}{4}\right]^{\frac{2}{3}}\right]^{-2}}$$
(2.26)

 $\eta_V$  is calculated by setting  $u = N_A / N_V$  and  $\eta_C$  is calculated by setting  $u = N_A / N_C$  where  $N_V$  and  $N_C$  are the effective density of states for the valance and conduction bands, respectively. They are given by:

$$N_{V} = \left[\frac{2\pi m_{p}^{*} kT}{h^{2}}\right]^{\frac{3}{2}}$$
(2.27)

and

$$N_{C} = \left[\frac{2\pi m_{n}^{*} kT}{h^{2}}\right]^{\frac{3}{2}}$$
 (2.28)

where h is Planck's constant and  $m_p^*$  and  $m_n^*$  are the hole and electron density of states effective masses. It should be noted that (2.25) is valid for both degenerately and nondegenerately doped material.

# 2.3 n-i-p-i-n Capacitors

# 2.3.1 Operation of n-i-p-i-n Structures as Storage Capacitors

P-i-n capacitors have been studied extensively for use in one-transistor dynamic memories in GaAs [5-9]. Similar concepts can be applied to SiC. When no charge is stored on an n-i-p-i-n capacitor, the p region is at ground and the p-n junctions are in equilibrium, Figure 2.3a. When a positive bias is applied to the top n region, the top junction is reverse biased and the bottom is forward biased, Figure 2.3b. Holes flow out of the p region through the forward biased junction, but can not be replenished by the reverse biased junction. This removal of holes charges the p region to a negative potential. Now, if the bias is

suddenly removed, the p region will remain at a negative potential. Thus both p-n junctions become reverse biased, Figure 2.3c. Note that in Figure 2.3, the i-layer was left out for simplification.

Ideally there would be no leakage currents and the capacitor would retain the stored charge forever. As might be expected, **this** is not the case for actual devices. The capacitors eventually return to zero-bias equilibrium due to leakage of charge through the reverse-biased p-i-n junctions.

# 2.3.2 n-i-p-i-n Capacitor Charge Storage

Under reverse bias conditions, the measured small signal AC capacitance of a p-i-n junction is primarily depletion capacitance given by [10, 13]:

$$C_{pin} = \frac{\epsilon_s A}{W}$$
 (2.29)

Where  $\in_{\mathbf{S}}$  is the semiconductor dielectric constant, A is the device area, and W is the depletion width. If the top and bottom **n-layers** are assumed to have the same doping, then the capacitance of an n-i-p-i-n structure after the bias is removed is given as follows:

$$C_{\text{nipin}} = \left[\frac{1}{C_{\text{top}}} + \frac{1}{C_{\text{bottom}}}\right]^{-1} = \left[\frac{W_{\text{top}}}{\epsilon_s A} + \frac{W_{\text{bottom}}}{\epsilon_s A}\right]^{-1} = \left[\frac{2W}{\epsilon_s A}\right]^{-1}$$
(2.30)

therefore:

$$C_{\text{nipin}} = \frac{\epsilon_s A}{2W} \tag{2.31}$$

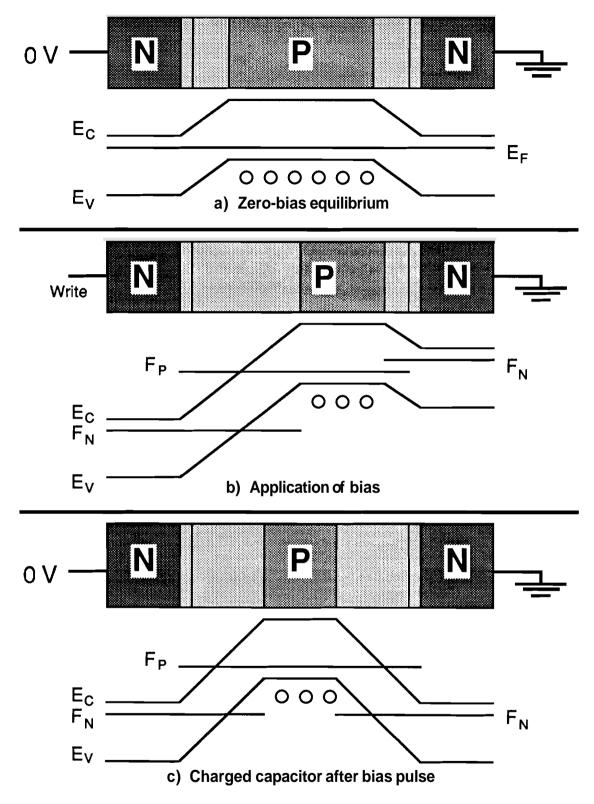


Figure 2.3 Various states in the charging of an n-p-n capacitor.

From (2.1), the charge stored on an n-i-p-i-n capacitor is given by

$$Q_T = 2qA \frac{N_D N_A}{N_D + N_A} [W - W_o]$$
 (2.32)

The factor of two accounts for the fact that there are two p-i-n junctions in an n-i-p-i-n capacitor.

Solving (2.31) for W and substituting into (2.32) a direct relationship between capacitance and stored charge is obtained:

$$Q_{T} = 2qA \frac{N_{D}N_{A}}{N_{D} + N_{A}} \left[ \frac{\epsilon_{s}A}{2C_{nipin}} - \frac{\epsilon_{s}A}{2C_{nipino}} \right]$$
(2.33)

Simplifying to get:

$$Q_{T} = qA^{2} \in {}_{S} \frac{N_{D}N_{A}}{N_{D} + N_{A}} \left[ \frac{1}{C_{nipin}} - \frac{1}{C_{nipino}} \right]$$
(2.34)

where  $C_{\mbox{\scriptsize nipino}}$  is the zero-bias equilibrium capacitance of the n-i-p-i-n structure.

# 2.3.3 Leakage Mechanisms in n-i-p-i-n Capacitors

As stated earlier in section 2.3.1, ideally there would be no leakage currents and the charge would be stored forever. This is not the case for actual devices, and they eventually return to their zero-bias equilibrium state due to leakage currents in the depletion regions of the device. This reverse leakage current governs the decay of charge as follows:

$$2I_{R} = -\frac{dQ}{dt} \tag{2.35}$$

where  $I_R$  is the leakage in one of the p-i-n junctions. For the n-i-p-i-n structures under study this reverse leakage current,  $I_R$ , is primarily due to thermal generation of electron-hole pairs in the depletion regions. Other sources of generation are assumed to be zero since the measurements are performed in an electrically shielded light tight box.

There is perimeter generation that scales with the device perimeter and depends on conditions at the surface of the device. The second component is bulk generation which scales with the area of the device. To first order, the leakage current can be modeled as [5,6,7,14]:

$$\frac{I_R}{A} = J_R = J_{Rbulk} + J_{Rperimeter} = qW_GG_B + qW_GAG_P$$
 (2.36)

where  $J_R$  is the reverse current density (Acm<sup>-2</sup>),  $G_B$  is the bulk generation rate (cm<sup>-3</sup>s<sup>-1</sup>),  $G_P$  is the effective perimeter generation rate (cm<sup>-2</sup>s<sup>-1</sup>), and P/A is the device perimeter-to-area ratio.  $W_G$  is the generation width which is approximately equal to the reverse bias depletion width minus the equilibrium depletion width.

#### 2.3.3.1 Bulk Generation Rate

The bulk generation rate is given by the relation [5,6]:

$$G_{B} = \frac{n_{i}}{\tau_{pB} exp\left[\frac{E_{T} - E_{i}}{kT}\right] + \tau_{nB} exp\left[\frac{E_{i} - E_{T}}{kT}\right]} = \frac{n_{i}}{\tau_{G}}$$
(2.37)

where  $\tau_{pB}$  and  $\tau_{nB}$  are the hole and electron bulk generation lifetimes,  $E_T$  is the energy level of the generation centers,  $E_i$  is the intrinsic Fermi level and  $n_i$  is the intrinsic carrier concentration.  $\tau_G$  is defined as follows:

$$\tau_{G} = \tau_{pB} \exp\left[\frac{E_{T} - E_{i}}{kT}\right] + \tau_{nB} \exp\left[\frac{E_{i} - E_{T}}{kT}\right]$$
(2.38)

Consider the following:

when  $E_T = E_i$ 

$$\tau_{G} = \tau_{p} + \tau_{n} \tag{2.39}$$

when  $E_T > E_i$ 

$$\tau_{G} \approx \tau_{p} \exp\left[\frac{E_{T} - E_{i}}{kT}\right] = \tau_{p} \exp\left[\frac{\Delta E_{T}}{kT}\right]$$
(2.40)

and when E<sub>T</sub> < E<sub>i</sub>

$$\tau_{G} \approx \tau_{n} \exp\left[\frac{E_{i} - E_{T}}{kT}\right] = \tau_{n} \exp\left[\frac{\Delta E_{T}}{kT}\right]$$
(2.41)

From the previous cases it is seen that (2.38) can be replaced by

$$\tau_{G} = \tau_{B} exp \left[ \frac{\Delta E_{T}}{kT} \right]$$
 (2.42)

subject to the following:

when  $E_T = E_i$ 

$$\tau_{\mathsf{B}} = \tau_{\mathsf{n}} + \tau_{\mathsf{p}} \tag{2.43a}$$

when  $E_T > E_i$ 

$$\tau_{\mathsf{B}} = \tau_{\mathsf{p}} \tag{2.43b}$$

and when E<sub>T</sub> < E<sub>i</sub>

$$\tau_{\rm B} = \tau_{\rm n} \tag{2.43c}$$

The intrinsic carrier concentration is defined as [13]:

$$n_{i} = \sqrt{N_{C}N_{V}} \exp\left[\frac{-E_{G}}{2kT}\right]$$
 (2.44)

where  $N_C$  and  $N_V$  are the density of states in the conduction and valance bands, and  $E_G$  is the energy **bandgap** of the semiconductor. Inserting (2.42) and (2.44) into (2.37):

$$G_{B} = \frac{\sqrt{N_{C}N_{V}} \exp\left[\frac{-E_{G}}{2kT}\right]}{\tau_{B} \exp\left[\frac{\Delta E_{T}}{kT}\right]} = \frac{\sqrt{N_{C}N_{V}} \exp\left[\frac{-E_{AB}}{kT}\right]}{\tau_{B}}$$
(2.45)

where  $E_{AB}$  is the activation energy for bulk generation,  $E_{AB}$  = ( $E_{G}$  /2 + $\Delta E_{T}$ ).

#### 2.3.3.2 Perimeter Generation Rate

The perimeter generation rate is given by [5,6]:

$$G_{p} = \left[ \int_{E_{V}}^{E_{c}} \frac{c_{ns}c_{ps}D_{IT}(E)dE}{c_{ns}exp\left[\frac{E-E_{i}}{kT}\right] + c_{ps}exp\left[\frac{E_{i}-E}{kT}\right]} n_{i} \right]$$
(2.46)

where  $c_{ns}$  and  $c_{ps}$  are the surface hole and electron capture coefficients (cm<sup>3</sup>s<sup>-1</sup>), and D<sub>IT</sub> is the surface state density (cm<sup>-2</sup>eV<sup>-1</sup>).

Equation (2.46) can be rewritten as:

$$G_{p} = s_{o} n_{i} \tag{2.47}$$

where  $\mathbf{s_o}$  is the surface generation velocity (cms<sup>-1</sup>) given by the integral in (2.46). By assuming that we can group the temperature dependent and independent components  $G_p$  can be put in the form:

$$G_{P} = C \exp\left[\frac{-E_{AP}}{kT}\right]$$
 (2.48)

where C is a temperature independent constant, and  $E_{AP}$  is the activation energy for the perimeter generation component. The constant C actually varies as  $T^2$ , neglecting this results in an error of less than 10% in the temperature range considered.

# 2.3.4 n-i-p-i-n Storage Time Theory

Consider a capacitor that has just been charged with a bias pulse as in figure **2.3c**. When the bias pulse is removed the charge stored on the capacitor is given by (2.32):

$$Q = 2qAN_BW_G (2.49)$$

where

$$W_{G} = W - W_{o} \tag{2.50}$$

and

$$N_{B} = \frac{N_{D}N_{A}}{N_{A} + N_{D}} \tag{2.51}$$

As stated in section 2.3.3, the rate at which charge leaks out of the n-i-p-i-n capacitor is governed by the reverse bias leakage current. Combining (2.35) and (2.36) gives:

$$\frac{dQ}{dt} = -2I_{R} = -2qW_{G}A\left[G_{B} + \frac{P}{A}G_{P}\right]$$
 (2.52)

Solving (2.49) for  $W_G$  and substituting into (2.52) gives:

$$\frac{dQ}{dt} = -2q \left[ \frac{Q}{2qAN_B} \right] A \left[ G_B + \frac{P}{A} G_P \right]$$
 (2.53)

which simplifies to:

$$\frac{dQ}{dt} = -\frac{Q}{N_B} \left[ G_B + \frac{P}{A} G_P \right]$$
 (2.54)

The solution of (2.54) is:

$$Q(t) = Q(0) \exp \left[ -\frac{G_{B} + \frac{P}{A}G_{P}}{N_{B}} t \right] = Q(0) \exp \left[ -\frac{t}{\tau_{s}} \right]$$
 (2.55)

**Q** is a decaying exponential function where **Q(0)** is the charge stored at  $t = 0^+$  and  $\tau_s$  is the time constant, or 1/e storage time of the structure:

$$\tau_{\rm s} = \frac{N_{\rm B}}{G_{\rm B} + \frac{P}{A}G_{\rm P}} \tag{2.56}$$

Along with storage times of various sizes of capacitors, (2.56) provides much useful information about generation processes in the device. From a plot of  $1/\tau_s$  versus P/A, the bulk and perimeter generation components can be extracted. Perimeter generation corresponds to the slope, and bulk generation is related to the y-intercept.

#### CHAPTER 3 - DEVICE FABRICATION AND MEASUREMENT

#### 3.1 Introduction

This chapter deals with two issues. First, the fabrication of n-i-p-i-n capacitors in **6H-SiC** is described where two lots of wafers, A and B containing four wafers each, are considered. Next, the experimental set-up and methods to measure storage times are described.

#### 3.2 Fabrication

A cross section of the structures studied is shown in Figure 3.1. They consisted of a series of circular n-i-p-i-n diodes of diameters 1.5, 3, and 4 mils (1 mil = 25.4 μm). The n-i-p-i-n epitaxial layers were grown on the Si-face of 25.4 mm diameter single crystal 6H-SiC substrates. The n and p-type dopants were nitrogen and aluminum, respectively, and were introduced in-situ during epitaxy. The 30 nm thick "i" layers were actually unintentionally doped n-type 6H-SiC with a carrier concentration in the range of 3-8x1015 cm<sup>-3</sup>. Doping of the n and p epilayers for the different wafers ranged from 1.3-6x1018 cm<sup>-3</sup>. 6H-SiC is degenerately doped in this range.

The circular mesas were defined by reactive ion etching in NF3 [15], and the surfaces were then passivated by growth of  $SiO_2$  via thermal oxidation. The wafers from lot A were oxidized in dry  $O_2$  at 1200 °C for 30 mins, resulting

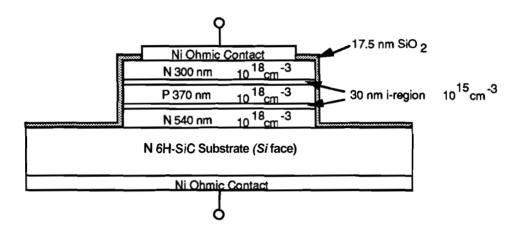


Figure 3.1 Cross section of n-i-p-i-n devices studied.

in an SiO<sub>2</sub> thickness of 17.5 nm. The wafers from lot **B** were oxidized in wet O<sub>2</sub> at 1100 °C for 40 mins, which also yielded 17.5 nm of SiO<sub>2</sub>. Ohmic contact was made to the top and bottom of the wafers with annealed nickel. All processing steps were performed by Cree Research, Inc., Durham, NC.

# 3.3 Measurement of Storage Times

Section 2.3.2 showed the relationship between stored charge and measured capacitance for an n-i-p-i-n device. Thus it is possible to observe the charge decay by experimentally monitoring the capacitance recovery.

Storage time measurements were performed as described by Neudeck [6]. Figure 3.2 shows a schematic representation of the test set up. The devices were contacted by using a MicroManipulator probe station that was located inside a shielded dark box. High temperature characterization was performed using a hot chuck with a built-in heating element and J-type thermocouple. The device capacitance was monitored using a Boonton 72B meter. Data from the meter's analog output was recorded on a Tektronix 11401 digitizing oscilloscope. Manually triggered pulses were fed to the device from a pulse generator via the capacitance meter bias inputs. The magnitude of pulse biases used ranged from 2 V to 5.2 V. Most measurements were carried out using either a 5 V or 5.2 V pulse.

Charge is written to the capacitor as described in section 2.3.1. Figure 3.3 shows the capacitance recovery transient from an actual measurement. Immediately after the pulse at  $t=0^+$  the magnitude of the stored charge is at its maximum and the capacitance  $C_{nipin}(0)$  is at its lowest value. As the charge

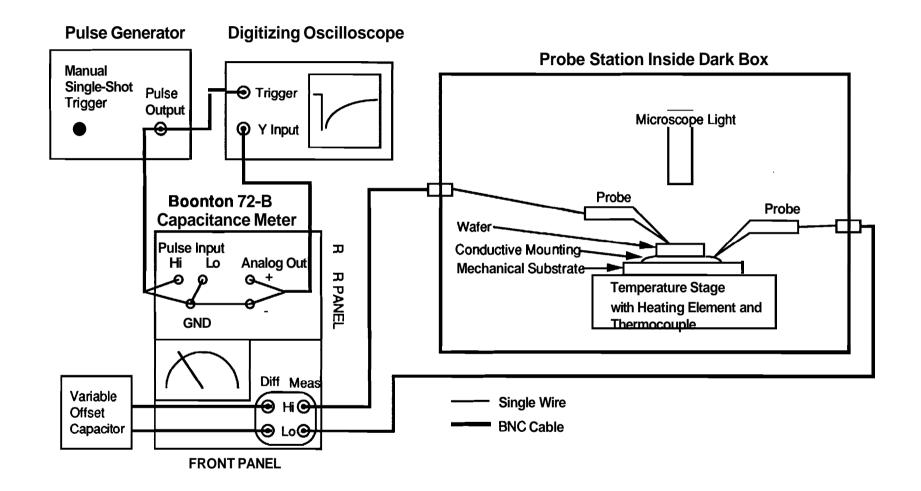


Figure 3.2 Schematic representation of experimental apparatus used to conduct n-i-p-i-n capacitor storage time measurements. After reference [6].

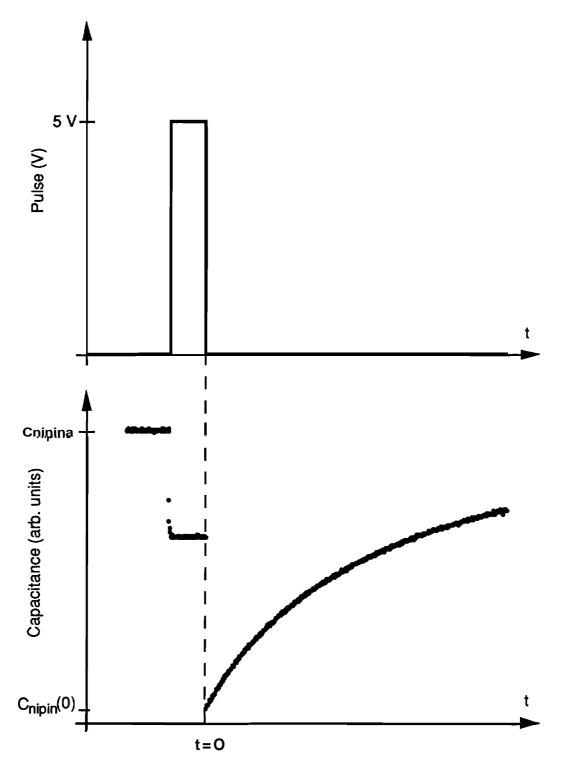


Figure 3.3 Capacitance recovery transient for an actual device.

in the device decays, the capacitance  $C_{nipin}$  increases until it reaches its **zero**-charge equilibrium value of  $C_{nipino}$ 

It is possible to use (2.34) to calculate charge from the measured capacitance and then use (2.55) to calculate the exponential time constant. This method requires several calculations and is time consuming. An easier but less accurate method is to measure the storage times directly from device capacitance transients. With that, the storage time is defined experimentally as the time for the capacitance to recover to within 1/e (36.8 %) of its zero-charge value [6]. This value is readily obtained from the C-t plot on the oscilloscope.

The relation between the capacitance recovery time  $\tau_c$  and the charge recovery time  $\tau_s$  is discussed thoroughly by Dungan [5].  $\tau_c$  is usually less than 20 % larger than  $\tau_s$ . The difference is not large enough to merit the additional work in calculating the true  $\tau_s$ . Therefore the approximation:

$$\tau_{\rm s} \equiv \tau_{\rm c} \tag{3.1}$$

will be made. This definition of storage time is used in the following chapters.

#### CHAPTER 4 - EXPERIMENTAL RESULTS AND DISCUSSION

#### 4.1 Introduction

In this chapter, the results of experimental characterization of devices in lot A and lot B are presented. These devices were passivated with dry and wet  $O_2$  as discussed in section 3.2. Storage times, activation energies, generation mechanisms and evidence of field-enhanced generation are discussed. Possible error in temperature measurement is considered in the final section of this chapter.

# 4.2 Experimental Measurements on Lot A (Dry O<sub>2</sub> Passivation)

# 4.2.1 Storage Times

As stated in section 3.3, the storage time constant  $\tau_s$  is defined as the time required for the capacitance to recover to within 1/e of its zero-bias equilibrium value. The storage times for several 1.5, 3 and 4 mil diameter mesa devices are shown in Figure 4.1. The measurements were made at 160 °C using a 5.2 V pulse. I-V characteristics of several hundred devices from these wafers were studied, and those devices showing a large reverse bias leakage were disregarded. Figure 4.1 shows that in spite of the variation among

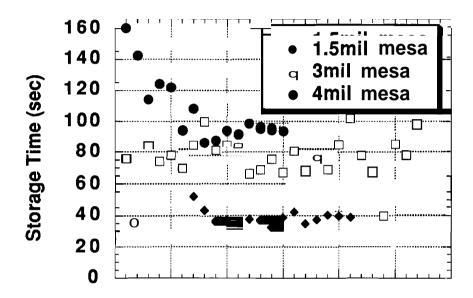


Figure 4.1 Storage times at 160 °C for several 1.5, 3 and 4 mil n-i-p-i-n capacitors passivated with dry  $O_2$ , lot A.

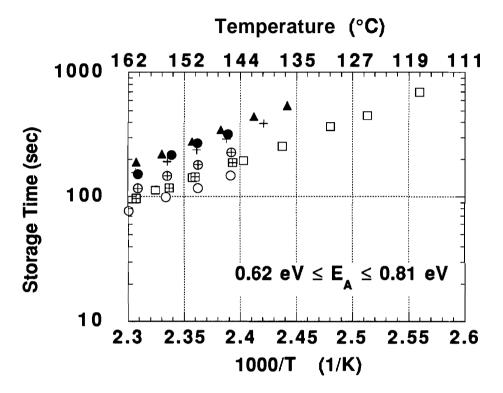


Figure 4.2 Storage time versus 1000/T for several 3 mil mesa devices from lot A.

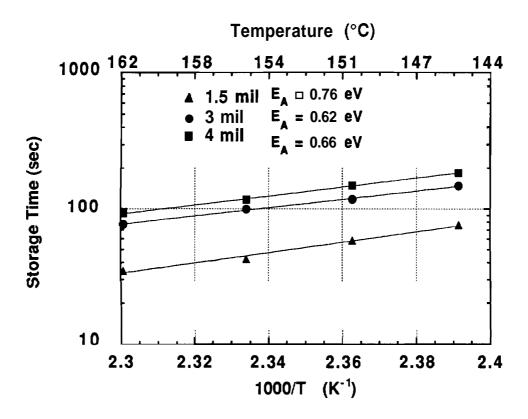


Figure 4.3 Storage time versus 1000/T for 1.5, 3 and 4 mil devices from lot A.

devices, a general trend is apparent. As area decreases (and P/A ratio increases), the storage time is reduced which correlates well with (2.56).

### 4.2.2 Thermal Activation of Storage Times

The capacitance recovery is thermally activated as can be seen in Figure 4.2. Here storage time versus 1000/T is plotted for several 3 mil devices on four different wafers from lot A. The plot is of the form:

$$\tau_{s} = \tau_{o} \exp\left[\frac{E_{A}}{kT}\right] \tag{4.1}$$

where  $\tau_0$  is a temperature independent proportionality constant and  $E_A$  is the activation energy. The activation energies in Figure 4.2 range from 0.62 eV to 0.81 eV. Similar data for 1.5 and 4 mil devices produce activation energies within this same range, Figure 4.3.

The activation energy is defined as the energy of the rate-limiting transition that a carrier has to make in going from one band to the other. From this definition one would usually expect the activation energy to be greater than or equal to half bandgap for a single level trap. Half bandgap is 1.45 eV for 6H-SiC, approximately two times larger than the measured activation energies for lot A. The origin of the less than half bandgap thermal activation is not well understood. Possible contributing factors are field-enhanced generation, multilevel generation centers, and/or a large density of traps at various energies throughout the bandgap.

Field-enhanced generation will be discussed in great detail in section 4.4.1. Multi-level centers have been seen in silicon and are generally attributed to trace amounts of metallic impurities such as Au or Pt [16]. After analyzing

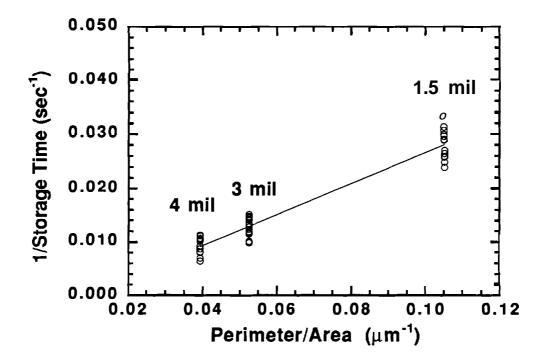


Figure 4.4 1/storage time versus P/A ratio for devices from lot A.

devices passivated with wet  $O_2$ , it will be seen that multi-level centers are unlikely. In section 4.2.3, it will be shown that these devices are dominated by perimeter generation which could indicate the presence of a large number of surface states along the perimeter of the device. These states are considered to be at various energy levels throughout the **bandgap**. If the density of these states is very large, it is possible that one trap could be in close enough physical proximity to another trap so a carrier could reach the conduction band through more than one center. This could result in an activation energy of less than half **bandgap**.

# 4.2.3 Storage Time Dependence on Perimeter to Area Ratio

A plot of  $1/\tau_8$  versus P/A ratio for several 1.5, 3 and 4 mil devices is shown in Figure 4.4. One device of each size lying closest to the least squares fit curve was chosen to perform more measurements. Figure 4.5 shows a plot of  $1/\tau_8$  versus P/A ratio for four different temperatures. As indicated by (2.56), the slope of these curves corresponds to the perimeter generation rate ( $G_P$ ) and the y-intercept corresponds to the bulk generation rate ( $G_B$ ). The nearly zero y-intercept of all curves indicates that the bulk component of generation is very small compared to the perimeter generation rate. A negative y-intercept is obtained for two of the curves. Negative values for generation rate have no physical meaning, so these less than zero intercepts are attributed to scatter in the data. This can be seen by noting that a small change in the value of one of the data points will not have a large effect on the slope of the curve fit ( $G_P$ ), but can significantly alter the y-intercept ( $G_B$ ).

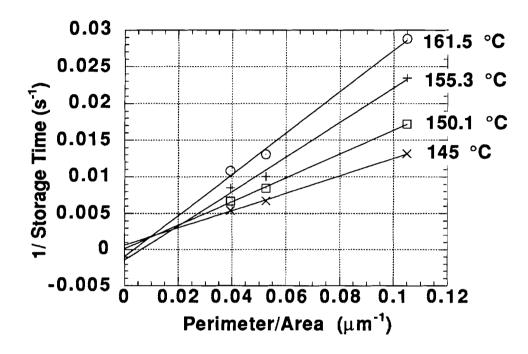


Figure 4.5 1/storage time versus P/A ratio at several temperatures for devices in lot A.

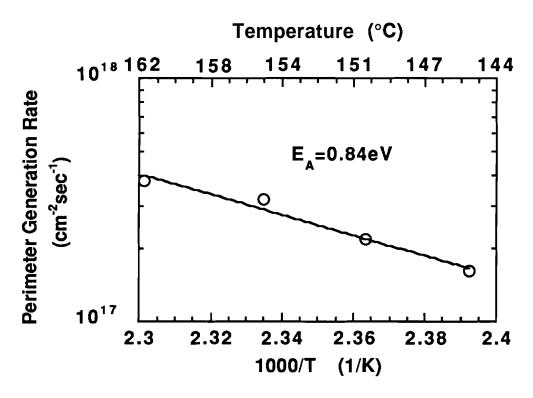


Figure 4.6 Perimeter generation versus 1000/T for devices of lot A.

Information about the thermal activation of the perimeter component can be found with (2.56) and the slopes of Figure 4.5. The perimeter generation ( $G_P$ ), shown in Figure 4.6, exhibits an activation energy of 0.84 **eV**, which is just slightly above the range of activation energies given earlier for the storage times of the devices.

# 4.3 Experimental Measurements on Lot B (Wet O<sub>2</sub> Passivation)

#### 4.3.1 Motivations for Better/Different Passivation

As seen in Figure 4.5, the devices in lot A are dominated by perimeter generation. This suggests that the storage time may be very sensitive to thermal oxidation conditions during formation of the passivating oxide. To test this hypothesis, a new set of devices was fabricated and passivated using wet oxidation (lot B) instead of dry oxidation (lot A). Wet oxidation has been observed to yield better MOS electrical characteristics on (100)  $\beta$ -SiC than dry oxidation [17].

# 4.3.2 Storage Times

The storage times were measured in the same manner as outlined in sections 3.2 and 4.1.0. It should be noted that due to the extremely long storage times at 160 °C these devices had to be measured at much higher temperatures. This temperature range was from 292 °C to 331 °C. Figures 4.7 and 4.8 display the storage times for 1.5, 3 and 4 mil devices. All measurements were made using a 5 V pulse. The 3 mil devices were

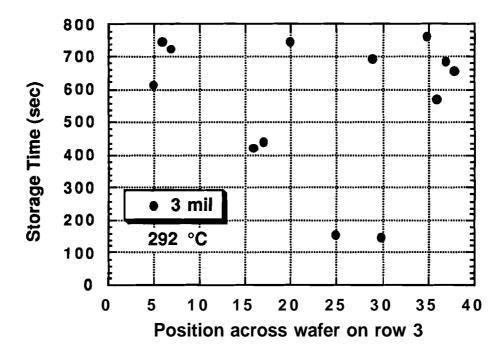


Figure 4.7 Storage times for 3 mil mesa devices passivated with wet  $O_2$ , lot B.

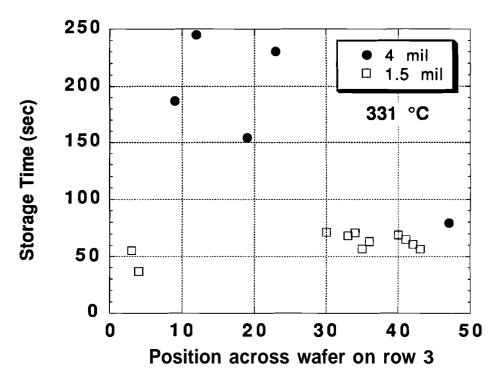


Figure 4.8 Storage times for 1.5 and 4 mil devices passivated with wet  $O_2$ , lot B.

measured at 292 °C. The 1.5 and 4 mil devices were both tested at 331 °C. When comparing the storage times of the 1.5 and 4 mil devices it is again seen that as the area decreases the storage time is reduced, in keeping with (2.56).

#### 4.3.3 Thermal Activation

As with the devices of lot A the capacitance recovery is thermally activated for the devices in lot B. Figure 4.9 shows storage time versus 1000/T measurements performed on 1.5, 3, and 4 mil mesa devices. Using (4.1) activation energies in the range of 1.38 eV to 1.55 eV are obtained. These are very close to the expected half bandgap activation energy of 1.45 eV.

# 4.3.4 Storage Time Dependence on Perimeter to Area Ratio

Figure 4.10 displays a plot of  $1/\tau_s$  versus P/A ratio for several 1.5, 3 and 4 mil devices. The two best 1.5 and 4 mil devices were measured. Since there was more scatter among the 3 mil devices, the best three were used in the  $1/\tau_s$  versus P/A plot. As stated earlier in section 4.2.3 the slope of these curves corresponds to the perimeter generation rate  $(G_P)$  and the y-intercept corresponds to the bulk generation rate  $(G_B)$ . Again the nearly zero y-intercept of all curves indicates that the bulk component of generation is very small compared to the perimeter generation rate. As before, the negative y-intercepts are due to scatter in the data.

Using (2.56) and the slopes of Figure 4.10, information about the thermal activation of the perimeter component is obtained. The perimeter generation (G<sub>P</sub>), shown in Figure 4.11, exhibits an activation energy of 1.55 eV which is in

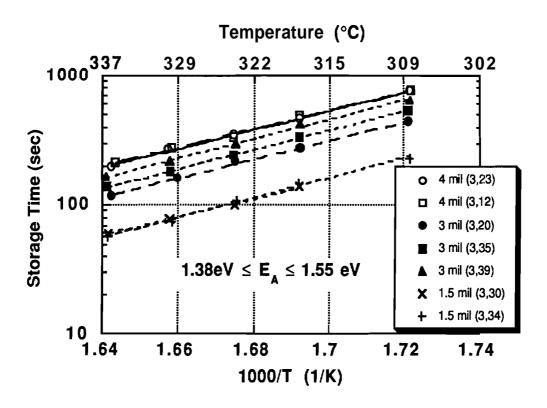


Figure 4.9 Storage time versus 1000/T for 1.5, 3 and 4 mil devices from lot B.

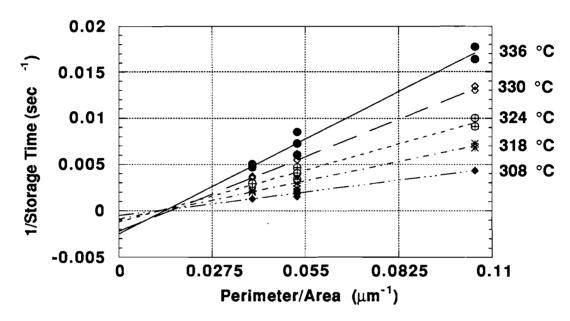


Figure 4.10 1/storage time versus P/A ratio at several temperatures for devices in lot B.

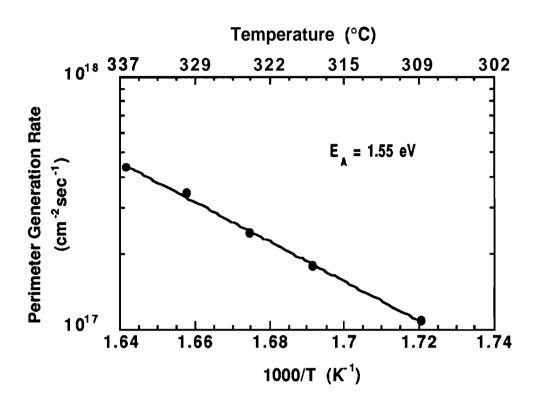


Figure 4.11 Perimeter generation versus 1000/T for devices of lot B.

the range of activation energies measured earlier for the storage times of the devices. This indicates that perimeter generation is still dominant, even in the devices passivated with wet  $O_2$ . Later, it will be seen that the magnitude of the perimeter generation has decreased in the devices passivated with wet  $O_2$  when compared to those passivated with dry  $O_2$ .

#### 4.4 Field-Enhanced Generation

Field-enhanced generation appears to play a role in the devices passivated with dry  $O_2$  (lot A). The devices passivated with wet  $O_2$  (lot B) **show** no evidence of field-enhanced generation. In this section the theory behind and evidence of field enhanced generation are considered.

# 4.4.1 Theory

Field-enhanced generation can be described as thermal generation that has been **enhanced** by the presence of a large electric field. **This** effect can be seen in Figure 4.12 [5,6,18,19]. For thermal generation to occur, an electron and hole must be excited by the crystal's thermal energy from a generation center in the forbidden gap into the conduction and valence bands respectively. The barrier can be represented by the Coulombic spatial potential presented in Figure **4.12a**. When a large electric field is present, the shape of the Coulombic potential is altered as seen in Figure **4.12b**. Thus, there is a reduction in the barrier height that the electron and hole must overcome. This reduction in barrier height was described theoretically by Frenkel in 1938 [18,191. Frenkel

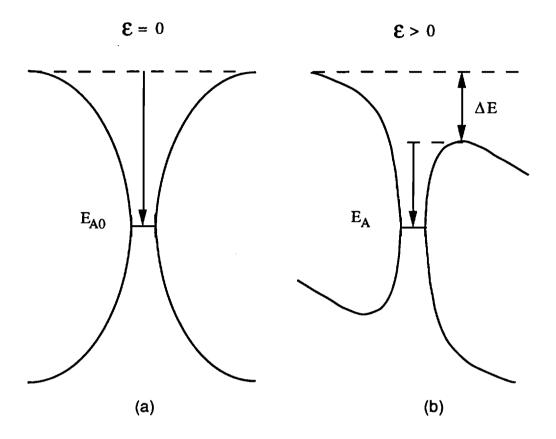


Figure 4.12 1-dimensional representation of coulombic spatial potential of a generation center. (a)  $\mathbf{E} = \mathbf{0}$  and (b)  $\mathbf{E} > \mathbf{0}$ , where it is seen that the shape of the coulombic potential is altered causing a reduction of the barrier height. After references [5,6,18,19].

derived a simple one **dimensional** approximate model for the barrier **lowering** given by: [18,191

$$\Delta E_{A} = \left[\frac{qE}{\pi \epsilon_{s}}\right]^{\frac{1}{2}} \tag{4.2}$$

where  $\Delta E_A$  is the barrier lowering in eV,  $\mathcal{E}$  is the electric field in V/cm, and  $\epsilon_s$  is the high-frequency semiconductor dielectric constant in F/cm.

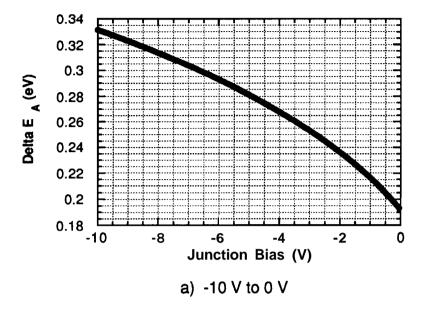
In GaAs, it has been seen that the most heavily doped p-n-p capacitors do not produce the longest storage times, despite the fact that they have the smallest generation volume. This is due to the higher electric fields present in the highly doped structures. These fields cause field-enhanced generation resulting in shortened generation lifetimes and reducing the activation energy for the capacitors [5]. Thus one of the primary parasitic reverse leakage mechanisms in highly doped junctions is field-enhanced generation. One would expect that the same effect might be seen in highly doped SiC p-n junctions.

If it is assumed that we have a symmetric n-p-n structure with  $N_A=6x10^{18}cm^{-3}$  and  $N_D=1.9x10^{18}cm^{-3}$  the semiconductor is degenerately doped. The maximum electric field on one junction is given by:

$$\left| \mathcal{E}_{\mathsf{m}} \right| = \frac{\mathsf{qN}_{\mathsf{A}}}{\in_{\mathsf{S}}} \mathsf{x}_{\mathsf{p}} \tag{4.3}$$

where

$$x_{p} = \frac{-x_{i} + \left[ [x_{i}]^{2} - \left[ 1 + \frac{N_{D}}{N_{A}} \right] \left[ \frac{2 \in s}{q N_{D}} \right] [V_{A} - V_{bi}] \right]^{\frac{1}{2}}}{1 + \frac{N_{A}}{N_{D}}}$$
(4.4)



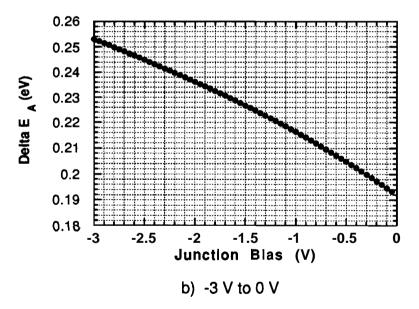


Figure 4.13 Plot of change in  $E_A$  versus junction bias due to field enhanced generation. The plots were obtained from (4.5) for the ranges (a) -10 V to 0 V and (b) -3 V to 0 V.

obtained from (2.10),(2.16) and (2.21). By using (4.3) and (4.4) with (4.2), a relationship between barrier lowering  $\Delta E_A$  and junction bias  $V_A$  is obtained:

$$\Delta E_{A} = \frac{q}{\epsilon_{s}} \left[ \frac{N_{A}}{\pi} \left[ -x_{i} + \left[ [x_{i}]^{2} - \left[ 1 + \frac{N_{D}}{N_{A}} \right] \left[ \frac{2\epsilon_{s}}{qN_{D}} \right] [V_{A} - V_{bi}] \right]^{\frac{1}{2}} \right] \frac{1}{2}$$

$$1 + \frac{N_{A}}{N_{D}}$$
(4.5)

Figure 4.13 plots  $\Delta E_A$  vs  $V_A$  obtained from (4.5) over the voltage range of -10 V to 0 V. This shows that for a reverse bias on both junctions of 10 V, the measured activation energy would be reduced by 0.33 eV. The junction biases used to empty the p-region where in the range between -2 V and -5 V.

# 4.4.2 Experimental Verification of Field-Enhanced Generation

## 4.4.2.1 Change in Activation Energy Versus Pulse Magnitude, Lot A

Recall, while the pulse is applied to the device, one junction is forward biased while the other is reverse biased. During this time most of the voltage drop occurs across the reverse biased junction and essentially none occurs across the forward biased junction. Once the bias is removed, both of the n regions are at ground potential and the p region is left floating, charged to a negative potential. Both p-n junctions will be reverse biased with the potential drops across each of the junctions being equal. Assume then that the bias on each will be less than or equal to one half the initial pulse magnitude. Under this assumption the reverse bias on each of the junctions after a 5.0 V pulse is removed would be  $\leq 2.5$  V.

Figure 4.13b is an expanded view of Figure 4.13a for the region -3 V to 0

V. From this figure it can be seen that a pulse of 5.2 V resulting in a 2.6 V reverse bias across each junction would cause a barrier reduction of approximately **0.247eV**. Likewise, a 2.5 V pulse would theoretically cause a barrier reduction of approximately 0.222 **eV**. From this information, one would expect to see a difference of 0.025 **eV** between the activation energy for a device measured using a 5.2 V pulse and that found using a 2.5 V pulse, if the dominant generation mechanism is field-enhanced generation.

Experimental data was collected on a 3 mil (67.5 $\mu$ m) diameter n-i-p-i-n device from lot A. The area of this device is 3,578  $\mu$ m<sup>2</sup>. Storage time measurements were taken at several different temperatures using pulse biases of 5.2 V and 2.5 V. Figure 4.14 shows a comparison between the two pulse magnitudes of storage time versus 1000/T. From the data, an activation energy can be obtained as described in section 4.2.2 from the slope of the exponetial fit for each of the points. Figure 4.14 shows that for a pulse bias of 5.2 V an activation energy of 0.664 eV is obtained, while for a pulse bias of 2.5 V an activation energy of 0.696 eV is obtained. The difference between the two activation energies measured is 0.032 eV, with the activation energy obtained using the 2.5 V pulse being larger. The difference of 0.032 eV is in reasonable agreement with the theoretical value of 0.025 eV obtained earlier. This could indicate that field-enhanced generation plays a dominant role in the devices passivated with dry  $\mathbf{O_2}$  (lot A).

# 4.4.2.2 Storage Time Versus Pulse Magnitude, Lot A and Lot B

It can be seen from (2.37), (2.47), and (2.56) that for a simple derivation for the charge recovery in a generation-limited p-n junction with symmetric

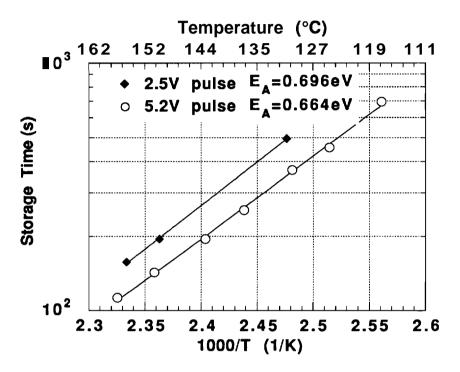


Figure 4.14 Comparison of storage time versus 1000/T for different bias pulses applied to a 3 mil diameter device, lot A.

doping (i.e.  $N_A=N_D$ ) that the two equations obtained for the recovery time constant are:

$$\tau_{\rm B} = \frac{N_{\rm B}\tau_{\rm G}}{n_{\rm i}} \tag{4.6}$$

for a bulk dominated device and

$$\tau_{P} = \frac{N_{B}}{s_{o}n_{i}}\frac{A}{P} \tag{4.7}$$

for a perimeter dominated device. These equations predict that the charge recovery time constant for a symmetrically-doped diode dominated by mid-gap traps will be independent of the magnitude of the initial stored charge, thus independent of the initial pulse bias.

As can be seen by Figure **4.15** for the **3** mil **SiC** device from lot A, there is a definite dependence of charge recovery time constant on pulse magnitude. The storage time for the device varied from **189** seconds for a **2.0** V bias to 118 seconds for a **5.2** V bias. Thus, it is seen that as pulse bias increases the storage time decreases. This effect can be explained by field-enhanced generation. As shown earlier in section **4.4.3.1** with differences in activation energy, field enhanced generation plays a major role in these **SiC** devices. Figure **4.16** plots storage time versus initial pulse for a **3** mil device from lot **B**. The plot exhibits no apparent dependence of storage time on pulse sign or magnitude. This seems to indicate that field-enhanced generation doesn't play a major role in the devices annealed with wet **O<sub>2</sub>** (lot **B**).

Increasing the magnitude of the pulse bias increases the charge uncovered causing an increase in the magnitude of the electric field across the p-n junctions. This increase in electric field causes an increase in field-enhanced barrier lowering. As the potential barrier is lowered it is easier for

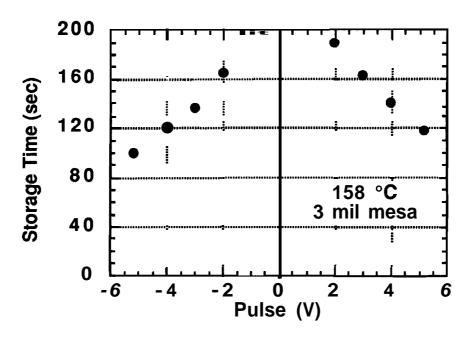


Figure 4.15 Dependence of storage time on pulse magnitude and polarity, lot A.

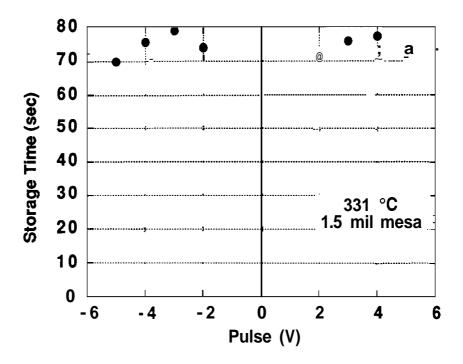


Figure 4.16 Dependence of storage time on pulse magnitude and polarity, lot B.

thermal generation to occur, thus causing a decrease in storage time. This accounts for the decrease in storage time with increasing pulse magnitude viewed in lot A.

At this time, it is beneficial to mention that this is not the same effect seen by Dungan [5]. In his GaAs devices, he saw an increase in storage time with an increase in pulse magnitude. The explanation for this was the fact that the capacitance-recovery transient was not a true exponential for two reasons. First, the capacitance is not directly proportional to the charge. Therefore, even if the charge recovery was exponential the capacitance recovery would be slightly non-exponential. The second reason is that in an asymmetrically-doped structure ( $N_A \neq N_D$ ), the charge recovery itself is non-exponential. As shown by Dungan these effects would give an increase in storage time with an increase in pulse magnitude. Field-enhanced barrier lowering did not seem to play a major role in the characteristics of the GaAs devices [5]. The opposite dependence on pulse magnitude is seen in the SiC devices of lot A, indicating that field-enhanced barrier lowering has a larger influence on these highly doped SiC devices annealed in dry  $O_2$  than do the factors causing non-exponential charge recovery.

Looking at Figure **4.15** it can be seen that there is a slight non-symmetry between pulse polarity. This could be due to non-symmetry in the two p-n junctions ( $N_{D1} \neq N_{D2}$ ). More charge is removed for one polarity than for the other. This can be seen most easily by recalling that for a simple p-n junction the charge removed during the pulse is given by:

$$Q = qAN_A[x_p - x_{po}]$$
 (4.8)

Where  $\mathbf{x}_{\textbf{po}}$  is the zero-bias equilibrium depletion width on the p side of the

junction and  $\mathbf{x_p}$  is the depletion width on the p side of the reverse biased junction. From (2.16) and (2.21) the depletion width  $\mathbf{x_p}$  is given by:

$$x_{p} = \left[\frac{2 \in s}{q} \left[\frac{N_{D}}{N_{A}[N_{A} + N_{D}]}\right] [V_{bi} - V_{A}]\right]^{\frac{1}{2}}$$
(4.9)

where  $V_{A}$  is the voltage applied across the junction, and  $V_{bi}$  is the built in junction potential.

Combining (4.8) and (4.9) the following is obtained:

$$Q = qA \left[ \frac{N_D N_A}{N_D + N_A} \right]^{\frac{1}{2}} \left[ \left[ V_{bi} - V_A \right]^{\frac{1}{2}} - \left[ V_{bi} \right]^{\frac{1}{2}} \right]$$
(4.10)

Rearranging to obtain:

$$Q = qA \left[ \frac{N_A}{1 + \frac{N_A}{N_D}} \right]^{\frac{1}{2}} \left[ \frac{2 \in s}{q} \right]^{\frac{1}{2}} \left[ [V_{bi} - V_A]^{\frac{1}{2}} - [V_{bi}]^{\frac{1}{2}} \right]$$
(4.11)

where it is seen that:

$$Q \alpha \frac{N_A}{1 + \frac{N_A}{N_D}} \tag{4.12}$$

Inspection of (4.12) now reveals that as  $N_D$  increases, the amount of charge uncovered increases. Equation (4.12) also shows that when  $N_{D1} \neq N_{D2}$  for a n-p-n capacitor more charge is uncovered for one pulse polarity than for the other. As stated earlier, this difference in charge stored will cause a difference in storage time. This could account for the non-symmetry seen in storage time with pulse polarity for the device from lot A.

# 4.4.2.3 Correspondence Between Measured Change in Activation Energy and Dependence of Storage Time on Pulse Bias in Lot A

If the change in activation energy with pulse bias, Figure 4.14, and the variation of storage time with pulse magnitude, **Figure** 4.15, are due to **field**-enhanced generation, then it is expected to see a correspondence between the two. Recall from (4.1) the thermally activated storage time is of the form:

$$\tau_{s} = \tau_{o} \exp\left[\frac{E_{A}}{kT}\right] \tag{4.13}$$

where  $\tau_0$  is a temperature independent constant.  $\tau_0$  can be obtained from the y-intercept of a plot of  $\tau_S$  vs 1/T.

If Figure 4.14 is extrapolated to 1/T=0, Figure 4.17 is obtained. It can be seen that there is a slight difference in the y-intercepts. For a 2.5 V bias pulse the y-intercept is 1.02x10<sup>-6</sup> seconds and for 5.2 V bias pulse the y-intercept is 1.81x10<sup>-6</sup> seconds. The difference is less than a factor of two. It should be realized that in fitting data points a slight variation in the measured value of a data point will cause only a slight variation in the slope of the fitted line, but will cause a significant change in the y-intercept. Therefore, the difference seen above is not extremely surprising, and it is not unreasonable to use an averaged value for  $\tau_0$ . If this value of  $\tau_0$  along with the activation energies obtained from Figure 4.14 are inserted into (4.13), the following is obtained. At a temperature of 158 °C,  $\tau_{scalculated}$  = 192 seconds for a 2.5 V bias pulse and  $\tau_{scalculated}$  = 81 seconds for a 5.2 V bias. Comparing these values with Figure 4.15, it is seen that they are reasonably close. So, measured changes in activation energy correspond reasonably well with measured differences in storage time versus pulse bias.

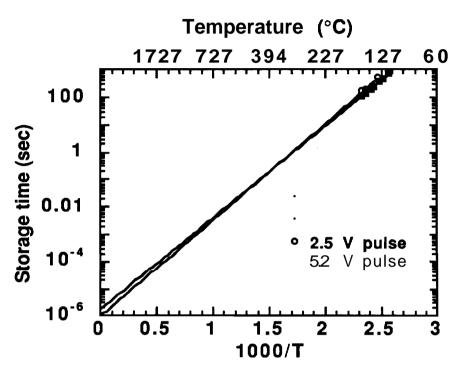


Figure 4.17 Storage time versus 1000/T extrapolated back to 1000/T=0 for 2.5V and 5.2V biases. The device from lot A has a diameter of 3 mil.

#### **4.5** Possible Error in Temperature Measurement

This section first considers possible sources of error in the measurement of device temperature. Then, the effect they would have on the measured activation energy is discussed.

#### **4.5.1** Sources of Temperature Error

Because of the test set up, it is possible that the measured temperature is not the actual temperature of the device for the following reasons. When using the Micromanipulator the temperature is monitored by a thermocouple located within the heated test chuck. Therefore, it is possible that the temperature on the outside of the chuck, where the test sample is located, is different than that at the thermocouple. Since the SiC sample is mounted on a 2" Si wafer in order to make electrical contact to the backside of the SiC, there is the possibility that a temperature gradient is formed from the bottom of the Si wafer up to the SiC. This means the SiC sample could be at a temperature less than that of the top of the test chuck. Another source of difference in temperature may exist between the Si wafer and the heated test chuck. There is no vacuum holding the wafer down onto the chuck, therefore this is a possible cause of a temperature variation if the wafer is not in good thermal contact with the chuck. One final possible cause of temperature difference is the fact that heat could be lost from the sample through contact with the unheated test probe.

# 4.5.2 Effect of Temperature Error on Measured EA

Considering all the possible circumstances mentioned above that could

result in an erroneous temperature measurement, it would at this time be good to look at the answer to the following question. What effect would a difference between measured and actual sample temperature have on the calculated activation energy? Consider Figure 4.18 which is a typical storage time versus 1000/T plot seen for the devices measured from lot A. The solid line represents the "measured" storage times for a device. The plot is of the form:

$$y = Cexp\left[\frac{E_A}{kT}\right] \tag{4.14}$$

From the equation above, for temperatures  $\mathbf{T_1}$  and  $\mathbf{T_2}$  the following is obtained:

$$\tau_1 = \text{Cexp}\left[\frac{E_A}{kT_1}\right] \tag{4.15}$$

$$\tau_2 = \text{Cexp}\left[\frac{\mathsf{E}_{\mathsf{A}}}{\mathsf{kT}_2}\right] \tag{4.16}$$

If (4.15) is divided by (4.16) and rearranged a relationship between  $\tau_1$  and  $\tau_2$  is obtained.

$$\tau_1 = \tau_2 \exp\left[\frac{E_A}{k} \left[\frac{1}{T_1} - \frac{1}{T_2}\right]\right]$$
 (4.17)

Manipulation of (4.17) gives a relationship between  $T_1$  and  $T_2$ :

$$\frac{1}{T_2} = \frac{1}{T_1} + \frac{k}{E_A} \ln \left[ \frac{\tau_2}{\tau_1} \right] \tag{4.18}$$

An activation energy of 0.66 eV is calculated from the measured storage times of the device in Figure 4.18. It is also known that at a measured temperature of  $T_2$  = 403 K the storage time is  $\tau_2$  = 370 seconds. Assuming room temperature is  $T_{room}$  =  $T_1$  = 296 K and using equation (4.17) along with the values for  $T_2$  and  $\tau_2$  obtained above, it is seen that the storage time at room

temperature would be  $\tau_{room} = 3.564 \times 10^5$  seconds.

Now, make the assumption that the theoretical activation energy should be half bandgap,  $E_A = 1.45$  eV, and ignore any effects other than temperature variation between the "measured" and "theoretical" results. Using (4.18), the value of  $\tau_{room}$ , and the value of  $\tau_2$  a new value  $T_2$  is obtained. Note that there should be no difference between "measured" and "theoretical" temperatures at room temperature.  $T_2$ ' would be the "theoretical" temperature for a storage time of 370 seconds if the activation energy is 1.45 eV. The value obtained for T2' is 337 K. If the difference between measured  $T_2$  and "theoretical"  $T_2$ ' is taken, it is seen that it would take a difference of 66 °C in order to change EA from 0.66 eV to 1.45 eV in the temperature range around 130 °C. This large value indicates that the reduction in activation energy in lot A is unlikely to be caused from an error in temperature measurement. If it is assumed in a worse case scenario that the difference between measured and "actual" temperature is 10 °C in the temperature range around 130 °C, (4.18) can be used to see that the decrease in activation energy due to using the "measured" temperature would be 0.05 eV. Thus, it is seen that if a temperature difference did in fact exist, its effect on the activation energy is much too small to alone account for the low activation energies measured in lot A.

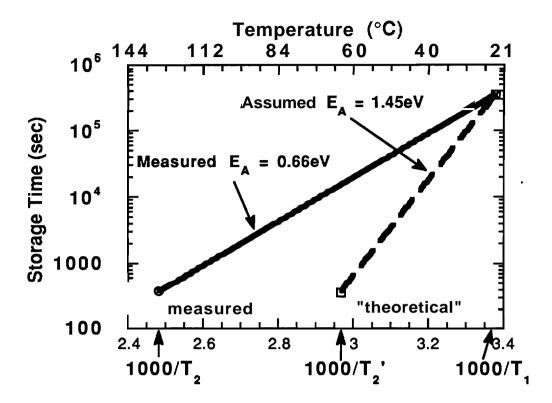


Figure 4.18 Storage time versus 1000/T plot for a typical measured device from lot A with  $E_A = 0.66 \, \text{eV}$ , and that obtained if a half bandgap activation energy of  $E_A = 1.45 \, \text{eV}$  is assumed. This figure shows that it would take a large error in temperature measurement to account for the lower than expected activation energy in lot A.

#### **CHAPTER 5 - CONCLUSION**

#### 5.1 Introduction

Comparison of storage times and generation currents in devices passivated with dry and wet  $O_2$  are presented in the first part of the chapter. The end of the chapter contains a conclusion and recommendations for further research.

# 5.2 Comparison of Devices Passivated with Wet and Dry O2

A comparison between the storage times of the devices from lot A (dry  $O_2$ ) and lot B (wet  $O_2$ ) can be obtained by extrapolating the storage time versus 1000/T curve of the (3,20) 3 mil device from Figure 4.9 and relating it to a device from figure 4.2. The result of the extrapolation is presented in Figure 5.1. This figure shows that the storage times of the device passivated with wet  $O_2$  are approximately five orders of magnitude larger than those from the device passivated with dry  $O_2$ .

Devices from lot A and lot B are dominated by perimeter generation as was seen in sections 4.2.3 and 4.3.4. As might be expected from the comparison of storage times given above, the magnitude of perimeter generation in devices passivated with dry  $O_2$  is larger than that in devices passivated with wet  $O_2$ . Figure 5.2 is a combination of Figure 4.6 and

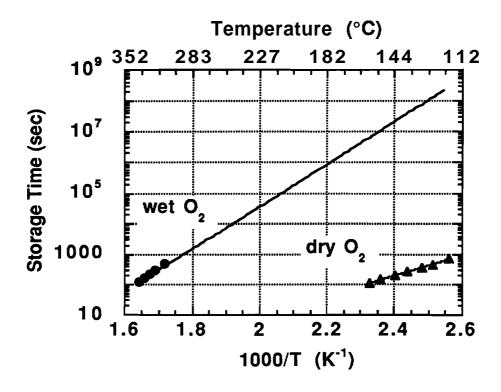


Figure 5.1 Comparison of storage times in 3 mil devices devices passivated with wet and dry oxidations.

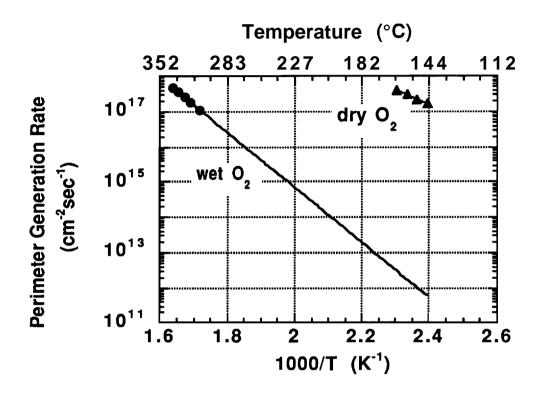


Figure 5.2 Comparison of perimeter generation in devices passivated with wet and dry oxidations.

Figure 4.11 extrapolated back to 140  $^{\circ}$ C. It shows a five order of magnitude decrease in perimeter generation rate for wet  $O_2$  devices. This corresponds very well with the five order of magnitude increase in storage time.

The improvement of device characteristics obtained by using wet  $O_2$  instead of dry  $O_2$  is not unexpected. It was mentioned in section 4.3.1 that Tang, et. al. observed wet  $O_2$  to yield better MOS electrical characteristics on (100)  $\beta$ -SiC than dry oxidation. The density of interface traps for dry oxides were orders of magnitude larger than those for wet oxides [17].

It should be noted that the extrapolation of the wet  $O_2$  data to lower temperatures is a best case scenario. Figure 5.3 shows that an actual measurement performed on a device at 250 °C resulted in a storage time slightly below the extrapolated value. This indicates the possibility of other leakage current mechanisms coming into effect at lower temperatures. Even so, the wet  $O_2$  passivated devices are still better than those passivated with dry  $O_2$ .

#### 5.3 Conclusion

In conclusion, this thesis presented results of the first research done on 6H-SiC n-i-p-i-n storage capacitors. Devices with surfaces passivated by dry and wet  $O_2$  were considered. Perimeter generation was the dorninant source of leakage current for both cases. The devices passivated with wet  $O_2$  demonstrated longer storage times and smaller leakage currents than those passivated with dry  $O_2$ . Charge recovery times of the SiC devices are the longest ever reported for any semiconductor device. They are far superior to devices of similar structure in GaAs and AlGaAs, Figure 5.4 [6]. These SiC devices show great promise for high temperature applications and even offer

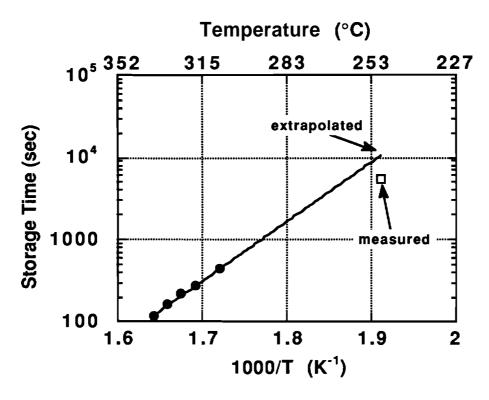


Figure 5.3 Comparison of extrapolated and measured values of storage time for a 3 mil device passivated with wet  $\rm O_2$ .

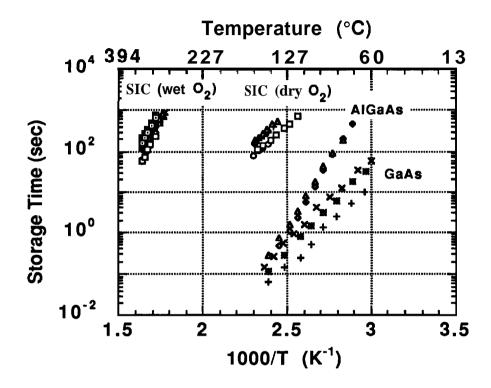


Figure 5.4 Storage time comparison for SiC, AlGaAs, and GaAs.

the possibility of building a one-transistor DRAM that would be static and non-volatile at room temperature.

#### 5.4 Recommendations for Further Research

Since perimeter generation is the dominant leakage mechanism for devices passivated with both wet and dry  $O_2$  passivations, it would be worthwhile to investigate other possible ways to reduce its effect. Different doping profiles need to be investigated in order to obtain the optimum device. Finally, measurements need to be performed at room temperature to determine if these devices can actually be used as static, nonvolatile memories.

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