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On-State Characteristics of SiC Power UMOSFETs on 115- μm Drift Layers

Y. Sui, T. Tsuji, and J. A. Cooper, Jr.

Abstract—We describe the on-state performance of trench oxide-protected SiC UMOSFETs on 115- μm -thick n-type 4H-SiC epilayers designed for blocking voltages up to 14 kV. An on-state current density of 137 A/cm² and specific on-resistance of 228 m Ω ·cm² are achieved at a gate bias of 40 V (oxide field of 2.67 MV/cm). The effect of current spreading on the specific on-resistance for finite-dimension devices is investigated, and appropriate corrections are made.

Index Terms—High voltage, power transistors, silicon carbide, wide bandgap.

I. INTRODUCTION

IN RECENT YEARS, 4H-SiC power MOSFETs have been recognized as attractive devices for high-voltage switching applications because of the low specific on-resistance and high breakdown electrical field of 4H-SiC [1]. Recently, Ryu *et al.* reported 10 kV DMOSFETs with specific on-resistance of 236 m Ω ·cm² on 115- μm -thick n-type epilayers [2]. In this letter, we report the first UMOSFETs built on 115- μm -thick 4H-SiC epilayers. These UMOSFETs exhibit specific on-resistance of 228 m Ω ·cm², demonstrating that vertical channel UMOS devices can provide on-state performance comparable or superior to that of DMOSFETs.

II. EXPERIMENTAL

A schematic cross section of the experimental device is shown in Fig. 1. A 115- μm -thick, 7.5×10^{14} cm⁻³ n-type epilayer is first grown on a (0001) n+ 4H-SiC substrate, cut 8° off-axis, followed by a 0.4 μm 2×10^{17} cm⁻³ n-type current spreading epilayer [3] and a 1.5 μm 2×10^{17} cm⁻³ p-type epilayer to form the base region of the UMOSFET. Source contacts are formed by implanting 4×10^{15} cm⁻² nitrogen at 650 °C using a Ti–Au mask. A three-zone junction termination extension (JTE) [4] edge termination is formed by Al implantation, with widths/doses of 100 $\mu\text{m}/2.4 \times 10^{13}$ cm⁻², 100 $\mu\text{m}/1.6 \times 10^{13}$ cm⁻², and 100 $\mu\text{m}/8 \times 10^{12}$ cm⁻², respectively.

Gate trenches approximately 2 μm deep are formed by reactive ion etching (RIE) in SF₆ using a Ni mask. Sacrificial oxidations are performed to smooth the trench sidewalls. Aluminum

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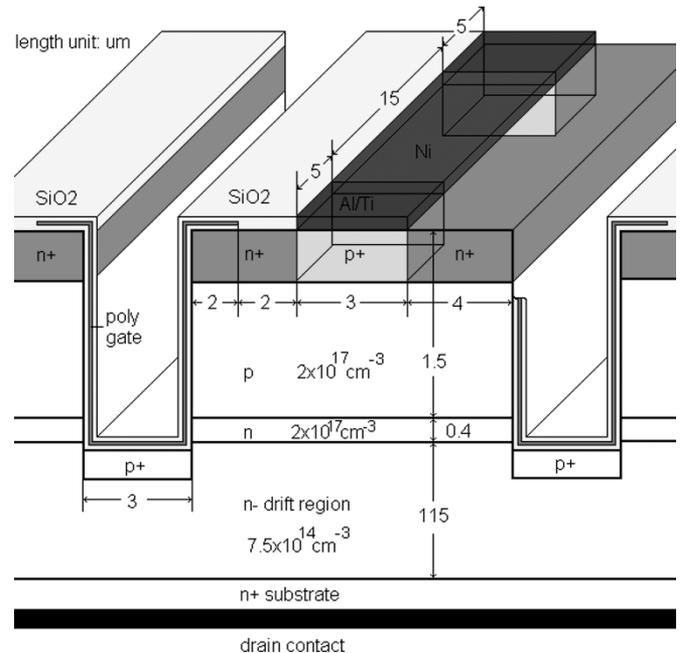


Fig. 1. Schematic cross section of the 4H-SiC UMOSFET. Doping levels and dimensions (in micrometers) are given in the figure. P+ implants and Ti-Al contacts to p+ implants are discrete islands along each source finger. Ni contacts to the n+ implants lie between the Ti/Al contacts. The cell pitch is 14 μm . JTE edge terminations, contacts to the polysilicon gate and contacts to the p+ trench implants are not shown.

(1.8×10^{14} cm⁻², 650 °C) is implanted into the trench bottom to protect the trench oxide from high electrical fields in the blocking state [5]. It is important to implement the n-type current spreading layer together with the trench bottom implant to minimize the JFET effect at the top of the n-drift layer. Without a current spreading layer, the portion of the n-drift layer between the p+ trench implant and the p+ base epilayer is depleted at high gate voltage, blocking the current path to the drain, which results in very high on-resistance. An additional JFET is formed between adjacent p+ trench implants, but the separation between p+ implants is sufficiently large (11 μm in this case) that the added resistance is negligible, as verified by computer simulations. All implants are annealed at 1600 °C in SiH₄ for 40 min.

To avoid anisotropic thermal oxidation of SiC, polycrystalline Si is deposited by low pressure chemical vapor deposition (LPCVD) at 600 °C and oxidized at 950 °C in wet O₂ for 2 h to produce a uniform oxide of 150-nm thickness on the sidewalls and bottom of the trench. A nitric oxide (NO) anneal is performed at 1100 °C after gate oxidation to improve the channel mobility and reduce interface state density [6], [7]. N-type source contacts are formed by depositing 100-nm

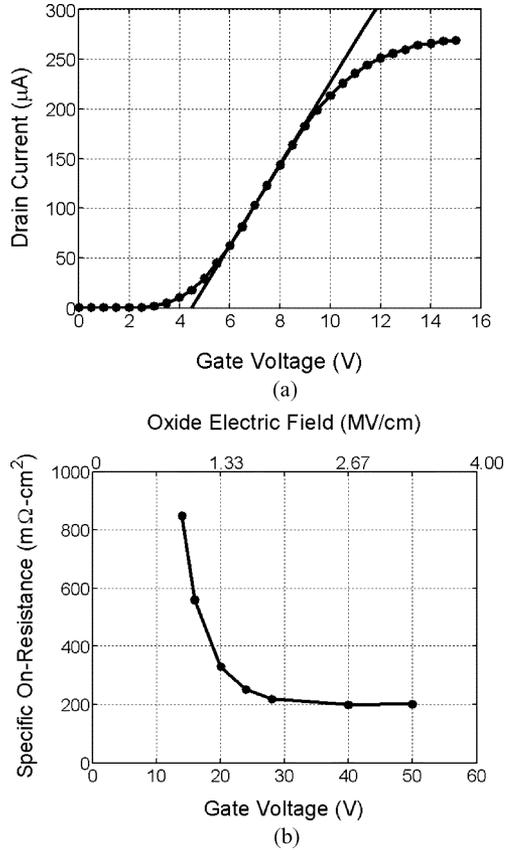


Fig. 2. (a) $I_d - V_{gs}$ characteristics of a small UMOSFET. A threshold voltage of 4.5 V is extrapolated from the linear region of the curve. A drain voltage of 50 mV is used for the measurement. (b) Specific on-resistance versus gate voltage for these devices.

Ni, and p-type base contacts are formed by depositing 33-nm Ti/167-nm Al. Contact to the drain is made by depositing 100-nm Ni on the back side of the wafer. All contacts are annealed at 900 °C in vacuum for 4 min. Finally, 900 nm of Al top metal is deposited and patterned, such that source and p-base are connected together.

The room-temperature linear region I_d versus V_{gs} characteristic of a UMOSFET with area of $7.74 \times 10^{-3} \text{ cm}^2$ is shown in Fig. 2(a), measured at a drain voltage of 50 mV. A threshold voltage of 4.5 V is extracted from the linear portion of the curve. Fig. 2(b) shows the specific on-resistance ($R_{on,sp}$) as a function of gate bias or oxide electric field. The on-resistance is calculated from the slope of the $I_d - V_{ds}$ characteristic in the linear region (c.f. Fig. 3). As the gate bias increases, the channel resistance is reduced, and the total specific on-resistance saturates for gate bias greater than 40 V. Because of the lightly doped thick drift layer, at this point the drift region resistance is dominant.

Fig. 3 shows the room temperature on-state $I_d - V_{ds}$ characteristics of a 4H-SiC UMOSFET with an active area of 0.0179 cm^2 . This device carries a current of 2.5 A (137 A/cm^2) at a forward voltage of 30 V. From the slope of the $I - V$ characteristics in the linear region, the specific on-resistance is measured to be $206 \text{ m}\Omega \cdot \text{cm}^2$ (uncorrected for current spreading in the drift layer). E_{ox} is maintained below 3 MV/cm ($V_{gs} = 45 \text{ V}$), although it has been reported that oxide layers in 4H-SiC MOSFETs are reliable for E_{ox} up to 4 MV/cm [8].

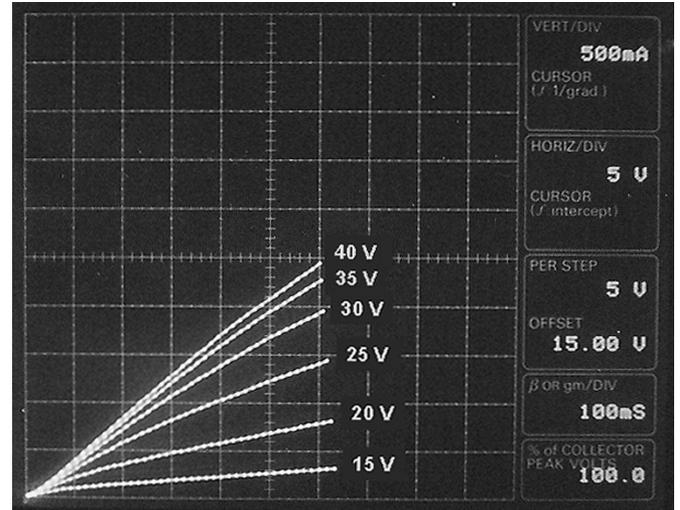


Fig. 3. $I_d - V_{ds}$ characteristic of a 4H-SiC UMOSFET with active area of 0.0179 cm^2 . The on-resistance, given by the slope of the $I_d - V_{ds}$ curve in the linear region, saturates at a gate bias of 40 V, where $E_{ox} = 2.67 \text{ MV/cm}$. A current density of 137 A/cm^2 is reached at $V_{gs} = 40 \text{ V}$ and $V_{ds} = 30 \text{ V}$.

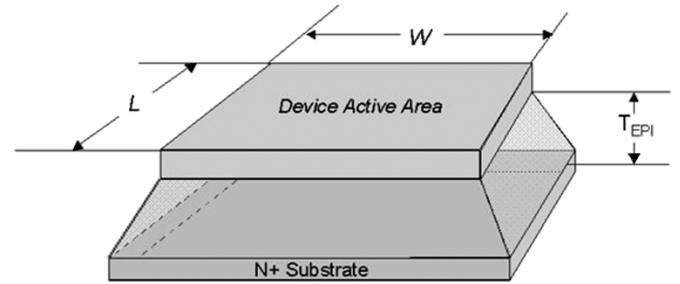


Fig. 4. Model for calculating current spreading effect in the thick drift layer. The spreading angle is taken to be 45° and the active device area is assumed to be rectangular.

To obtain the true specific on-resistance, we have to account for the fact that current spreading in the drift region artificially lowers the specific on-resistance of a finite-dimension device. The current spreading effect can be modeled using a trapezoidal structure, as shown in Fig. 4. Consider the total specific on-resistance consisting of the drift region resistance ($R_{d,sp}$) and the source/channel/contact resistance ($R_{other,sp}$). Assume $R_{on,sp}$ is the specific on-resistance for an infinitely large device, where the current spreading effect is negligible, and $R_{on,sp}^{meas}$ is the measured (apparent) specific on-resistance for a finite dimension device. The $R_{other,sp}$ components of the two specific on-resistances are the same, but the drift region resistances are different. By comparing the two specific on-resistances, we can eliminate $R_{other,sp}$ and write

$$R_{on,sp} = R_{on,sp}^{meas} + R_{d,sp}(1 - \alpha) \quad (1)$$

where α is the ratio of $R_{d,sp}^{meas}/R_{d,sp}$. For an n-type doping of $7.5 \times 10^{14} \text{ cm}^{-3}$, the mobility μ_N in the bulk drift layer is $937 \text{ cm}^2/\text{Vs}$ [9]. This allows us to calculate $R_{d,sp}$ to be $102 \text{ m}\Omega \cdot \text{cm}^2$. With the geometry of the actual UMOSFETs, α is calculated to be 0.78 [10], [11]. For the measured $R_{on,sp}^{meas} = 206 \text{ m}\Omega \cdot \text{cm}^2$, the specific on-resistance after correction for current spreading is $R_{on,sp} = 206 + 102 \times (1 - 0.78) = 228 \text{ m}\Omega \cdot \text{cm}^2$. The $228 \text{ m}\Omega \cdot \text{cm}^2$

specific on-resistance is the lowest reported value for 4H-SiC MOSFETs with 115- μm blocking epilayers.

As mentioned earlier, blocking layers of the doping and thickness used here are theoretically capable of blocking 14 kV, and have actually been demonstrated to block 10 kV [2]. However, problems with the edge terminations in the present devices limited our blocking voltage to just over 5 kV.

III. CONCLUSION

On-state characteristics of 228 $\text{m}\Omega \cdot \text{cm}^2$ 4H-SiC power UMOSFETs built on 115 μm blocking epilayer are demonstrated. The specific on-resistance is comparable to the best reported values for 4H-SiC DMOSFETs on a similar epilayer. Drift layer current spreading has been removed from calculations of specific on-resistance.

REFERENCES

- [1] A. Agarwal, S. H. Ryu, and J. Palmour, *Silicon Carbide, Recent Major Advances*, W. J. Choyke, Ed. Berlin, Germany: Springer-Verlag, 2004, pp. 785–812.
- [2] S. H. Ryu, S. Krishnaswami, A. Agarwal, J. Richmond, and J. Palmour, "Development of 10 kV 4H-SiC power DMOSFETs," in *Mater. Sci. For.*, vol. 457–460, 2004, pp. 1385–1388.
- [3] J. Tan, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage accumulation-layer UMOSFETs in 4H-SiC," *IEEE Electron Device Lett.*, vol. 19, no. 5, pp. 487–489, May 1998.
- [4] V. A. K. Temple, "Increased available breakdown voltage and controlled surface electric fields using a junction termination extension (JTE) technique," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 954–957, 1983.
- [5] J. A. Cooper, Jr., "Structure for Increasing the Maximum Voltage of Silicon Carbide UMOS Power Transistors," U.S. Patent 6 180 958, Jan. 30, 2001.
- [6] J. R. Williams, G. Y. Chung, C. C. Tin, K. McDonald, D. Farmer, R. K. Chanana, R. A. Weller, S. T. Pantelides, O. W. Holland, M. K. Das, L. A. Lipkin, and L. C. Feldman, "Nitrogen passivation of the interface states near the conduction band edge in 4H-silicon carbide," in *Proc. Materials Research Society Symp.*, vol. 640, 2001, pp. H.3.5.1–H.3.5.12.
- [7] I. Khan, J. A. Cooper Jr., T. Isaacs-Smith, J. R. Williams, and L. C. Feldman, "The effect of crystal orientation and post-oxidation NO anneal on inversion layer electron mobility in 4H-SiC UMOSFETs," presented at the Electronic Materials Conf., Santa Barbara, CA, Jun. 26–28, 2002.
- [8] D. Stephani, "Recent progress in the development of SiC power switches," presented at the Int. Conf. Silicon Carbide and Related Materials, Lyon, France, Oct. 5–10, 2003.
- [9] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 1442–1447, Dec. 2001.
- [10] I. Khan, "High voltage SiC UMOSFETs," Ph.D. dissertation, Purdue Univ., West Lafayette, IN, Aug. 2002.
- [11] I. Khan, J. A. Cooper, Jr., M. A. Capano, T. Isaacs-Smith, and J. R. Williams, "High voltage UMOSFETs in 4H SiC," presented at the *Int. Symp. Power Semiconductor Devices and ICs*, Santa Fe, NM, Jun. 4–7, 2002.