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Effects of bias stress on ZnO nanowire field-effect transistors fabricated with organic gate nanodielectrics

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The effects of bias stress (gate stress or drain stress) on nanowire field-effect transistor (NW-FET) stability were investigated as a function of stress bias and stress time. The *n*-channel NW-FETs used a nanoscopic self-assembled organic gate insulator, and each device contained a single ZnO nanowire. Before stress, the off current is limited by a leakage current in the 1 nA range, which increases as the gate to source bias becomes increasingly negative. The devices also exhibited significant changes in threshold voltage (V_{th}) and off current over 500 repeated measurement sweeps. The leakage current was significantly reduced after gate stress, but not after drain stress. V_{th} variations observed upon successive bias sweeps for devices following gate stress or drain stress were smaller than the V_{th} variation of unstressed devices. These observations suggest that gate stress and drain stress modify the ZnO nanowire-gate insulator interface, which can reduce electron trapping at the surface and therefore reduce the off current levels and variations in V_{th}. These results confirm that gate and drain stresses are effective means to stabilize device operation and provide high performance transistors with impressive reliabilities. © *2006 American Institute of Physics*.
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Nanowire field-effect transistors (NW-FETs) have been the focus of intense research in recent years due to their proven applications in ring oscillators, gas sensors, DNA sensors, flexible devices, and memory devices.[1–4] Even though many studies have addressed the mobility, on-off current ratio, and contact resistance (Schottky contact) of NW-FETs, there have not been extensive investigations of reliability issues. Device reliability is one of the important issues for NW-FET output (*IV*) characteristics. Reduction of leakage current and minimization of threshold voltage variations are crucial issues for complementary metal-oxide-semiconductor (CMOS) technologies. However, the nanowire transistors reported to date have typically utilized metal source/drain contacts and planar gating geometries, and metal contacts allow both electron and hole injections, depending on the polarity of the gate bias. This ambipolar conduction is known to result in high off currents in Si nanowire and carbon nanotube transistors,[5] making it difficult to achieve high on-off current ratios in devices based on these materials. In this sense, optimized bias stress can be a valuable tool for nanowire device stabilization, especially for removing leakage current and minimizing threshold voltage variation. Gate stress and drain stress have been observed to degrade transistor performance in metal-oxide-semiconductor field-effect transistors (MOSFETs).[6,7] However, these methods can also be used to improve transistor stability and lifetime. Even though short time gate stress or drain stress can initially degrade device metrics, they can provide improved current-voltage (*IV*) output characteristics and longer device lifetimes. For instance, drain stress is effective for removing kick effects and gate stress is effective for removing leakage currents for polysilicon thin-film transistors (TFTs).[8]

In this study, we report the effects of gate stress and drain stress on the stability and reliability of ZnO NW-FETs using a self-assembled nanodielectric (SAND) organic gate insulator. The aims of this study are to: (i) examine the performance reliability of ZnO nanowire FETs after moderate dc voltage drain stress and moderate dc voltage gate stress, (ii) minimize leakage current and threshold voltage shift, and (iii) investigate the degradation mechanisms of ZnO NW-FETs. For optimized gate-stress and drain-stress conditions, it will be seen that we achieve significantly enhanced device performance in terms of low and stable off currents, constant subthreshold slopes and mobilities, and minimum threshold voltage variations.

Single ZnO NW-FET devices were fabricated using a 15 nm SAND as the gate insulator. The cross section of the SAND-based ZnO NW-FET device, along with the structure of the SAND film, are shown in Fig. 1. The SAND films used in this study consist of three layer-by-layer self-assembled organic multilayers; this structure has been shown to be a high performance gate insulator ($C_i \sim 180$ nF/cm^2, $V_{breakdown} \sim 7$ MV/cm, and $I_{leakage} \sim 1 \times 10^{-8}$ A/cm^2 at 1 V).[9] The average diameter and length of the ZnO nanowires (Nanolab Inc.) are 120 nm and 5 μm, respectively. The ZnO nanowire dispersion was transferred onto SAND-coated Si wafer substrates. Aluminum metal for source/drain contacts was deposited by e-beam evaporation. Subsequently, the ZnO NW-FET devices were subjected to an ozone treatment (UVO 42-220, Jelight Co. Ltd.) for 1 min to achieve the highest device performance in terms of outstanding on-off current ratio ($\sim 10^7$) and subthreshold slope (~ 130 mV/decade). The devices were passivated with SiO_2

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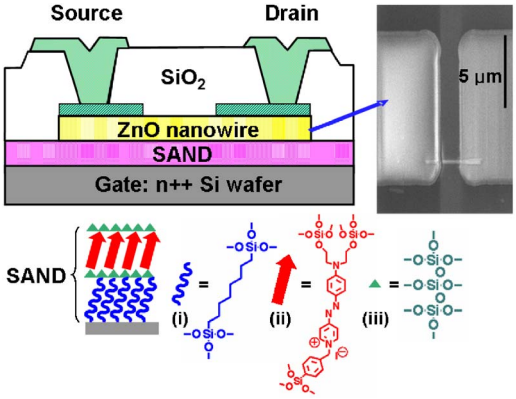

FIG. 1. (Color online) Cross-sectional view of SAND-based ZnO NW-FET device structure, along with top-view scanning electron micrograph, type-III SAND structure, and component building blocks: (i) α,ω-difunctionalized hydrocarbon chain, (ii) stilbazolium π-electron layer, and (iii) trisiloxane capping layer.

to prevent contamination from air/moisture. The current-voltage (IV) characteristics of the devices were measured using a probe station with an HP 4156A semiconductor parameter analyzer, both before and after the gate-stress and drain-stress procedures.

Representative SAND-based single ZnO NW-FETs (length ~120) were used to examine bias-stress effects. The drain current versus gate-source voltage (I_{ds}-V_{gs}) characteristics of each device were recorded during 500 successive measurements. Devices were characterized before stress, and following drain stress at V_{ds}=4 V and V_{gs}=2 V for 30 s, or gate stress at V_{ds}=2 V and V_{gs}=−6 V for 30 s. Figure 2 shows the I_{ds}-V_{gs} curves of two SAND-based ZnO NW-FETs before and after applying gate stress or drain stress. The I_{ds}-V_{gs} curves before and after gate stress in Fig. 2(a) show that, before stress, the devices exhibit a leakage current in the 1 nA range which increases as the gate to source voltage becomes increasingly negative. The leakage current is minimized upon gate stress and remains at $\sim 2.0\times 10^{-11}$ A during 500 successive measurements. Figure 2(b) shows the I_{ds}-V_{gs} curve before and after drain stress. Leakage current of the device is not reduced after drain stress. This indicates that drain stress is not effective in removing leakage current. We also applied higher gate stress (V_{ds}=4 V and V_{gs}=−9 V for 30 s), but the I_{ds}-V_{gs} curve degrades, presumably because of damage to the device.

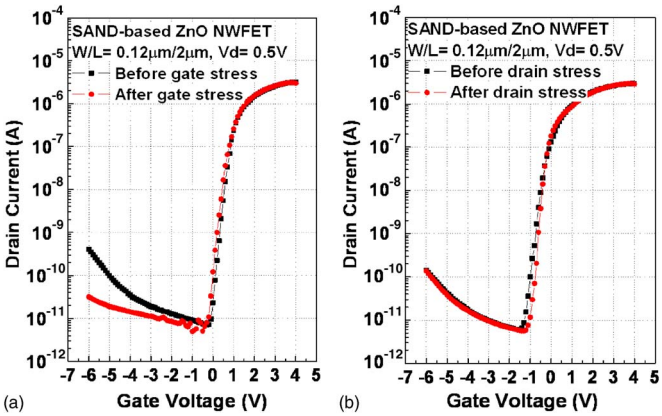

FIG. 2. (Color online) I_{ds}-V_{gs} characteristics of SAND-based ZnO NW-FETs before and after bias-stress processing for (a) gate stress and (b) drain stress.

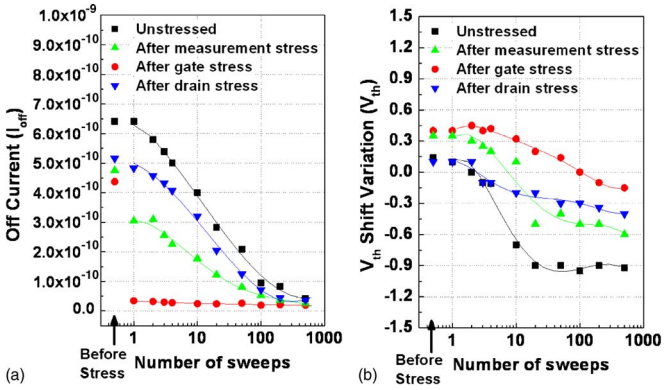

FIG. 3. (Color online) Off current and threshold voltage variations observed for ZnO NW-FETs in successive sweeps following bias stress. (a) Off current (I_{off}) vs number of sweeps. (b) V_{th} shift variation (ΔV_{th}) vs number of sweeps.

Figure 3(a) shows the off current variation of four ZnO NW-FET devices during 500 successive measurements. Over the 500 sweeps, the measured off current at −6 V drops from 6.4×10^{-10} to 4.2×10^{-11} A in the case of the unstressed device, from 3.0×10^{-10} to 2.4×10^{-11} A after measurement stress, and from 4.9×10^{-10} to 1.75×10^{-11} A after drain stress. The off current of the gate stressed device is initially small and remains at $\sim 2.7\times 10^{-11}$ ($\pm 0.7\times 10^{-11}$) A during the 500 measurement sweeps. This indicates that gate stress is effective in reducing the off current of ZnO NW-FETs.

Since the measurement sweeps also involve application of both gate and drain voltages, it is important to consider whether the cumulative bias exposure during the measurement sweeps is sufficient to induce significant stress effects on the device. The measurement sweeps are performed at constant V_{ds}=0.5 V, and V_{gs} values ranged up to the same voltage as the gate stress (−6 V). Although it is difficult to predict the cumulative effects of biasing at other bias points, the net time spent at the −6 V bias point during 500 measurement sweeps is approximately 1 s, so the net stress induced in a series of measurements is expected to be significantly less than that in the gate stress procedure. In order to confirm this observation, a device was initially stressed with V_{gs}=−6 V, V_{ds}=0.5 V for 30 s [Fig. 3(a)]. Note that this stress condition corresponds to the same drain bias and maximum negative gate bias applied during a measurement sweep and is therefore denoted a "measurement stress". The current on-off ratios measured following this measurement stress indicate that biasing at this lower drain-source bias does not provide the same effect as the full gate stress procedure.

Threshold voltage variations (ΔV_{th}) of four ZnO NW-FET devices are shown in Fig. 3(b). The initial threshold voltages of these devices were 0.1, 0.1, 0.3, and 0.4 V, respectively. V_{th} variations of stressed ZnO NW-FETs during 500 measurement sweeps for the devices following drain stress ($\Delta V_{th}\sim -0.5V_{th}$) and gate stress ($\Delta V_{th}\sim -0.5V_{th}$) were significantly smaller than the V_{th} variation of the unstressed device ($\Delta V_{th}\sim -1.0V_{th}$) and the bias-stressed device. In the case of unstressed SAND-based ZnO NW-FETs, V_{th} is shifted by ~−1.0 V and the off current is decreased by one order of magnitude over the 500 measurement sweeps. The initial V_{th} shift in the negative direction is also smaller than the unstressed devices during the first ten measurement sweeps. The initial rapid V_{th} shift over the first ten measurement sweeps is tentatively ascribed to mobile charges in the

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SAND. The observation of comparable effects following bias stress implies that the bias effect during measurement is different from gate stress or drain stress. It can be seen that drain stress is somewhat effective for minimizing V_{th} shift, but not for reducing off current. However, gate stress is more effective for removing off current leakage and reducing V_{th} shift simultaneously.

The behavior following bias stress can provide insights into which of the possible mechanisms dominate the off current and threshold voltage shifts in the NW-FETs. One possible mechanism is gate leakage due to electron tunneling through the gate dielectric during the application of a gate voltage. However, since the leakage current of the SAND gate dielectrics ($I_{leakage}$) in this study is ~40 pA at −6 V, the tunneling current should be negligible. Ambipolar effects can be significant in NW transistors with Schottky contacts, which allow both electron and hole injections, and result in high off currents. However, the reduction in leakage current after gate stress in the present devices indicates that ambipolar effects are not significant here. The most probable mechanisms then involve interface traps (between the ZnO NW and the SAND) or surface states (between ZnO NW and the SiO_2 passivation layer), which would result in conduction via gate-induced drain leakage, as well as shifts in V_{th}. Since nanowire devices have a relatively large surface: volume ratios compared to bulk transistors, their electrical characteristics can be very sensitive to interface states. It is suggested that bias stress modifies the ZnO NW—gate dielectric interface, and possibly the ZnO NW—source/drain metal interface. The bias stress, especially gate stress, can reduce the interface trap density and consequently reduce the leakage current. In addition, the elimination of leakage current after gate stress could be explained by changes in the surface barrier of the ZnO NW-FETs. The surface barrier may be increased after bias stress, which would reduce the number of trapped electrons at the surface, which can tunnel from the gate under gate biases.

The extracted V_{th} shifts can be confirmed by using the defect pool model,[6,10,11] i.e., Eq. (1) where A and β are temperature dependent parameters, V_{gs} is the gate bias voltage, V_{th_before} is the V_{th} of the ZnO NW-FET before bias stress applied, and t is the bias-stress time duration. The V_{th} shift is proportional to the amount of induced carriers in the ZnO NW channel. It can be estimated that the degradation during operation is caused by self-heating because the temperature of NW-FETs increases during switch-on.[12]

$$\Delta V_T(t) = A(V_{gs} - V_{th_before})t^{\beta}. \quad (1)$$

Figure 4(a) shows the family of I_{ds}-V_{gs} characteristics for the gate-stressed device. The I_{ds}-V_{gs} curves demonstrate an on-off current ratio of $\sim 10^6$, a subthreshold slope of ~130 mV/decade, and a mobility of ~1200 $cm^2/V\,s$. The drain current (I_{ds}) versus drain-source voltage (V_{ds}) characteristics of a gate-stressed ZnO NW-FET device using a 15 nm SAND gate dielectric after 500 measurement sweeps are shown in Fig. 4(b), exhibiting typical transistor characteristics with a well-defined saturation region. The device exhibits a low operating voltage (~2.1 V) and high on current (~1.75 μA per ZnO NW at V_{ds}=1.0 V, V_{gs}=2.1 V). These results demonstrate that the applied gate stress greatly stabilizes the devices during subsequent transistor.

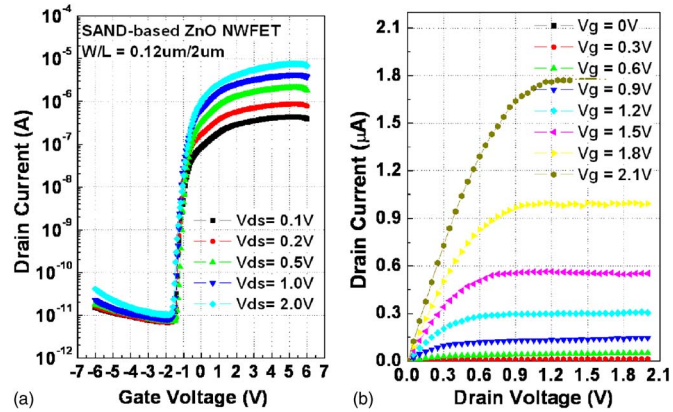

FIG. 4. (Color online) ZnO NW-TFT output modification by gate stress. (a) I_{ds}-V_{gs} characteristics for different V_{ds} from 0.1 to 1.0 V. (b) I_{ds}-V_{ds} characteristics.

The effects of gate stress or drain stress on ZnO NW-FETs with SAND gate dielectrics have been characterized, and for repeated measurements, degradation of device parameters by applied stress bias is found to be smaller than for unstressed devices. Gate stress and drain stress are shown to afford the minimum threshold voltage variation and to reduce the off current of the devices. The drain stress is effective in reducing the V_{th} variation, but does not reduce the off current. The gate stress is effective in minimizing the off current and the V_{th} variation of the ZnO NW-FETs simultaneously. Potential mechanisms for the improvements observed following gate stress and drain stress have been discussed. Since low V_{th} variation and low off current are essential in all CMOS-like transistor technologies, gate-stress and drain-stress are clearly important strategies for the optimization of high performance transistors with high reliabilities.

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