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Substrate engineering for high-performance surface-channel III-V metal-oxide-semiconductor field-effect transistors

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High-performance inversion-type enhancement-mode In$_{0.65}$Ga$_{0.35}$As metal-oxide-semiconductor field-effect transistors (MOSFETs) with atomic-layer-deposited Al$_2$O$_3$ as gate dielectric are demonstrated. A 0.5 μm gate-length MOSFET with an Al$_2$O$_3$ gate oxide thickness of 10 nm shows a gate leakage current less than $5 \times 10^{-6}$ A/cm$^2$ at 4 V gate bias, a threshold voltage of 0.40 V, a maximum drain current of 670 mA/mm, and transconductance of 230 mS/mm at drain voltage of 2 V. More importantly, a model is proposed to ascribe this 80% improvement of device performance from In$_{0.53}$Ga$_{0.47}$As MOSFETs mainly to lowering the energy level difference between the charge neutrality level and conduction band minimum for In$_{0.65}$Ga$_{0.35}$As. The right substrate or channel engineering is the main reason for the high performance of the devices besides the high-quality oxide-semiconductor interface.


Silicon-based technology will encounter physical and technical limits within the next decade, which motivates the semiconductor industry to explore alternative device technologies such as Ge, III-Vs, and carbon nanotubes to replace silicon as active channel materials. In the past four decades, great efforts have been made to search for low-defect, thermodynamically stable insulators for III-V metal-oxide-semiconductor field-effect transistors (MOSFETs). Although some high-performance depletion-mode (D-mode) III-V MOSFETs have been demonstrated previously, the reported inversion-type enhancement-mode (E-mode) III-V MOSFETs suffer from low drain currents. There are only two exceptions in the literature. One is molecular beam epitaxy (MBE) grown Ga$_2$O$_3$(Ga$_2$O$_3$)$_x$/In$_{0.53}$Ga$_{0.47}$As MOSFET with maximum drain current of 360 mA/mm; another one is atomic layer deposition (ALD) grown Al$_2$O$_3$, HfO$_2$, or HfAlO/In$_{0.53}$Ga$_{0.47}$As MOSFETs with maximum drain current of 367–430 mA/mm. 

In this letter, we report high-performance inversion-type E-mode In$_{0.65}$Ga$_{0.35}$As MOSFETs using ALD Al$_2$O$_3$ as gate dielectric. The maximum drain current of 670 mA/mm and extrinsic transconductance of 230 mS/mm for a 0.5 μm gate-length MOSFET are achieved, which have about 80% improvement over previously reported inversion-type E-mode In$_{0.53}$Ga$_{0.47}$As MOSFETs. It is reasonable to believe that the interface quality of Al$_2$O$_3$/In$_{0.65}$Ga$_{0.35}$As and Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As is similar due to the similar surface chemistry during the pretreatment and ALD process. 12% In concentration difference should not change the interface quality dramatically. To explain this dramatic improvement of device performance, a charge neutrality level (CNL) based model is proposed. It shows that III-V channel or substrate itself, which attracts less attention in the past, is the main determinant for III-V MOSFETs’ maximum drain current and, thus, device performance.

Figure 1(a) shows the cross section schematic of the device structure of an ALD Al$_2$O$_3$/In$_{0.65}$Ga$_{0.35}$As MOSFET. A 500 nm p-doped $4 \times 10^{17}$ cm$^{-3}$ buffer layer, a 300 nm p-doped $1 \times 10^{17}$ cm$^{-3}$ In$_{0.53}$Ga$_{0.47}$As transition layer, and a 20 nm p-doped $1 \times 10^{17}$ cm$^{-3}$ strained In$_{0.65}$Ga$_{0.35}$As channel layer were sequentially grown by MBE on a 2 in. InP p+ substrate. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30-nm-thick Al$_2$O$_3$ layer was deposited at a substrate temperature of 300 °C as an encapsulation layer. For device fabrication, source and drain regions were selectively implanted with a Si dose of $1 \times 10^{14}$ cm$^{-2}$ at 30 keV and $1 \times 10^{14}$ cm$^{-2}$ at 80 keV through the 30-nm-thick Al$_2$O$_3$ layer. The implantation activation was achieved by rapid thermal anneal (RTA) at 700–800 °C for 10 s in a nitrogen ambient. A 10 nm Al$_2$O$_3$ film was regrown by ALD after removing the encapsulation layer by buffer oxide etch solution and soaking in ammonia sulfide for 10 min for surface preparation. The source and drain Ohmic contacts were made by electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 400 °C for 30 s also in a N$_2$ ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.50 to 100 μm.

Figure 1(b) shows the dc $I_{ds}−V_{ds}$ characteristics with a gate bias from 0 to 4 V in steps of +0.5 V. The measured MOSFET has a mask designed gate length $L_{mask}$ of 0.50 μm and gate width of 100 μm. $L_{mask}$ is defined by source drain implantation mask. A maximum drain current of

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670 mA/mm is obtained at a gate bias of 4 V and a drain bias of 2 V. The device performance has a significant leap in drain current, compared to our previous results on In0.20Ga0.80As MOSFETs. The maximum drain current is also 80% higher than those recent results from In0.53Ga0.47As MOSFETs. The maximum drain current of 670 mA/mm is the highest value ever reported in enhancement-mode III-V MOSFETs, including “implant-free” E-mode III-V MOSFETs with maximum drain current of 243–443 mA/mm.15,16 Note that the device operation is fundamentally different between “implant-free” E-mode III-V MOSFETs and the conventional inversion-type E-mode III-V MOSFETs as demonstrated in this letter.

A maximum extrinsic transconductance $G_m$ is $\sim 230 \text{ mS/mm}$ for In0.65Ga0.35As compared with $G_m$ of $\sim 160 \text{ mS/mm}$ for In0.53Ga0.47As in Fig. 2(a). The extrinsic $G_m$ could be further improved by reducing equivalent oxide thickness and improving the quality of the interface. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics are calculated by subtracting the half of serial resistance $R_{SD}$. The resulting intrinsic maximum drain current and transconductance for 0.5 μm In0.65Ga0.35As MOSFET are 910 mA/mm and 280 mS/mm, respectively (not shown). By the conventional linear region extrapolation method or second derivative method, the intrinsic threshold voltage is determined around 0.40 V. The gate leakage current is very low, below $5 \times 10^{-6} \text{ A/cm}^2$ at 4 V gate bias, which is more than eight orders of magnitude smaller than the drain on current.

Figure 2(b) summarizes all measured drain current $I_{ds}$ versus $L_{mask}$ under $V_{gs}=4 \text{ V}$ and $V_{ds}=2 \text{ V}$ or $V_{ds}=0.05 \text{ V}$ for both In0.65Ga0.35As MOSFETs and In0.53Ga0.47As MOSFETs. The drain current or transconductance is linearly inversely proportional to $L_{mask}$ as expected and start to saturate at $L_{mask}=0.75 \mu m$. The maximum drain current has the potential to increase further by reducing gate length and/or implementing In richer InGaAs channels. Note that most of commercial GaAs technology, such as pseudomorphic high-electron-mobility transistor (pHEMT), has maximum drain current around 400 mA/mm at 0.25 μm gate length. For GaAs pHEMT, due to its high low-field mobility, the maximum drain current is mainly limited by the saturation velocity, modulation doping concentration and heterostructure itself. The maximum drain current saturates at 5–10 μm gate length and does not scale with gate length for short gate length devices. In contrast to GaAs pHEMT, the demonstrated surface channel InGaAs MOSFET, more or less like real Si MOSFET, has the gate length scalability down to submicron, as shown in Fig. 2(b). With further improved interface quality and improved heterostructure design, the maximum drain current could be way higher than the value that the doped GaAs pHEMT technology offers.

Figure 3 illustrates the basic idea to qualitatively explain why the device performance of In0.65Ga0.35As MOSFETs is better than that of In0.53Ga0.47As MOSFETs and much better than that of In0.20Ga0.80As MOSFETs. Presumably every interface has donor-type interface traps and acceptor-type interface traps. A convenient notation is to interpret the sum of
than In0.53Ga0.47As, and much less for In0.20Ga0.80As or Ga2O3 only less than 1 mA in situ MOSFETs.12–14 and Al2O3 dielectrics.20 It also explains why Al2O3, HfO2, HfAlO, and GaAs MOSFETs have similar device performance on the same III-V substrate. The statement here does not exclude the effect of the interface quality, which is mainly determined by dielectric materials, surface preparation, and oxide formation, on device performance. But the high-mobility channel or substrate itself plays the most important role here. The detailed model description could be found in Ref. 21.

A similar conclusion can also be reached by calculating the surface potential \( \psi_s \) or band bending condition for strong inversion on different substrates. The strong inversion requires \( \psi_s = (2kT/q)\ln(N_A/n_i) \), where \( N_A \) is channel doping concentration and \( n_i \) is intrinsic carrier concentration. With \( N_A \) of \( 1 \times 10^{15} \) cm\(^{-3} \), \( n_i \) (GaAs) of \( 2 \times 10^{16} \) cm\(^{-3} \), and \( n_i \) (InAs) of \( 1 \times 10^{15} \) cm\(^{-3} \), it is clear that it requires much less band bending or surface potential movement to realize strong inversion in In-rich InGaAs than in GaAs.

In summary, we have demonstrated unprecedented high device performance of inversion-type E-mode In0.65Ga0.35As MOSFETs using ALD Al2O3 gate dielectrics. These results suggest III-V channel or substrate itself is the main determinant for the device performance of III-V MOSFETs, though the interface quality is also important. The substrate engineering is a very important perspective, requiring more attention in future III-V MOSFET research.

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