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Substrate engineering for high-performance surface-channel III-V metal-oxide-semiconductor field-effect transistors

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High-performance inversion-type enhancement-mode n-channel $In_{0.65}Ga_{0.35}As$ metal-oxide-semiconductor field-effect transistors (MOSFETs) with atomic-layer-deposited Al_2O_3 as gate dielectric are demonstrated. A 0.5 μm gate-length MOSFET with an Al_2O_3 gate oxide thickness of 10 nm shows a gate leakage current less than 5×10^{-6} A/cm^2 at 4 V gate bias, a threshold voltage of 0.40 V, a maximum drain current of 670 mA/mm, and transconductance of 230 mS/mm at drain voltage of 2 V. More importantly, a model is proposed to ascribe this 80% improvement of device performance from $In_{0.53}Ga_{0.47}As$ MOSFETs mainly to lowering the energy level difference between the charge neutrality level and conduction band minimum for $In_{0.65}Ga_{0.35}As$. The right substrate or channel engineering is the main reason for the high performance of the devices besides the high-quality oxide-semiconductor interface. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2822892]

Silicon-based technology will encounter physical and technical limits within the next decade, which motivates the semiconductor industry to explore alternative device technologies such as Ge, III-Vs, and carbon nanotubes to replace silicon as active channel materials. In the past four decades, great efforts have been made to search for low-defect, thermodynamically stable insulators for III-V metal-oxide-semiconductor field-effect transistors (MOSFETs). Although some high-performance depletion-mode (D-mode) III-V MOSFETs have been demonstrated previously,[1–5] the reported inversion-type enhancement-mode (*E*-mode) III-V MOSFETs suffer from low drain currents.[6–10] There are only two exceptions in the literature. One is molecular beam epitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)/In_{0.53}Ga_{0.47}As$ MOSFET with maximum drain current of 360 mA/mm;[11] another one is atomic layer deposition (ALD) grown Al_2O_3, HfO_2, or $HfAlO/In_{0.53}Ga_{0.47}As$ MOSFETs with maximum drain current of 367−430 mA/mm.[12–14] A clear hint among the available experimental results is that III-V substrate itself could play a much more important role in device performance if certain quality of oxide/III-V interface is achieved.

In this letter, we report high-performance inversion-type *E*-mode $In_{0.65}Ga_{0.35}As$ MOSFETs using ALD Al_2O_3 as gate dielectric. The maximum drain current of 670 mA/mm and extrinsic transconductance of 230 mS/mm for a 0.5 μm gate-length MOSFET are achieved, which have about 80% improvement over previously reported inversion-type *E*-mode $In_{0.53}Ga_{0.47}As$ MOSFETs.[12–14] It is reasonable to believe that the interface quality of $Al_2O_3/In_{0.65}Ga_{0.35}As$ and $Al_2O_3/In_{0.53}Ga_{0.47}As$ is similar due to the similar surface chemistry during the pretreatment and ALD process. 12% In concentration difference should not change the interface quality dramatically. To explain this dramatic improvement

of device performance, a charge neutrality level (CNL) based model is proposed. It shows that III-V channel or substrate itself, which attracts less attention in the past, is the main determinant for III-V MOSFETs' maximum drain current and, thus, device performance.

Figure 1(a) shows the cross section schematic of the device structure of an ALD $Al_2O_3/In_{0.65}Ga_{0.35}As$ MOSFET. A 500 nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ transition layer, and a 20 nm p-doped 1×10^{17} cm^{-3} strained $In_{0.65}Ga_{0.35}As$ channel layer were sequentially grown by MBE on a 2 in. InP $p+$ substrate. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30-nm-thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer. For device fabrication, source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV through the 30-nm-thick Al_2O_3 layer. The implantation activation was achieved by rapid thermal anneal (RTA) at 700−800 °C for 10 s in a nitrogen ambient. A 10 nm Al_2O_3 film was regrown by ALD after removing the encapsulation layer by buffer oxide etch solution and soaking in ammonia sulfide for 10 min for surface preparation. The source and drain Ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA process at 400 °C for 30 s also in a N_2 ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.50 to 40 μm and a gate width of 100 μm.

Figure 1(b) shows the dc $I_{ds}-V_{ds}$ characteristics with a gate bias from 0 to 4 V in steps of +0.5 V. The measured MOSFET has a mask designed gate length L_{mask} of 0.50 μm and gate width of 100 μm. L_{mask} is defined by source drain implantation mask. A maximum drain current of

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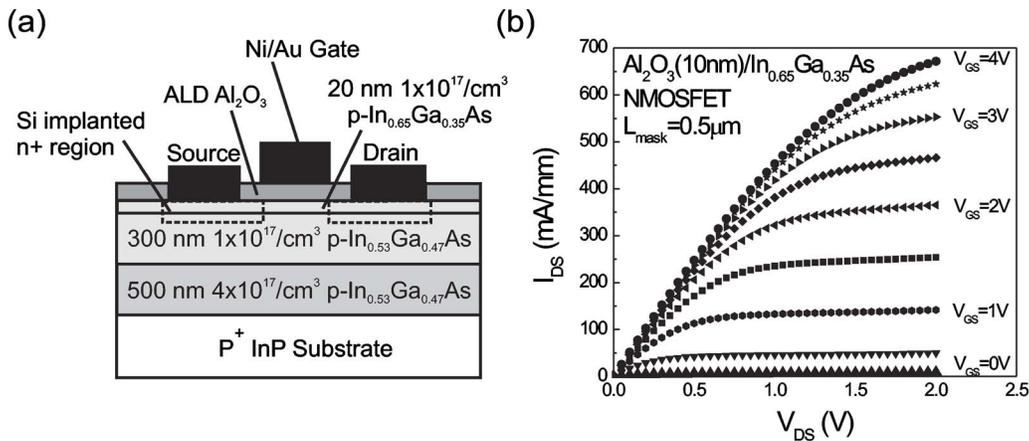[a]Author to whom correspondence should be addressed. Electronic mail: yep@purdue.edu

FIG. 1. (Color online) (a) A cross section of an inversion-type *E*-mode $Al_2O_3/In_{0.65}Ga_{0.35}As$ MOSFET (b) *I-V* characteristic of a 0.5 μm mask gate length $In_{0.65}Ga_{0.35}As$ MOSFET with a 10 nm ALD Al_2O_3 as a gate dielectric.

670 mA/mm is obtained at a gate bias of 4 V and a drain bias of 2 V. The device performance has a significant leap in drain current, compared to our previous results on $In_{0.20}Ga_{0.80}As$ MOSFETs.[8,9] The maximum drain current is also 80% higher than those recent results from $In_{0.53}Ga_{0.47}As$ MOSFETs.[12–14] The maximum drain current of 670 mA/mm is the *highest* value ever reported in enhancement-mode III-V MOSFETs, including "implant-free" *E*-mode III-V MOSFETs with maximum drain current of 243–443 mA/mm.[15,16] Note that the device operation is fundamentally different between "implant-free" *E*-mode III-V MOSFETs and the conventional inversion-type *E*-mode III-V MOSFETs as demonstrated in this letter.

A maximum extrinsic transconductance G_m is ~230 mS/mm for $In_{0.65}Ga_{0.35}As$ compared with G_m of ~160 mS/mm for $In_{0.53}Ga_{0.47}As$ in Fig. 2(a). The extrinsic G_m could be further improved by reducing equivalent oxide thickness and improving the quality of the interface. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics are calculated by substracting the half of serial resistance R_{SD}. The resulting intrinsic maximum drain current and transconductance for 0.5 μm $In_{0.65}Ga_{0.35}As$ MOSFET are 910 mA/mm and 280 mS/mm, respectively (not shown). By the conventional linear region extrapolation method or second derivative method, the extrinsic threshold voltage is determined around 0.40 V. The gate leakage current is very low, below 5×10^{-6} A/cm^2 at 4 V gate bias, which is more than eight orders of magnitude smaller than the drain on current.

Figure 2(b) summarizes all measured drain current I_{ds} versus L_{mask} under $V_{gs}=4$ V and $V_{ds}=2$ V or $V_{ds}=0.05$ V for both $In_{0.65}Ga_{0.35}As$ MOSFETs and $In_{0.53}Ga_{0.47}As$ MOSFETs. The drain current or transconductance is linearly inversely proportional to L_{mask} as expected and start to saturate at $L_{mask}=0.75$ μm. The maximum drain current has the potential to increase further by reducing gate length and/or implementing In richer InGaAs channels. Note that most of commercial GaAs technology, such as pseudomorphic high-electron-mobility transistor (pHEMT), has maximum drain current around 400 mA/mm at 0.25 μm gate length. For GaAs pHEMT, due to its high low-field mobility, the maximum drain current is mainly limited by the saturation velocity, modulation doping concentration and heterostructure itself. The maximum drain current saturates at 5–10 μm gate length and does not scale with gate length for short gate length devices. In contrast to GaAs pHEMT, the demonstrated surface channel InGaAs MOSFET, more or less like real Si MOSFET, has the gate length scalability down to submicron, as shown in Fig. 2(b). With further improved interface quality and improved heterostructure design, the maximum drain current could be way higher than the value that the doped GaAs pHEMT technology offers.

Figure 3 illustrates the basic idea to qualitatively explain why the device performance of $In_{0.65}Ga_{0.35}As$ MOSFETs is better than that of $In_{0.53}Ga_{0.47}As$ MOSFETs and much better than that of $In_{0.20}Ga_{0.80}As$ MOSFETs. Presumably every interface has donor-type interface traps and acceptor-type interface traps. A convenient notation is to interpret the sum of
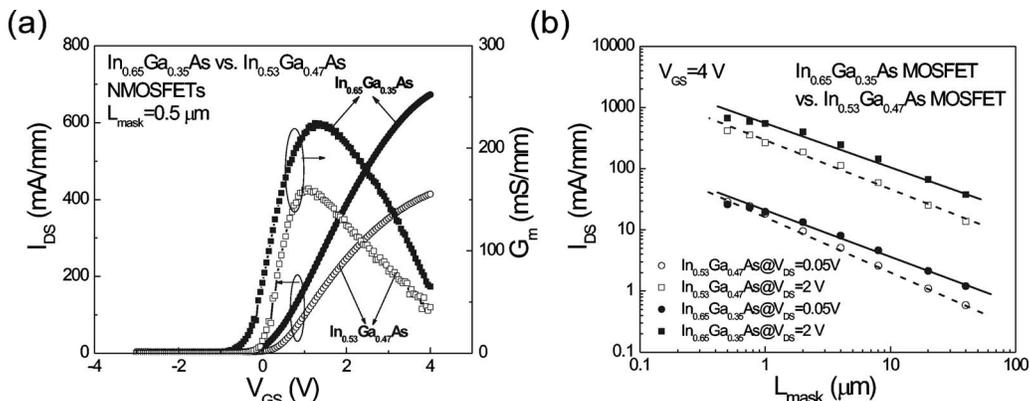

FIG. 2. (a) Extrinsic drain current and transconductance vs gate bias for 0.5 μm $In_{0.65}Ga_{0.35}As$ MOSFET and 0.5 μm $In_{0.53}Ga_{0.47}As$ MOSFET for comparison. (b) The drain current at $V_{gs}=5$ V and $V_{ds}=2$ V or $V_{ds}=0.05$ V vs $1/L_{mask}$. The solid and dashed lines are guides for the eyes.
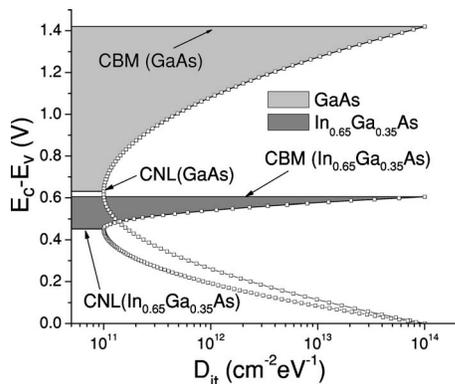
FIG. 3. Schematic for the parabolic D_{it} distribution within energy band of GaAs and $In_{0.65}Ga_{0.35}As$. The CNL is aligned 0.8 eV below CBM for GaAs and 0.15 eV below CBM for $In_{0.65}Ga_{0.35}As$. The shadow area shows the built-up negative charges in interface traps after Fermi-level moves from CNL to CBM. The model is extremely simplified to highlight the fundamental point by assuming D_{it} distribution is parabolic in logarithm scale and D_{it} value at CBM and valence band maximum is fixed at $10^{14}/cm^2$ eV.

these by an equivalent D_{it} distribution, with an energy level called charge neutrality level E_{CNL}. If Fermi level E_F is above E_{CNL}, the states are of acceptor type and negatively charged if the states are occupied. If Fermi level E_F is below E_{CNL}, the states are of donor type and positively charged if the states are occupied. Assuming that Fermi-level stabilization energy is located at E_{CNL} and the strong electron inversion occurs when Fermi-level reaches conduction band minimum (CBM), the amount of acceptor type interface traps from CNL to CBM should be less for $In_{0.65}Ga_{0.35}As$ than $In_{0.53}Ga_{0.47}As$, and much less for $In_{0.20}Ga_{0.80}As$ or GaAs, as illustrated in Fig. 3. The farther the E_{CNL} locates from CBM, the more negative trapped charges are built in when the Fermi-level sweeps to CBM, the more difficult it is to realize a large amount of inversion charges to participate the transport. The traps not only reduce the mobile inversion charges, but also prevent further surface potential bending due to the Coulomb repulsion. Assuming a linear extrapolation exhibits in $In_xGa_{1-x}As$ binary and ternary alloys[17] and CNL for InAs is at 0.2 eV above CBM,[18] CNL and CBM differences for GaAs, $In_{0.20}Ga_{0.80}As$, $In_{0.53}Ga_{0.47}As$, and $In_{0.65}Ga_{0.35}As$ are ~0.8, 0.6, 0.27, and 0.15 eV, respectively. It explains why $Al_2O_3/In_{0.20}Ga_{0.80}As$ MOSFET[8,9] has much less maximum drain current than $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFET[12–14] and $Al_2O_3/In_{0.65}Ga_{0.35}As$ MOSFET. It also explains why $Ga_2O_3(Gd_2O_3)/GaAs$ MOSFETs have only less than 1 mA/mm drain current[7] and $Ga_2O_3(Gd_2O_3)/In_{0.53}Ga_{0.47}As$ MOSFET has 360 mA/mm drain current.[11] Another interesting material to double check the availability of the above model is InP. InP has the bandgap of 1.35 eV, which is very similar to 1.42 eV of GaAs. However, CNL locates only ~0.5 eV below CBM.[19] It is much easier to realized inversion-mode InP MOSFET than GaAs MOSFET. The 100 mA/mm drain current InP MOSFETs have been demonstrated using ALD high-k dielectrics.[20] It also explains why Al_2O_3, HfO_2, HfAlO, and even *in situ* grown $Ga_2O_3(Gd_2O_3)$ have the similar device performance on the same III-V substrate. The statement here does not exclude the effect of the interface quality, which is mainly determined by dielectric materials, surface preparation, and oxide formation, on device performance. But the high-mobility channel or substrate itself plays the most im-

portant role here. The detailed model description could be found in Ref. 21.

A similar conclusion can also be reached by calculating the surface potential ψ_s or band bending condition for strong inversion on different substrates. The strong inversion requires $\psi_s \approx (2kT/q)\ln(N_A/n_i)$, where N_A is channel doping concentration and n_i is intrinsic carrier concentration. With N_A of 1×10^{17} cm³, n_i (GaAs) of 2×10^6 cm³, and n_i (InAs) of 1×10^{15} cm³, it is clear that it requires much less band bending or surface potential movement to realize strong inversion in In-rich InGaAs than in GaAs.

In summary, we have demonstrated unprecedented high device performance of inversion-type E-mode $In_{0.65}Ga_{0.35}As$ MOSFETs using ALD Al_2O_3 gate dielectrics. These results suggest III-V channel or substrate itself is the main determinant for the device performance of III-V MOSFETs, though the interface quality is also important. The substrate engineering is a very important perspective, requiring more attention in future III-V MOSFET research.

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