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# Simplified Surface Preparation for GaAs Passivation Using Atomic Layer-Deposited High-$\kappa$ Dielectrics

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***Abstract*—Atomic layer deposition (ALD) provides a unique opportunity to integrate high-quality gate dielectrics on III–V compound semiconductors. The physics and chemistry of a III–V compound semiconductor surface or interface are problems so complex that even after three decades research understanding is still limited. We report a simplified surface preparation process using ammonium hydroxide ($NH_4OH$) to remove the native oxide and make the hydroxylated GaAs surface ready for ALD surface chemistry. The effectiveness of GaAs passivation with ALD $Al_2O_3$ is demonstrated with small hysteresis, 1%–2% frequency dispersion per decade at accumulation capacitance, and a mid-bandgap $D_{it}$ of $8 \times 10^{11}$ to $1 \times 10^{12}$ $cm^{-2} \cdot eV^{-1}$ determined by the Terman method. The results from ammonium sulfide $[(NH_4)_2S]$-, hydrofluoric acid (HF)-, and hydrochloric acid (HCl)-treated surfaces and a surface with native oxide are also presented to compare with the results from the ammonium-hydroxide-treated surface. Fermi-level unpinning is also easily demonstrated on the ALD $HfO_2$ and p-type GaAs interface.**

***Index Terms*—Aluminum oxide, ammonium hydroxide, atomic layer deposition (ALD), Fermi-level pinning, Fermi-level unpinning, gallium arsenide, hafnium oxide, MOS structures.**

## I. Introduction

GaAs MOSFETs have been a subject of study for several decades. The renewed research thrust is for advanced ultra-large-scale-integration digital applications or ultimate CMOS technology beyond the 22-nm node by using III–V compound semiconductors as conduction channels to replace traditional Si or strained Si, integrating novel dielectrics with these high-mobility materials, and heterogeneously incorporating them on Si or silicon-on-insulator (SOI). The lack of high-quality thermodynamically stable gate dielectric insulators on GaAs or III–V that can match device criteria similar to $SiO_2$ on Si, remains the main obstacle to realizing a GaAs MOSFET technology with commercial value. In the past decades, both GaAs native oxides and deposited insulating layers have been attempted as gate dielectrics. The literature testifies to the extent of this effort [1], [2], with currently active approaches, including sulfur passivation [3], silicon interface control layers (Si ICLs) [4]–[6], *in situ* molecular-beam-epitaxy growth of $Ga_2O_3(Gd_2O_3)$ [7]–[9], *ex situ* atomic layer deposition (ALD) growth of $Al_2O_3$ and $HfO_2$ [10]–[12], wet oxidation of InAlP [13], jet vapor deposition of $Si_3N_4$ [14], ALD or PVD of $HfO_2 + Si$ ICL [15]–[17], PVD of $HfO_2 + Ge$ ICL [18], ALD of $HfO_2 + AlON$ ICL [19], and self-assembly organic nanodielectrics [20]. Among them, ALD is the most promising approach to depositing high-$\kappa$ dielectrics (i.e., HfSiON). Given the Si industry's familiarity with ALD for front-end processes, the transition to ALD III–V MOSFETs integrated on the Si CMOS platform would be easier.

In this paper, we report the details of a simplified surface preparation process using ammonium hydroxide ($NH_4OH$) to remove the native oxide and leave a hydroxylated GaAs surface that is ready for the first ALD surface chemistry reaction with trimethyl aluminum. This simple wet chemical process avoids the complexity and process dependence that exists in other reported methods that require ultrahigh-vacuum well-controlled hydrogen/nitrogen plasma, deadsorption of capping layers, or the control of interfacial layers. The effectiveness of GaAs passivation with ALD $Al_2O_3$ on a ($NH_4OH$)-treated surface is demonstrated with small hysteresis, 1%–2% frequency dispersion per decade at accumulation capacitance, and mid-bandgap $D_{it}$ of $8 \times 10^{11}$ to $1 \times 10^{12}$ $cm^{-2} \cdot eV^{-1}$ determined by the Terman method. Results from surfaces treated in ammonium sulfide $[(NH_4)_2S]$, hydrofluoric acid (HF), or hydrochloric acid (HCl), are also presented along with a native oxide surface to compare with the results from the ammonium-hydroxide-treated surface. The results of ALD $HfO_2$ on p-type GaAs, grown by hafnium chloride ALD process, are also briefly presented. The purpose of this paper is to report the most simple process for achieving an unpinned GaAs Fermi-level using ALD.

## II. Device Fabrication

The starting material is 2-in p-type or $n^+$-type GaAs substrates with (001) crystal orientation purchased from AXT, Inc. Before surface treatment, all wafers underwent a standard degrease process using acetone, methanol, and isopropanol. The ($NH_4OH$) treatment is carried out by soaking the samples in ($NH_4OH$) (29%) solution for 3 min to remove native oxide and rinsing in flowing deionized (DI) water followed by gently drying the surface using an $N_2$ blowgun. The ($NH_4OH$) etching step removes arsenic and gallium oxides from the surface and the surface becomes covered by elemental arsenic and a tiny amount of gallium suboxide [21]. The subsequent ALD process results in the disappearance of elemental arsenic and a self-cleaning of the GaAs surface [12], [22]. The $(NH_4)_2S$ treatment is done by dipping the sample in a $HCl:H_2O = 1:1$ solution for 1 min to remove the native oxide, rinse in flowing DI water, soaking the sample in $(NH_4)_2S$ for 10 min at room

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temperature and drying using an $N_2$ gun. The HF treatment is done by dipping the sample in diluted 1% HF solution for 1 min, cleaning with DI water and an $N_2$ dry. The HCl treatment is performed by dipping the sample in a $HCl:H_2O = 1:1$ solution for 1 min, followed by a DI water clean and an $N_2$ dry. Some samples that only underwent a degrease cleaning, which are expected to have 1–2-nm native oxide of GaAs, are used as reference.

After the above surface pretreatments, the samples were immediately loaded into an ASM F-120 ALD system. It took about 1 h to ramp up to the growth temperature of 300 °C from room temperature at a base pressure of 2–3 torr in $N_2$. ALD $Al_2O_3$ films of 5 and 10 nm were deposited by using alternating pulses of trimethyl aluminum (TMA) and water $(H_2O)$ precursors. The optimized pulselength and $N_2$ purge time for GaAs were 0.8 and 1.0 s, respectively, for TMA, and 1.0 and 1.0 s, respectively, for $H_2O$. For $HfO_2$ ALD growth, hafnium chloride $(HfCl_4)$ and $H_2O$ were used as the Hf source and oxidant, respectively. The optimized pulselength and $N_2$ purge time for GaAs were 1.4 and 2.0 s, respectively, for $(HfCl_4)$, and 1.0 and 2.0 s, respectively, for $H_2O$. Films of 10 and 20-nm $HfO_2$ were grown on native oxide and $(NH_4OH)$-treated GaAs substrates at 300 °C. The samples underwent postdielectric deposition annealing (PDA) for 10–30 s at 600 °C–800 °C by rapid thermal annealing (RTA) in an $N_2$ ambient. A 200-nm-thick Ti/Au layer was electron-beam deposited and lithographically defined to form $100 \times 100$ $\mu$m MOS capacitors. Electrical contact to the GaAs substrates in this paper was made via an electron-beam evaporated Ti/Au backgate. Au is widely used for GaAs technology although it is not a Si CMOS compatible material. Other metals such as Ag(0.95)In(0.05)/Ge and Al could be used to replace Au as ohmic contact and gate metals. An HP4284 LCR meter was used for the capacitance measurement as shown in the inset of Fig. 1. We focus on the results from p-type GaAs substrates since they are directly related with our research interest—the inversion-type n-channel GaAs MOSFET. The results obtained from n-type GaAs substrates are quantitatively different from p-type GaAs due to the different surface electrochemical properties. A more systematic investigation is ongoing.

## III. Results and Discussions

The $C$–$V$ measurements are widely used to quantitatively study a MOS structure. There are three quantities that are the most important factors to evaluate the quality of high-$\kappa$ dielectrics on novel channel materials. The first is the amount of hysteresis that results when the MOS capacitor is biased well into accumulation and inversion. The second is the percentage of frequency dispersion at the accumulation capacitance. The third is the frequency dependent flatband shifts observed mostly after high-temperature annealing. All of these factors are related with the interface trap density $D_{\rm it}$. The high-frequency (1 kHz–1 MHz) $C$–$V$ loops for a capacitor with 5-nm ALD $Al_2O_3$ film on p-type GaAs are shown in Fig. 1. This capacitor was $(NH_4OH)$ pretreated and annealed with an RTA step of 700 °C for 30 s in an nitrogen ambient. The doping concentration is $\sim 5 \times 10^{17}/\text{cm}^3$ for this device determined by the slope

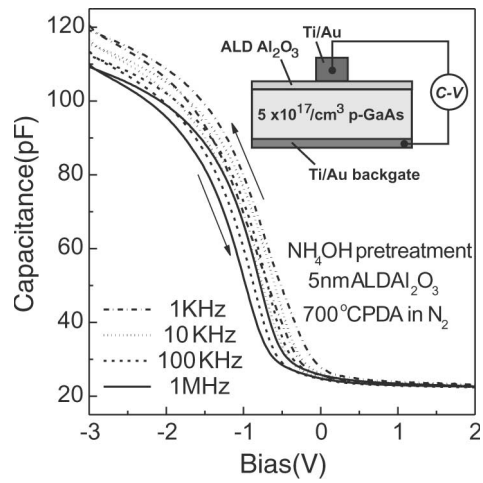


Fig. 1. High-frequency (1 kHz–1 MHz) $C$–$V$ loops for a MOS capacitor with 5-nm ALD $Al_2O_3$ film on p-type GaAs substrate. The GaAs surface was $NH_4OH$ pretreated and PDA was done at 700 °C for 30 s in nitrogen ambient. Inset: The schematic picture of an $Al_2O_3$/p-GaAs MOS capacitor under $C$–$V$ measurement with Ti/Au as both top-gate and back-gate. The capacitor size is $100 \times 100$ $\mu$m.

of the $1/C^2$ versus bias plot. The hysteresis at the flatband condition is $\sim$150 mV, which is larger than our previous reported results of 10–80 mV hysteresis [23] for a 30-nm-thick oxide film which was deposited on a metal–organic chemical-vapor-deposition epitaxial InGaAs surface grown by a more advanced ALD reactor (ASM Pulsar 2000). The frequency dispersion at accumulation capacitance is about 2% per decade on the 5-nm $Al_2O_3$ samples, which is further improved to $\sim$1% per decade on the 10-nm $Al_2O_3$ samples. The frequency dependent flatband shift is negligible with the PDA process up to 700 °C and becomes significant only with PDA of 800 °C and above. The mid-bandgap $D_{\rm it}$ is estimated be between $8 \times 10^{11}$ and $1 \times 10^{12}$ $\text{cm}^{-2} \cdot \text{eV}^{-1}$ determined by the Terman method. Note that the $C$–$V$ data presented in this paper is not necessarily going to be the best that can be achieved.

The frequency response of a MOS capacitor in the inversion region depends on the inversion-charge generation time. The minority response time for thermal generation/recombination of GaAs is $> 400$ s [8], therefore the minority carries cannot keep up with the low-frequency $C$–$V$ measurement even at frequencies as low as 1 Hz. Additionally, no inversion is obtained at frequencies as low as 100 Hz on $Al_2O_3/\text{GaAs}$ MOS capacitors. However, at higher temperatures or under photo (light) illumination, more carriers are generated and their response time is significantly reduced so that the minority-carrier contribution to the capacitance can be profound. Although full inversion could be observed at the $Al_2O_3/In_{0.2}Ga_{0.8}As$ interface with increasing light intensity [24], in the case of $Al_2O_3/\text{GaAs}$ in Fig. 2, the inversion layer is difficult to form even when illuminated by the same intensity $(0 \sim 0.45\ \text{W}/\text{cm}^2)$ of light used for $In_{0.2}Ga_{0.8}As$. The difference in surface recombination velocity of $Al_2O_3/\text{InGaAs}$ and $Al_2O_3/\text{GaAs}$, which is related with interface trap density, is not the sole explanation for the above phenomena. The minority carrier concentration and its response time for thermal generation/recombination could play more important roles on inversion than the interface trap

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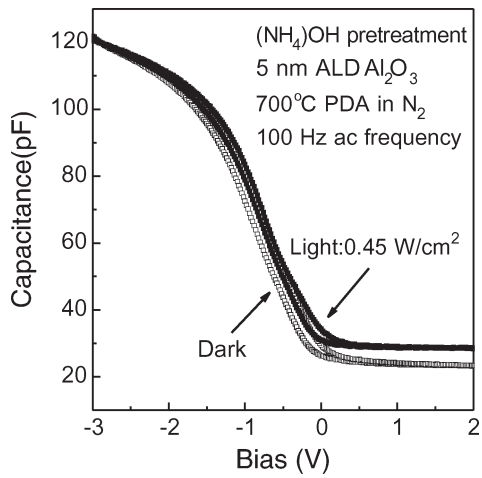


Fig. 2. Five hundred hertz $C$–$V$ loops for a MOS capacitor with 5-nm ALD $Al_2O_3$ film on p-type GaAs substrate measured in dark and with illumination. The inversion layer is difficult to form in GaAs even the device is illuminated with the light intensity of 0.45 W / cm$^2$, in contract to the results from $In_{0.2}Ga_{0.8}As$ reported in [24].

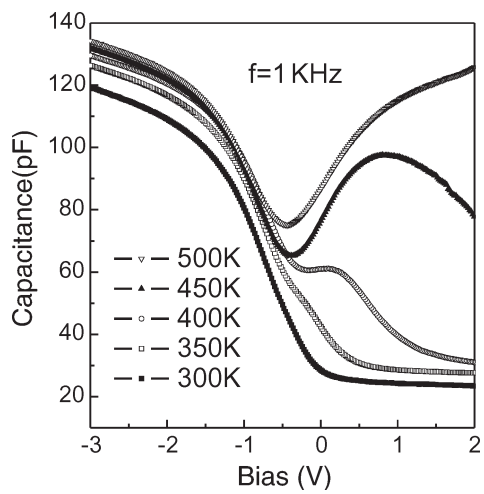


Fig. 3. Capacitance measurement at 1 kHz as a function of bias with different ambient temperatures. Inversion can be clearly seen at elevated temperatures (above 400 K).

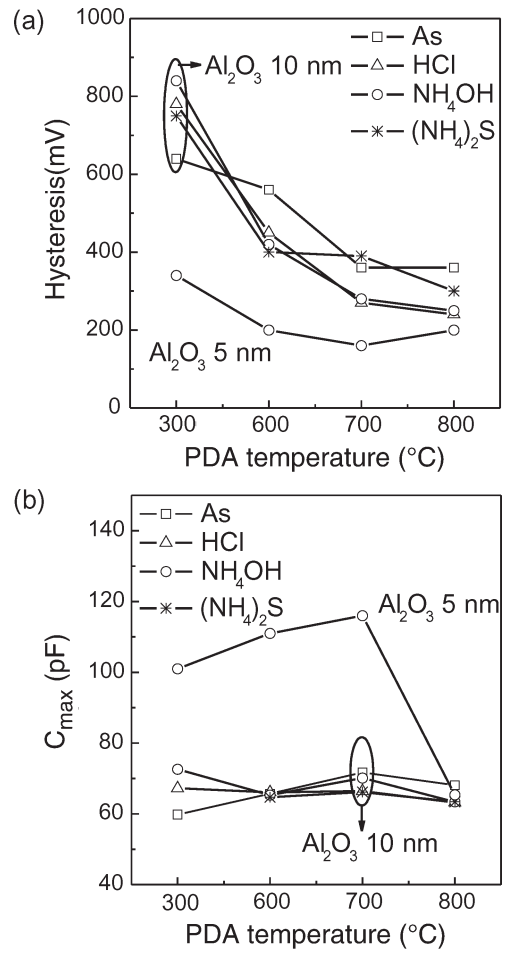


Fig. 4. (a) Hysteresis at flatband condition obtained from $C$–$V$ loops versus PDA temperature on different film thickness and surface treatment. Significant reduction of $C$–$V$ hysteresis verifies the importance of PDA process between 700 °C–800 °C in $N_2$ ambient. (b) The measured maximum capacitance value at accumulation versus PDA temperature on different film thickness and surface treatment.

density. $In_{0.2}Ga_{0.8}As$ has a much higher minority concentration than GaAs due to its lower band gap.

Temperature dependent $C$–$V$ measurements with a wide range of small ac signal frequencies are also widely used to study the minority-carrier recombination kinetics. The $C$–$V$ measurements at 100 Hz–1 MHz and at elevated temperatures from 300–500 K are systematically studied. Fig. 3 shows the results measured at 1 kHz as a function of bias at different temperatures. The major effect of temperature occurs during depletion-inversion at positive biases. At room temperature (300 K), minority carriers do not follow the 1-kHz signal for GaAs, thus a high-frequency curve is measured as shown in Figs. 1 and 3. However, as temperature is increased from 300 to 500 K, minority carriers begin to follow because generation and recombination rates increase with temperature, and the transition is made from a high-frequency curve to a low-frequency curve. By systematically varying both the temperature and the frequency, the temperature dependence of the transition frequency can be determined. The activation energy $(E_A)$ of minority-carrier generation and recombination for $Al_2O_3$/GaAs MOS structures is $\sim 0.71 \pm 0.05$ eV, which is just about half the bandgap energy of GaAs. This activation energy is that of intrinsic electrons in GaAs. Therefore, the dominant mechanism for minority carrier response must be generation and recombination through semiconductor bulk traps or interface traps in the measured MOS structures over the temperature range 300–500 K. The significant change from high-frequency $C$–$V$ for 300 K to low-frequency $C$–$V$ for 500 K is due to the dramatic increase of minority carrier concentration in the bulk GaAs through thermal generation as opposed to improved interface properties at high temperatures. This is why the inversion features at quasi-static $C$–$V$ or low-frequency $C$–$V$ should not be used as conclusive evidence to characterize the MOS interface, because it could be more related to the minority carriers in semiconductors instead of $D_{\rm it}$.

Fig. 4(a) shows hysteresis at the flatband condition obtained from $C$–$V$ loops versus PDA temperature on samples with different film thicknesses and surface treatments. The hysteresis is significantly reduced from 850 to 220 mV for the 10-nm $Al_2O_3$ film ($NH_4OH$ treatment) and from 340 to 150 mV

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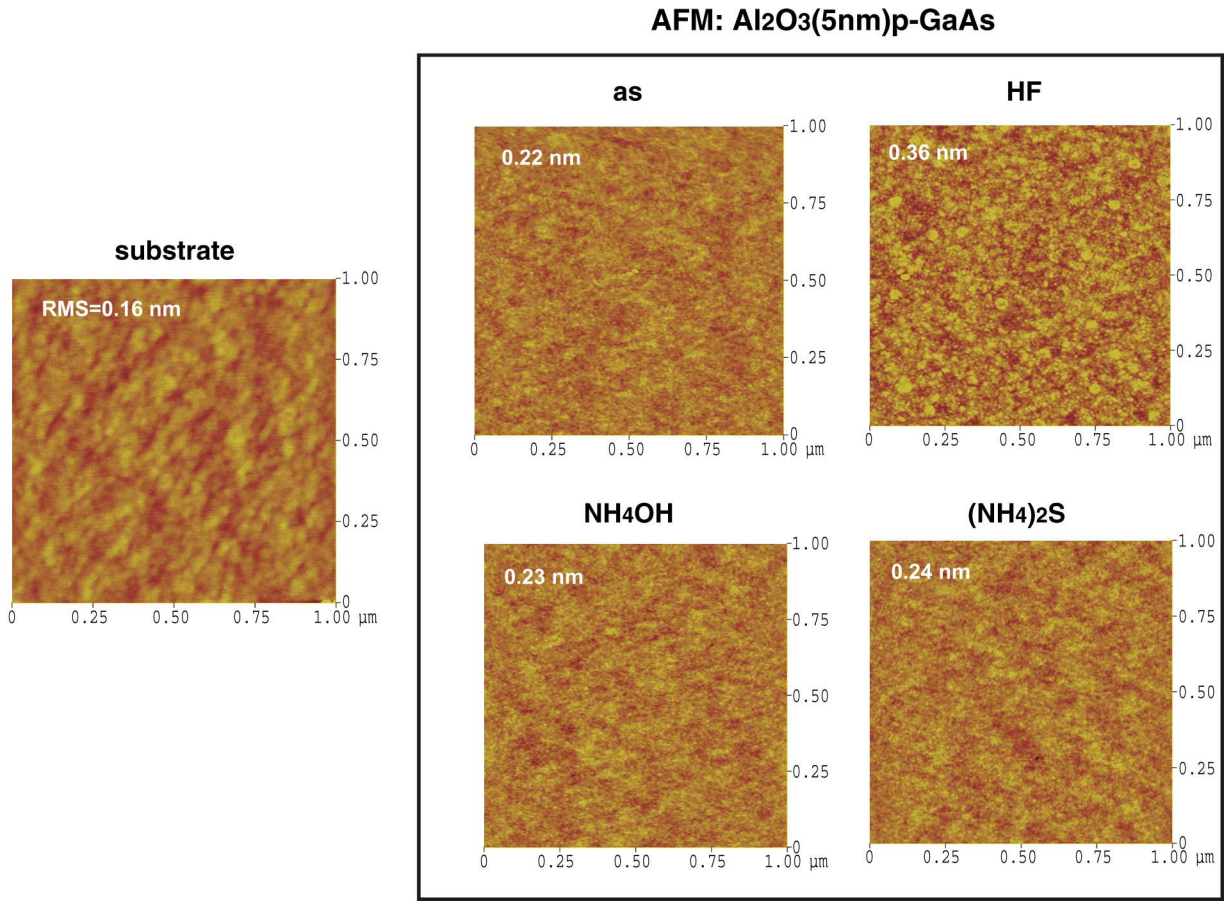


Fig. 5. AFM images on surface morphology of the GaAs substrate and 5-nm ALD $Al_2O_3$ films with four different surface pretreatments. The area of each single AFM image is $1 \times 1$ $\mu$m.

for the 5-nm $Al_2O_3$ film ($NH_4OH$ treatment), illustrating the importance of the PDA process between 700 °C–800 °C in $N_2$ ambient. A similar trend is also observed on other films with different surface treatments. Fig. 4(b) summarizes the measured maximum capacitance at accumulation versus PDA temperature on samples with different film thicknesses and surface treatments. In general, higher PDA temperatures result in a weak increase in accumulation capacitance, which is clearly demonstrated on the 5-nm $NH_4OH$ curve from 300 °C as grown versus PDA 700 °C. The sudden drop of capacitance after PDA 800 °C is probably due to the chemical reaction between $Al_2O_3$ and GaAs in $N_2$ to creating a significantly thick interfacial layer. In other words, 5-nm-thick $Al_2O_3$ is too thin as an encapsulation layer for GaAs to be annealed at as high as 800 °C. This result is consistent with our previous results on the fabrication of inversion-mode GaAs MOSFETs using $Al_2O_3$ as an encapsulation layer for Si dopant activation in GaAs between 750 °C–850 °C [23]. Fig. 4(b) also verifies that 10 nm of $Al_2O_3$ is safe on GaAs with PDA up to 800 °C. The reason for incomplete data on 5-nm $Al_2O_3$ with different surface treatments is described below.

For $H_2O$-based ALD processes, the OH functional groups or oxide layer on the surface is necessary for high-quality film growth. It is widely reported that ALD oxide (such as $HfO_2$ or $Al_2O_3$) grown on OH-terminated (hydrophilic) or oxide surfaces needs no incubation time and achieves smooth lateral 2-D growth, but in hydrogen-terminated (H-terminated; hydrophobic) surfaces, the termination leads to retardation nucleation, as well as a rough 3-D growth surface, which results in high leakage current [25], [26]. To investigate the ALD $Al_2O_3$ growth on GaAs surfaces with different pretreatment, we employed atomic force microscopy (AFM) to study the surface morphology. Fig. 5 shows AFM images of a bare GaAs substrate and 5-nm ALD $Al_2O_3$ grown on surfaces with different pretreatment. As shown in Fig. 5, the $(NH_4OH)$-treated surface exhibits a low RMS roughness of 0.23 nm. The As (native oxide)- and $(NH_4)_2S$-treated surfaces also reveal low RMS roughness between 0.22–0.24 nm. However, the HF-treated surface shows the largest RMS roughness of 0.36 nm with many 30–50-nm-sized islands on the film surface indicating 3-D growth. It has been reported that acid-treated (HCl or HF) surfaces are hydrophobic, while alkaline (KOH- or $(NH_4OH)$)-treated surfaces are hydrophilic [27], [28]. The hydrophilicity can be attributed to the OH groups on the GaAs surface while the hydrophobic surface may be due to a lack of the functional groups such as OH or oxide. For ALD dielectrics on GaAs, it is necessary to avoid the hydrophobic surface by pretreating in HF or HCl acid before the ALD process.

The leakage current measurements show significant differences between samples with different surface treatments, particularly the 5-nm thin film. We measured the dependence of the leakage current density ($J_L$) on the applied potential

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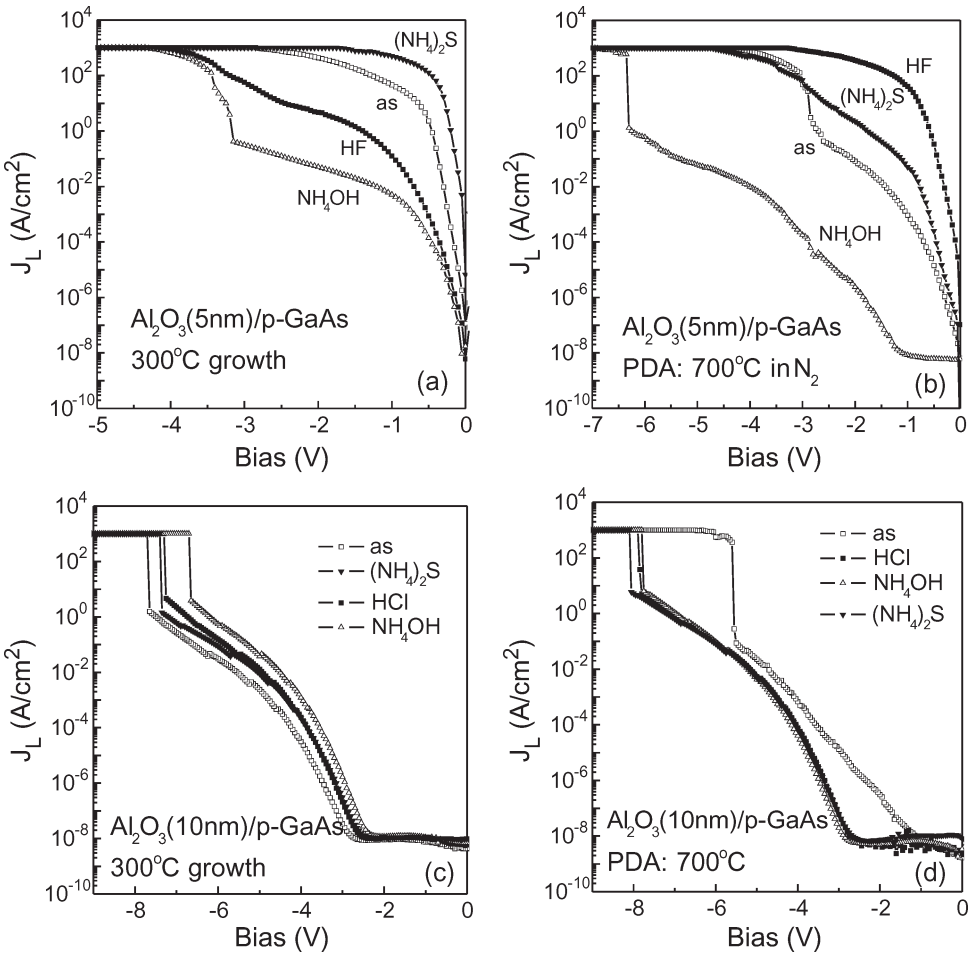


Fig. 6. Leakage current density $J_L$ versus gate bias on, (a) 5-nm as-grown ALD $Al_2O_3$, (b) 5-nm ALD $Al_2O_3$ with 700 °C PDA, (c) 10 nm as-grown ALD $Al_2O_3$, (d) 10-nm ALD $Al_2O_3$ with 700 °C PDA. The $NH_4OH$-treated sample shows the best performance on leakage current and breakdown voltage on 5-nm ALD $Al_2O_3$.

on the capacitor for the 5-nm ALD $Al_2O_3$ samples with four different surface treatments as shown in Fig. 6(a) without PDA and in Fig. 6(b) after 700 °C PDA. The negative bias means that the metal electrode is negative with respective to the p-type GaAs. The plot shows that the $(NH_4OH)$-treated sample has the best electrical characteristics and is further improved after the PDA process due to the improvement of bulk oxide quality and the possible increase of interfacial layer. The rest of the inappropriately treated samples show large leakage current densities for 5-nm oxide films, which leads to unreliable $C$–$V$ measurements. The leakage current density is significantly improved for 10-nm films on all samples with and without PDA as shown in Fig. 6(c) and (d), respectively. The degreased sample (as grown) has a lower breakdown voltage than its peers, which we ascribe to the existence of native oxide at the interface where unfavorable interdiffusions or chemical reactions may occur during the 700 °C PDA. The low current density for 10-nm films allows us to measure the reliable $C$–$V$ characteristics presented in Fig. 4. The conclusion is that the well-prepared hydroxylated GaAs surface is extremely critical to growing dense ultrathin ALD films at a few nanometer thicknesses. This is an important observation since ultrathin high-$\kappa$ dielectrics with the equivalent oxide thickness (EOT) of $\sim$1 nm is of interest for the future 22-nm technology node and beyond.

We have implemented the same methodology to study ALD $HfO_2$ films on as- (native oxide) and $(NH_4OH)$ pretreated GaAs substrates. Fig. 7 summarizes the leakage current density of 10- and 20-nm $HfO_2$ on p-type GaAs at room temperature. From Fig. 7(a), we found the breakdown voltage (considering the effect of a $-1.2$-V flatband shift) of as-grown 10-nm $HfO_2$ on the $(NH_4OH)$ surface to be 5.1 MV/cm, which is slightly larger than the as-surface (native oxide) at 4.6 MV/cm. However, for the as-grown 20-nm $HfO_2$ on as-surface GaAs shown in Fig. 7(b), the breakdown voltage is 3.8 MV/cm, which is lower than that of the as-grown 10-nm $HfO_2$ because the as-grown thicker film is crystallizes easier at the 300 °C ALD growth temperature [29]. The breakdown voltage of the as-grown $HfO_2$ is drastically reduced to 2.4 $\sim$ 2.8 MV/cm after PDA at 600 °C in $N_2$ due to full crystallization.

Fig. 8 briefly shows the $C$–$V$ characteristics of the $NH_4OH$-treated sample with 20-nm $HfO_2$ at various ac frequencies. The sample underwent a 600 °C PDA process in $N_2$ for 30 s. Frequency dispersion is small ($\sim$2% per decade) between 1 kHz and 1 MHz. The hysteresis is $\sim$0.8 V for the 20-nm film near the flatband voltage. The estimated dielectric permittivity of $HfO_2$ by accumulation capacitance at 100 Hz is $\sim$17.2, slightly lower than the reported 20–23. Some frequency dependent flatband shifts are seen due to the 600 °C PDA process. The

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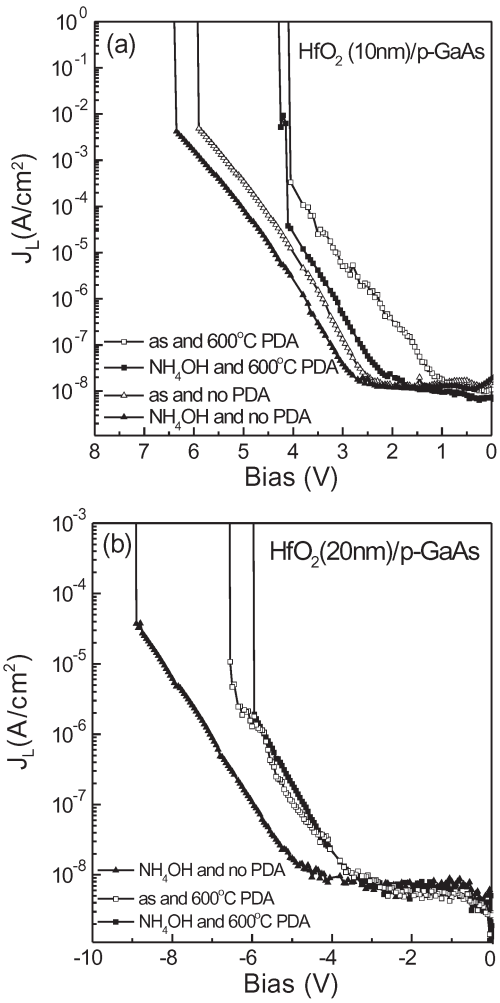


Fig. 7. Leakage current density $J_L$ versus gate bias on (a) 10-nm ALD $HfO_2$ (b) 20-nm ALD $HfO_2$ with different surface treatment and PDA conditions.

mid-bandgap $D_{\rm it}$ is estimated to be $\sim 1-2\times 10^{12}$ $\rm cm^{-2}\cdot eV^{-1}$ by the Terman method. The obvious Fermi-level pinning of PVD $HfO_2$ directly on n-type GaAs in Fig. 1 of [15] is not observed here. We ascribe it to the difference of oxide formation (ALD versus PVD) and dopant type of the GaAs substrates (p-type versus n-type) [30]. The built-up charges at the interface by plasma-enhanced or other fast deposition methods could be the major reason for the widely observed Fermi-level pinning in GaAs. The thermal grown $SiO_2$ on Si does not have built-up charges at the interface, due to the nature of native oxides, which is proved to be the best available dielectric on semiconductor. With appropriate material choice, ALD, as an extremely slow and gentle process based on surface chemical reactions, has the potential to provide high-quality, thermodynamically stable insulators on GaAs or III–V semiconductors. Much more work is needed to achieve GaAs MOS structures with the mid-bandgap $D_{\rm it}\sim 10^{10}$ $\rm cm^{-2}\cdot eV^{-1}$ or device criteria that are similar to $SiO_2$ on Si.

## IV. Conclusion

In conclusion, we have systematically studied $C$–$V$ characteristics of ALD $Al_2O_3$/GaAs and $HfO_2$/GaAs MOS capacitors with different surface preparations and PDA processing. Using $NH_4OH$ pretreatment, approximately 100-mV level hysteresis in $C$–$V$ loops and less than 2% per decade frequency dispersion at accumulation capacitance were demonstrated without any significant flatband shifts in $Al_2O_3$/p-GaAs. The ($NH_4OH$)-treated hydroxylated (-OH terminated or partially terminated) GaAs surface is extremely important for dense ultrathin ALD film growth at a few nanometer thickness ($<$ 5 nm) for subnanometer EOT in the 22-nm technology node. This paper provides conclusive experimental evidence that ALD oxides can unpin the Fermi level in GaAs or III–V in general with appropriate surface preparation and material choice. This conclusion is further confirmed by newly fabricated inversion-mode devices, showing maximum drain current of 430 mA/mm in InGaAs MOSFETs and 80 mA/mm in InP MOSFETs using ALD $Al_2O_3$ as gate dielectrics.

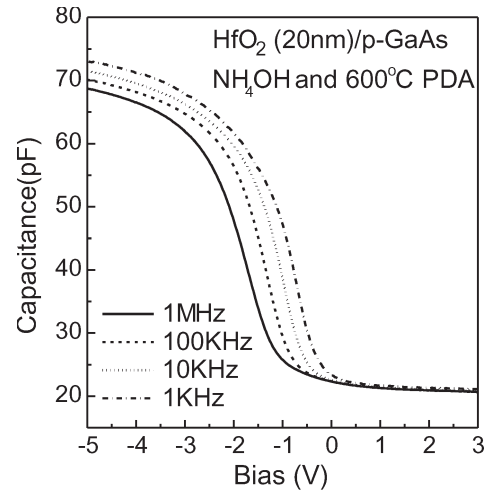


Fig. 8. Measured multiple frequency $C$–$V$ curves for a 20-nm ALD $HfO_2$/p-type GaAs MOS capacitor with $NH_4OH$ pretreated surface and 600 °C PDA.

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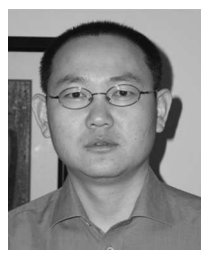

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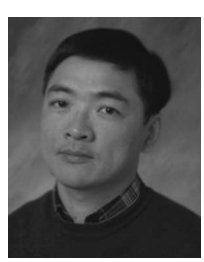

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