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Y Sui Purdue University

X Wang Purdue University

James A. Cooper
Birck Nanotechnology Center, Purdue University, james.a.cooper.1@purdue.edu

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High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC

Y. Sui, Student Member, IEEE, X. Wang, and J. A. Cooper, Fellow, IEEE

Abstract—SiC power MOSFETs designed for blocking voltages of 10 kV and higher face the problem of high drift layer resistance that gives rise to a high internal power dissipation in the ON-state. For this reason, the ON-state current density must be severely restricted to keep the power dissipation below the package limit. We have designed, optimized, and fabricated high-voltage SiC p-channel doubly-implanted metal—oxide—semiconductor insulated gate bipolar transistors (IGBTs) on 20-kV blocking layers for use as the next generation of power switches. These IGBTs exhibit significant conductivity modulation in the drift layer, which reduces the ON-state resistance. Assuming a 300 W/cm² power package limit, the maximum currents of the experimental IGBTs are $1.2\times$ and $2.1\times$ higher than the theoretical maximum current of a 20-kV MOSFET at room temperature and 177 °C, respectively.

Index Terms—High temperature, high voltage, insulated gate bipolar transistors (IGBTs), power transistors, silicon carbide, wide bandgap.

I. INTRODUCTION

N THE PAST decade, extensive research has been focused on 4H-SiC power MOSFETs for blocking voltages up to 10 kV. Both 10-kV doubly-implanted MOSFETs (DMOSFETs) and trench-gate MOSFETs (UMOSFETs) with low ONresistance have been reported [1], [2]. However, the demand for higher blocking voltage does not stop at 10 kV. Theoretically, the specific ON-resistance of the drift region in unipolar power devices is proportional to the square of the blocking voltage [3]. Therefore, the maximum ON-current for highvoltage MOSFETs must be severely restricted to keep the device power dissipation below the package power dissipation limit. Researchers have considered various device options for applications over 10 kV [4], including n-channel insulated gate bipolar transistors (IGBTs), p-channel IGBTs, and thyristors. The n-IBGT requires a p-type substrate, but p⁺ substrates in 4H-SiC have high resistivity due to the low free hole concentration and low hole mobility. Thus, viable n-IGBTs must have their substrates removed and replaced with a thin p⁺ epilayer or implanted layer, which complicates the processing. Even with the substrate removed, the performance of n-IGBTs is only marginally better than that of p-IGBT [4]; thus, we chose to pursue the p-IGBT in this letter. P-channel IGBTs have been

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The authors are with School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: cooperj@purdue.edu).

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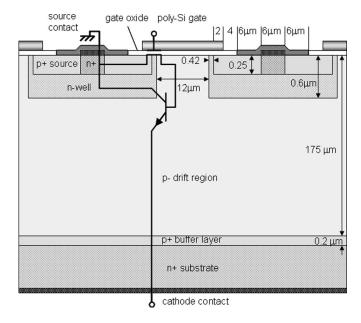


Fig. 1. Schematic cross section of the 4H-SiC p-channel DMOS-IGBT. All dimensions are in micrometers. The ambipolar lifetime for the p- drift layer in the experimental device is 458 ns on average. The equivalent circuit of the device is an n-p-n BJT with the base driven by a p-channel MOSFET. During ON-state operation, the source is grounded, the gate is biased negatively beyond threshold, and the cathode is biased negatively.

reported in SiC by others [5]–[7], but to our knowledge, this is the first report of IGBTs designed for blocking voltages of 20 kV.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1 shows a schematic cross section of the experimental device. A 0.2- μ m, 1×10^{18} cm⁻³ p⁺ buffer layer is grown on a silicon-face n⁺ 4H-SiC substrate, cut 8° off axis, followed by a 175- μ m, 2×10^{14} cm⁻³ p-type epilayer. In the experimental wafers, this epilayer has an average ambipolar lifetime of 458 ns, as measured by time-resolved photoluminescence decay. The material is provided by Cree, Inc.

A uniform layer of polysilicon (1.5 μ m thick) is deposited on the wafer by low-pressure chemical vapor deposition (LPCVD) at 600 °C. The polysilicon is then patterned by reactive ion etching (RIE) using a nickel mask to form the implant windows for n-well implantation. The n-well regions are formed by nitrogen ion implantation (total dose of 3.9×10^{13} cm⁻²). The nickel mask is then removed, and the wafer is thermally oxidized in wet oxygen for 9 h at 1000 °C. The lateral growth of the polysilicon fingers is measured to be $0.84~\mu$ m by scanning electron microscopy. Aluminum ions are then implanted using the expanded polysilicon and a gold optically aligned p⁺ block

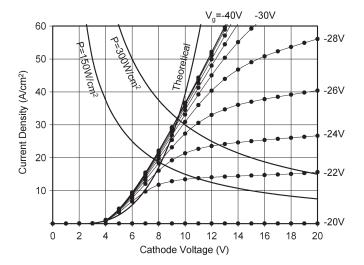


Fig. 2. Room-temperature cathode I-V characteristics of an experimental p-IGBT (active area $1.45\times 10^{-3}~{\rm cm}^2$) at gate voltages from -20 to -40 V in 2-V intervals. The theoretical curve at $V_q=-20$ V is plotted for comparison.

mask to form p^+ source regions. This self-aligned process [8] allows us to make a short channel (\sim 0.42 μ m) with conventional optical lithography. Metals and polysilicon are then removed. The n^+ base contact is formed by nitrogen ion implantation using a gold mask. All metals are then removed, and implant activation anneal is performed in SiH₄ at 1600 °C.

A preoxidation clean is performed, and the wafer is oxidized in a pyrogenic oxidation tube at 1150 °C for 150 min, followed by 1150 °C argon postoxidation anneal. The gate oxide thickness is around 50 nm as measured by ellipsometer. The wafer is then annealed in nitric oxide at 1175 °C for 2 h to reduce the interface state density [9]. A 400-nm polysilicon gate is deposited by LPCVD, doped by phosphorus spin-on dopant, and patterned by RIE. N-well and p⁺ source contacts are formed by depositing and patterning nickel (100 nm) and titanium/aluminum (33 nm/167 nm), respectively. A nickel backside contact is then deposited, and all contacts are annealed at 1000 °C in vacuum for 2 min. Finally, a 500-nm gold top metal is deposited and patterned. The device structure is similar to a p-channel DMOSFET, but with a p-n junction at the bottom.

III. RESULTS AND DISCUSSION

The room-temperature current–voltage I-V characteristic of the experimental p-IGBT is shown in Fig. 2. The cathode current density is plotted against cathode voltage for gate bias from -20 to -40 V in 2-V intervals. The threshold voltage is high due to the high doping concentration in the n-well surface region and possibly a high interface state density. A threshold-adjust implant (aluminum, 40 keV, $2-3\times 10^{13} \text{ cm}^{-2}$) will be used in future devices to reduce the threshold voltage to around 3 V. The peak inversion-layer field-effect hole mobility in these devices is $5.64 \text{ cm}^2/\text{V} \cdot \text{s}$, as measured by the constant-current method [10]. We assume that the device must operate under a 300 W/cm^2 package power dissipation limit. The operating frequency is typically chosen so that the switching loss is equal to the conduction loss (i.e., each 150 W/cm^2). If the duty cycle is 50%, the instantaneous power dissipation during the

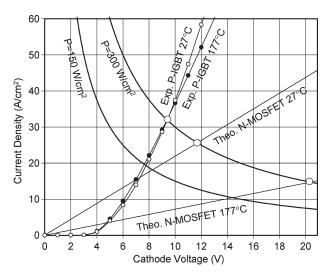


Fig. 3. I-V characteristics of the experimental 20-kV p-IGBT and a theoretical 20-kV n-MOSFET at 27 °C and 177 °C. Circles indicate the operating points at 27 °C and 177 °C, assuming a total power dissipation of 300 W/cm², 50% duty cycle, and switching loss equal to the conduction loss. The p-IGBT carries $1.2\times$ and $2.1\times$ higher current than the theoretical limit for the n-MOSFET at 27 °C and 177 °C, respectively.

portion of the cycle when the device is conducting will be 300 W/cm^2 . Under this assumption, the maximum current density is about 31 A/cm^2 . The theoretical I-V curve (obtained by MEDICI numerical simulation) is plotted for comparison. The experimental device has an ON-current density very close to the theoretical value at the 300 W/cm^2 power limit.

Fig. 2 also shows evidence of strong conductivity modulation in the $175-\mu m$ p-type drift layer. The experimental p-IGBT has less than 10-V drop to reach a current density of 31 A/cm², as opposed to over 150-V drop for a theoretical MOSFET with the same drift layer (no conductivity modulation).

Fig. 3 shows the experimentally measured I-V characteristics of the p-IGBT and theoretical simulation results for the n-MOSFET at 27 °C and 177 °C. The n-MOSFET shows obvious degradation at 177 °C due to a reduction in electron mobility with temperature [11], but the p-IGBT is almost invariant with temperature. This is because the determining factor for conductivity modulation is the ambipolar diffusion length $(L_A = (D_A \tau_A)^{1/2})$. The ambipolar diffusion coefficient D_A is proportional to mobility and decreases with T in power law form [11], whereas the ambipolar lifetime τ_A increases with T in power law form [12]. Therefore, the ambipolar diffusion length is almost independent of temperature from room temperature to 200 °C. This gives the SiC IGBT a significant advantage over the SiC MOSFET since power devices will reach high-junction temperatures if they are continuously operated at the package power limit. The circles in Fig. 3 indicate the operating points of the p-IGBT and n-MOSFET at 27 °C and 177 °C. The experimental p-IGBT carries 2.1× higher current than the theoretical limit for n-MOSFETs at 177 °C.

For vertical power devices with lateral dimensions comparable to the drift layer thickness, current spreading in the drift layer must be accounted for to correctly evaluate the ON-resistance [2]. However, numerical simulations on infinitely large IGBTs and finite-dimension IGBTs indicate that current

spreading has a negligible effect on the performance of finitedimension IGBTs. This is because the portion of the drift region outside the "shadow" of the active device does not have the same level of conductivity modulation as the area directly under the device. Consequently, the performance of our experimental devices is quite representative of that of a large-area device.

These experimental p-IGBTs are fabricated on 4H-SiC epilayers that are designed to block 20 kV. However, the experimental devices do not have the necessary edge terminations to achieve the full blocking voltage. Because of the thick lightly doped drift layer, the effect of junction curvature is very pronounced, and the breakdown voltage of an unterminated junction is expected to be less than 2 kV [13]. The maximum blocking voltage measured on devices with partial edge terminations is around 5 kV.

IV. CONCLUSION

We report the first 4H-SiC p-channel IGBTs built on 20-kV blocking epilayers. The ON-state performance agrees well with theoretical predictions. We have investigated the temperature dependence of the device performance and find that p-IGBTs provide approximately twice the ON-state current as MOSFETs at 177 °C. IGBTs are as simple to fabricate as MOSFETs, and their superior performance makes them promising candidates for power switching applications at blocking voltage of 10 kV and above.

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