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Nanoscale Transistors: Physics and Materials

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ABSTRACT

We analyze a modern-day 65nm MOSFET technology to determine its electrical characteristics and intrinsic ballistic efficiency. Using that information, we then predict the performance of similar devices comprised of different materials, such as high-k gate dielectrics and III-V channel materials. The effects of series resistance are considered. Comparisons are made between the performance of these hypothetical devices and future generations of devices from the ITRS roadmap, including double-gate MOSFETs. We conclude that a Si channel device with a high-k gate dielectric and metal gate will outperform III-V channel materials for conventional CMOS applications, but will still not suffice in achieving long-term ITRS goals.

INTRODUCTION

Much has been accomplished in the way of improving MOSFET device characteristics for continuation of Moore’s law. Strained silicon channels and modified gates and insulators have helped a lot, and the most current 65nm technology produces ~1600µA/µm of drive current with a 1.2V power supply and 1.2nm SiON gate insulator. But this is not enough, and new methods are needed to meet future ITRS roadmap requirements [1]. Options being explored include new device structures such as the tri-gate/finFET and new materials for the gate (FUSI/metal), insulator (high-k dielectrics), and channel (III-V semiconductors). This paper examines the extent to which these new materials options can address the device performance challenges at the end of the ITRS.

To predict how a new material or structure will affect performance, it is first necessary to understand the operation of a present-day device. A short review of the theory behind ballistic devices is presented in the next section, as a refresher for those familiar with the concepts, and as a brief but essential introduction for those who are unfamiliar. Topics include calculation of inversion charge, thermal and injection velocities, and ballistic drain current. In the analysis section, a detailed examination of the 65nm device is presented using actual experimental data for the transistor. Important device parameters such as leakage current, subthreshold swing and DIBL are taken directly from the published results, and accurate estimations for threshold voltage and series resistance are made based on both the ITRS roadmap and published measurements. We calculate the ballistic efficiency of the intrinsic device using a comparison of the on currents and of injection velocity. Our analysis supports a similar, recent study on the same device [2], and provides a starting point to examine various device options.
In the discussion section, we use a simple ballistic model to determine the performance of similar MOSFETs, but with different materials. The gate is made into a metal, the insulator a high-k dielectric, and the channel GaAs. Our conclusions are outlined in the final section. We find that for these device structures (with metal gates and high-k dielectrics), Si will have higher currents than GaAs in the low and high drain voltage regions, as well as for low gate voltages above threshold. Stated another way, the increase in current due to the addition of the same high-k dielectric (decrease in EOT) is much greater for Si than for a III-V material which has a low effective mass in the channel and confinement directions. Most importantly, we find that even if the ITRS goals of a high-k, metal, double gate structure operating at the ballistic limit in the channel with significantly lower series resistance are all achieved, they are not nearly enough to achieve the on-current target at the desired power supply.

THEORY

A model for analysis of MOSFETs is shown in figure 1. The source and drain contacts have well defined Fermi levels where carriers are in thermal equilibrium with the lattice. Hence, there is strong scattering in the source and drain regions but none in the channel in the ballistic limit. The maximum potential energy point on this conduction band diagram acts as the barrier to electrons in the channel and is known as the virtual source. In general, the MOSFET current above threshold can be expressed as

\[ I_D = WQ_i \langle \nu \rangle \]  

(1)

where \( W \) is the device width, \( Q_i \) is the inversion charge density at the top of the barrier (virtual source), and \( \langle \nu \rangle \) is the average electron velocity at the top of the barrier. Inversion charge density can be found from

\[ Q_i = C_G \left( V_{gs} - V_T \right) \]

**Figure 1.** Ballistic transport model for nanoscale MOSFETs.
\[ Q_i = -C_G (V_{gs} - V_T) \]  

(2)

where \( C_G \) is the gate capacitance (per unit area), \( V_{gs} \) the gate to source voltage in the intrinsic device, and \( V_T \) is the threshold voltage. Since we are dealing with an n-channel MOSFET, the inversion charge is negative.

For the ballistic MOSFET, current is defined by the carrier distribution at the top of the barrier, which consists of two parts; \( n^+ \) electrons (per m²) injected from the source to the drain at velocity \( v^+ \), and \( n^- \) electrons moving from the drain to the source at velocity \( v^- \). The net drain current is given by

\[ I_D = Wq \left( n^+ v^+ - n^- v^- \right) \]  

(3)

The negative portion of the carrier distribution diminishes with higher drain bias, but the total inversion charge at the top of the barrier is constant at

\[ Q_i = -q \left( n^+ + n^- \right) = -C_G (V_{gs} - V_T) \]  

(4)

Hence, the ballistic MOSFET current can be expressed as

\[ I_D = W C_G (V_{gs} - V_T) v^+ \left[ \frac{1 - \left( n^- / n^+ \right) \left( v^- / v^+ \right)}{1 + n^- / n^+} \right] \]  

(5)

\( n^+ \) and \( n^- \) are determined by the position of the source and drain Fermi levels with respect to the top of the barrier, and their accurate representation involves Fermi-Dirac integrals [3]. Note that due to quantum mechanical confinement of the carriers, the energy at the top of the barrier is not the conduction band but the first subband energy level \( \varepsilon_1 \) of the quantum well. Using these exact expressions, the ballistic MOSFET I-V characteristics are given by

\[ I_D = W C_G (V_{gs} - V_T) v_{inj} \left( \frac{1 - \mathcal{F}_{1/2} \left( \eta_F \right) - q V_D / k_B T_L}{1 + \mathcal{F}_0 \left( \eta_F \right) - q V_D / k_B T_L} \right) \]  

(6)

In these expressions, \( \eta_F = (E_F - \varepsilon_1) / k_B T_L \), \( \mathcal{F}_0 \) is the Fermi-Dirac integral of order zero, and \( \mathcal{F}_{1/2} \) of order one half [4]. \( v_{inj} \) is called the ballistic injection velocity and is given by

\[ v_{inj} = \sqrt{\frac{2 k_B T_L}{\pi m^*}} \mathcal{F}_{1/2} \left( \eta_F \right) \]  

(7)

For \( V_{ds} \gg k_B T_L / q \), the drain current from (6) saturates to

\[ I_D (on) = W C_G v_{inj} (V_{gs} - V_T) \]  

(8)
The ballistic efficiency of a device is the ratio between the actual on current and the ballistic on current from (8), or the ratio between the calculated average velocity \( \langle v \rangle \) (inversion charge must be known through (2)) and \( v_{inj} \) from (7).

**ANALYSIS**

A detailed analysis of a volume-manufactured device of today is presented to compare its performance with the ballistic limit. This 65 nm technology high-performance nMOS device has a uni-axially strained silicon channel and polysilicon gate [5]. For this work, the channel length is assumed to be the same as the quoted gate length of 35nm. The device has a SiON gate dielectric with an effective oxide thickness (EOT) of 1.2nm. At a supply voltage of \( V_{DD} = 1.2V \), the on-current is \( I_{ON} = 1620\mu A/\mu m \) with an off-current of \( I_{OFF} = 0.1\mu A/\mu m \). The subthreshold slope is \( S = 105mV/\text{dec} \) and DIBL is 150mV/V for this nMOSFET.

The drain current of a MOSFET above threshold is proportional to the number of carriers in inversion and the carrier velocity in the channel from (1). The inversion charge density per unit area in the channel is given by (2), and increases proportionately with the gate capacitance \( C_G \) in inversion. In inversion, poly gate depletion capacitance and the semiconductor capacitance add in series to the gate insulator capacitance, thus decreasing the gate capacitance. The effective oxide thickness in inversion (\( EOT_{elec} \)) for this nMOS device is estimated using Schred [6]. Our analysis shows that the poly gate depletion increases the EOT by about 0.35nm and the inversion layer thickness also adds another 0.35nm. Hence, the \( EOT_{elec} \) for this device is about 1.9nm, which is about 1.6 times the EOT for the oxide layer alone.

The inversion charge is also proportional to the gate overdrive \( V_{GS} - V_T \) in the on state. The threshold voltage for this device is extracted from the \( g_m/I_D \) vs. \( V_{GS} \) plot, and is found to be 0.3V. Gate overdrive needs to be computed using the intrinsic \( V_{GS} \) in the channel by eliminating the voltage drop at the source due to parasitic source series resistance. It is assumed that the source and drain series resistances are equal, and we estimated the parasitic series resistance of this device to be \( R_{SD} = 175 \Omega \cdot \mu m \). Hence, at the on condition when the gate voltage is at \( V_{DD} \), the net inversion electron density is computed to be \( 8.6 \times 10^{12} \text{ cm}^{-2} \).

The average carrier velocity for a MOSFET can be obtained from the on current using (1). As the on current for this device is 1620\( \mu A/\mu m \), using the carrier density computed above, the average carrier velocity is \( \langle v \rangle = 1.17 \times 10^7 \text{ cm/s} \). This compares reasonably well with the study in [2] which presents effective velocity of about \( 1.1 \times 10^7 \text{ cm/s} \) for a DIBL of 150mV/V, which corresponds to the analyzed device. The computed carrier velocity can be compared to the theoretical ballistic limit to find the ballistic efficiency, as discussed in the theory section.

Assuming parabolic bands and single subband occupation, the ballistic injection velocity vs. inversion carrier density is plotted in figure 2. For the device analyzed, \( v_{inj} = 1.65 \times 10^7 \text{ cm/s} \) from figure 2, suggesting a ballistic efficiency of 0.7 for the intrinsic device. However, the \( v_{inj} \) data is computed using a silicon transverse effective mass of 0.19\( m_0 \). As the device being analyzed has a strained silicon channel, the transverse effective mass will be lower [7], and hence the ballistic injection velocity will be higher. Thus, the true ballistic efficiency is likely closer to 0.65--0.7 for this device. This is also close to the analysis in [2] which predicts a ballistic efficiency of 0.6--0.65.
Both saturation and linear region of operation are important for device switching considerations, and so resistance in the linear region $R_{\text{lin}}$ is an important figure of merit. The linear region resistance is shown in figure 3 as a function of gate voltage. Eliminating the parasitic source/drain resistance, the intrinsic channel resistance $R_{\text{ch}}$ is found to be 50 $\Omega$-$\mu$m at the on-state, which is almost double the plotted ballistic series resistance limit. Figure 4 compares the I-V characteristics of this device with its ballistic limit, and shows that series resistance is the major limiting factor today. Scattering in the channel is much less important than scattering in the source and drain. Hence, series resistance plays a significant role in limiting the ultimate device performance, and ways to decrease its effect will have a great impact.
DISCUSSION

As devices continue to be scaled down according to Moore’s law, materials innovation is required to manage electrostatics and achieve higher performance. Polysilicon depletion is a major concern with current day devices, and the gate material should be replaced with metal gate in the near future. Scaling of gate dielectric thickness has stopped at 1.2nm in order to limit quantum mechanical gate leakage. New high-k dielectric materials need to be developed to continue increasing gate capacitance. Also, new higher mobility channel materials will be required to improve transport properties. Different device geometries and structures like double gate MOSFETs will also contribute to improve performance. Here, we analyze the potential impact of these modifications on the ultimate performance of MOSFETs. The modifications were applied to the current generation device, and the performance gain is compared to the projected ITRS high performance logic roadmap for year 2020.

Metal gate

A self-consistent solution of the Schrödinger and Poisson equations was performed using Schred [6] to analyze the performance improvement by using metal gate. The device dimensions are the same as the 35nm channel length device analyzed above. The workfunction of the metal gate was adjusted to match the threshold voltage of the original device, while the channel doping was kept comparable. Results for the metal gate and gate capacitance of the real device are plotted in figure 5. The improvement of gate capacitance in inversion can be observed at $V_{GS} = V_{DD} = 1.2V$. There is no gate depletion term for the metal gate and so the gate capacitance is 30% higher than the otherwise comparable polysilicon gate device. Elimination of the polysilicon depletion has reduced the effective electrical oxide thickness ($EOT_{elec}$) from 1.9nm to
1.55nm, which is still 1.3 times EOT. The improvement in gate capacitance directly reflects a corresponding 30% increase in the inversion charge and hence improvement of on current.

**High-k gate dielectric**

Replacing the polysilicon gate by metal is not enough to keep following the scaling trends predicted by ITRS. As channel lengths get shorter with every future generation, gate insulator capacitance needs to be scaled up to keep short channel effects under control. Without going into any of the complexities of developing high-k dielectric materials and their compatibility with channel materials, we will assume that high-k materials will be available in future to meet the ITRS predictions. The ITRS high performance logic requirements for the year 2020 quote the required electrical oxide thickness (EOT) to be 0.5nm. Gate capacitance for a future MOSFET with this EOT is plotted in figure 6. The gate capacitance at inversion is about three times higher than current day technology. The inversion charge also increases proportionately causing an increase in the effective inversion layer thickness. Thus, the overall $EOT_{elec}$ is smaller, but is increased from 1.3 times $EOT = 1.2$nm to 1.4 times $EOT = 0.5$nm.

**Double gate**

Apart from using new materials, another potential way to improve device electrostatics and induce higher number of carriers is to modify the device geometry. The ITRS predicts the use of double gate (DG) MOSFET structures from year 2011 to continue the device scaling according to Moore’s law. It is instructive to compare the ultimate performance of double gate structures and devices with high-k insulators corresponding to ITRS projection for year 2020 with the present day devices. Figure 7 compares the ballistic drain current vs. drain to source voltage for a few such devices with metal gates and $R_{SD} = 175$ Ω-µm at $V_{GS} = V_{DD} = 1.2$V. The on current of the 65nm device can be improved by 45% by incorporating metal gate and operating at the
Figure 6. Comparison of gate capacitance for high-k gate dielectrics. These are ITRS predictions for high performance logic, year 2020 ($EOT = 0.5\text{nm}$) and current technology ($EOT = 1.2\text{nm}$), both with metal gates.

ballistic limit. Incorporating high-k dielectrics ($EOT = 0.5\text{nm}$) improves the current drive by another 50%. About 40% more improvement can be expected with double gated structures at $EOT = 1.2\text{nm}$, but at $EOT=0.5\text{nm}$ the on-current increases by 20%. Though the future generation devices will be driven at lower supply voltage, the trend is expected to be very similar, as seen in the following subsection.

Figure 7. Projected $I_D$ vs. $V_{DS}$ plots for Si, Si with high-k, Si double gate, and Si double gate with high-k, all metal gate ballistic MOSFETs with $R_{SD} = 175\ \Omega\cdot\mu\text{m}$. High-k denotes $EOT = 0.5\text{nm}$ (ITRS high performance logic, prediction for year 2020.)
GaAs channel

As noted earlier, the MOSFET current is governed by the inversion carrier density as well as the carrier velocity. Improving the gate and insulator materials will improve 2-D electrostatics. Modifications to the channel material are required to enhance the transport properties. The current generation device analyzed above uses strained silicon to improve the effective mobility (by an enhancement factor of ~1.6 [5]). Future generation devices will need channel materials with lower effective mass in the transport direction to improve the carrier velocity. III-V materials like GaAs are possible candidates for replacing silicon based devices because it is believed that they will operate with high speed at lower power supply voltages [8]. GaAs has an effective mass of $m^* = 0.067m_0$, which is about a third of the transverse effective mass of silicon ($m_t = 0.19m_0$). Carriers with smaller effective mass are expected to have higher mobility and operate closer to the ballistic limit. However, the ballistic injection velocity limit is also increased as it varies inversely with the effective mass. A lower effective mass also results in a lower gate capacitance at inversion due to a small density of states, causing a reduced carrier density. Figure 8 compares the overall ballistic performance of GaAs devices to silicon devices.

![Figure 8](image.png)

Figure 8. Projected $I_D$ vs. $V_{DS}$ plots for Si, GaAs, Si with high-k, and GaAs with high-k for: (a) planar MOSFET with $V_{DD} = 0.6$ V, (b) planar MOSFET with $V_{DD} = 1.2$ V, (c) double gate MOSFET with $V_{DD} = 0.6$ V, (d) double gate MOSFET with $V_{DD} = 1.2$ V. Ballistic transport, metal gate and $R_{SD} = 55 \, \Omega \cdot \mu m$ is assumed for all devices.
Parasitic series resistance is assumed to be $R_{SD} = 55 \, \Omega \cdot \mu m$ according to ITRS high performance logic prediction for year 2020. Figure 8(a) compares a GaAs channel device with a silicon device with $EOT = 1.2\,\text{nm}$ and $0.5\,\text{nm}$ at $V_{DD} = 0.7\,\text{V}$, and figure 8(b) does the same at $V_{DD} = 1.2\,\text{V}$. It is evident that at $EOT = 1.2\,\text{nm}$ the improvement in mobility is dominant, resulting in superior performance of the III-V device. At $EOT = 0.5\,\text{nm}$ the increase in carrier density is much higher for silicon devices, and the lower inversion capacitance of III-V materials hinders their performance. Figure 8(c) and (d) plots the same characteristics for double gate MOSFETs, and its evident that silicon devices have better on-current than GaAs devices at all $EOT$. Also note that linear region slope of the curves denote channel resistance, which becomes important during switching. The saturation voltage of Si device is lower than GaAs, suggesting a lower $R_{ch}$, which may improve the switching delay at the system level [9]. However, the ITRS high performance logic prediction for year 2020 quotes on current of 2981 $\mu A/\mu m$ at a supply voltage of 0.7V. Our results show that the silicon double gate MOSFET with metal gate and $EOT = 0.5\,\text{nm}$ operating at $V_{DD} = 0.6\,\text{V}$ at the ballistic limit still cannot meet the ITRS predicted value.

CONCLUSIONS

Using a present-day 65nm n-channel MOSFET as a starting point, we estimated the ballistic operation of similar devices made of different materials. Our results show that higher drive currents are achieved using III-V channel materials only when the EOT is large and the device is planar. Even then, saturation voltages are higher than that for Si. The lowest saturation voltages and very highest on currents are achieved with a ballistic double-metal-gate Si channel device with a high-k dielectric as an insulator and a series resistance of the ITRS target of 55 $\Omega \cdot \mu m$. Even with the ITRS specifications for the gate stack, series resistance, double gate structure, and ballistic operation within the channel, the 2020 ITRS on-current target for high-performance cannot be achieved. The best on-current achieved under our optimistic assumptions is ~80% of the ITRS target. High-k gate insulators and metal gates provide useful performance gains, but III-V channel materials do not help at the end of the ITRS. It is our belief that to continue scaling, it will be necessary to go beyond the conventional MOSFET altogether. New materials are not enough.

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