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Self-aligned wafer-level integration technology with an embedded faraday cage for substrate crosstalk suppression

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it can be noticed and confirmed by the plot of the cost function $F(\chi)$ versus the iteration number (see Fig. 4), the electric behavior of the trial solution evolves from an unsatisfactory compliance with the project constraints until an accurate fitting.

To complete the assessment with an experimental analysis, a prototype of the fractal-shaped patch antenna (see Fig. 5) has been built by using a photolithographic printing circuit technology. Then, it has been equipped with an additional ground plane of dimensions $90 \times 140 \text{ cm}^2$ for approximating the numerical modeling of the simulated structure (i.e., the patch over an infinite ground plane). For comparison purposes, simulated and measured (in an anechoic chamber) VSWR values are reported in Figure 6. As it can be observed, there is a good agreement that further points out the reliability of the numerical synthesis procedure.

Finally, for completeness, the radiation properties of the synthesized antenna are analyzed. In particular, the plots of the horizontal and vertical ($\phi = 0^\circ$) gain patterns are shown in Figure 7. As expected, the obtained results turn out compliant with the project specifications since an hemispherical coverage, suitable for both GPS and mobile communication systems, is obtained whatever the frequency band.

4. CONCLUSIONS

In this letter, the design of a three-band fractal-shaped patch antenna has been described. Starting from a set of design constraints, the perimeter of the rectangular reference structure has been iteratively modified by optimizing the descriptors of the fractal boundaries and the position of the input port through a PSO-based procedure. The synthesized structure has been analyzed both numerically and experimentally by considering an antenna prototype.

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SELF-ALIGNED WAFER-LEVEL INTEGRATION TECHNOLOGY WITH AN EMBEDDED FARADAY CAGE FOR SUBSTRATE CROSSTALK SUPPRESSION

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ABSTRACT: A modification to a recently developed chip/wafer integration technology has proven to be very effective in suppressing the substrate crosstalk for mixed signal systems. In this implementation, analog and digital chips are fabricated on separate dies, and then integrated on a single Si substrate using a Self-Aligned Wafer-Level Integration Technology. A truly grounded faraday-cage structure is realized by sidewall metallization around each die resulting in an ultimate substrate noise reduction. Any planar chip with any thickness can be used in this technology. Simulation and measurement results show that when a high-resistivity silicon substrate as an integration medium is used along with grounded faraday cage, substrate coupling is suppressed to less than -60 dB for frequencies up to 25 GHz . For a low-resistivity silicon substrate, the substrate coupling is a dominant mechanism in generating mixed-signal noise, however, when sidewall metallization as faraday cage is utilized, the substrate coupling is reduced by at least 20 dB for frequencies below 25 GHz . The substrate noise suppression is higher than 35 dB for frequencies below 2 GHz . To our knowledge, these are the best values reported for isolation improvement of thick silicon substrates at microwave frequencies. © 2008 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 50: 829–832, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23207

Key words: integration; mixed-signal circuits; microwave integrated circuits; substrate crosstalk; system-on-chip

1. INTRODUCTION

High performance densely-packed integrated mixed-signal circuits for System-on-Chip (SoC) applications suffer from substrate noise coupling. In a typical SoC mixed-signal circuit, noise is injected into the substrate from switching transistors because of the parasitic capacitance between the transistor channel and the substrate. A resistor network is usually used to model the common substrate on which both digital and analog circuits are embedded. Therefore, the resistor network propagates the noise across the substrate as shown in Figure 1(a). The propagated noise is injected into sensitive analog or RF circuitry through the parasitic capacitance between the substrate and analog (or RF) transistor. At frequencies above its dielectric relaxation time constant, the silicon substrate behaves as a lossy dielectric which requires a combination of parallel capacitor and resistor in the noise propagation model. This coupling mechanism, which is caused by the semi-conductive nature of the substrate and parasitic effect of the device layout, enhances the digital noise coupled into the sensitive analog or RF circuit at high frequencies [1].

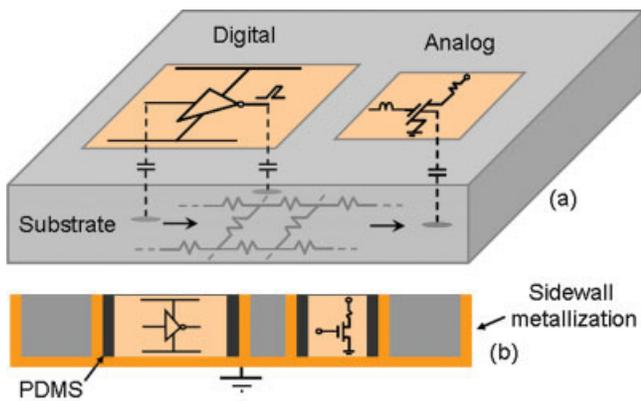


Figure 1 (a) Illustration of substrate coupling for a common substrate, (b) Reduction of substrate coupling using sidewall metallization in SAWLIT. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

Many isolation techniques to reduce substrate crosstalk have been proposed such as guard rings [2, 3], junction-isolated wells [3], SOI substrates [2-5], high-resistivity SIMOX (Separation by IMplanted OXYgen) substrates [6, 7], metal-filled trenches [8], and a ring of metal-filled vias [9]. In general, most of these techniques require a large footprint and thick metallization and become ineffective at high frequencies. The method in [9] shows significant isolation improvement through implementing a faraday cage based on a ring of grounded vias that surrounds the noisy or sensitive circuit. This technique is applied to a thin substrate ($77\ \mu\text{m}$) with vias of $10\ \mu\text{m}$ diameter. Applying this technique to a thick substrate ($550\ \mu\text{m}$) requires either very high aspect ratio vias that are challenging to implement (aspect ratio more than 50) or large diameter vias (diameter $>50\ \mu\text{m}$) that occupy large chip area.

In this work, we have demonstrated a truly faraday-cage structure to suppress the substrate crosstalk in mixed-signal circuits. The faraday cage is readily implemented on a recently developed heterogeneous integration technology as conceptually shown in Figure 1(b).

2. TECHNOLOGY

The requirement of good performance and low cost at high operating frequencies cannot be achieved either by system in package (SiP) or SoC approaches. It is the synergistic development of technologies that will enable excellent performance, agility, and multifunctionality, while constraining the manufacturing cost. The integration technology shown in this work achieves monolithic performance similar to SoC using hybrid heterogeneous integration similar to SiP. This is achieved by tightly integrating various optimized chips and components.

In [10, 11], a self-aligned wafer-level integration technology (SAWLIT) suitable for Microwave Integrated Circuit (MMIC) has been reported. Heterogeneous integration of analog, digital, and RF chips is achieved by embedding them in a Si interposer substrate. This integration scheme offers several advantages over standard wirebonding and flip-chip technologies [12]. Single substrate solution, batch fabrication of the integration process, availability of high-Q embedded passive components, low integration cost, low power dissipation, heterogeneous integration capability, easy technology revisions and quick time to market, minimum parasitics, and reduced substrate coupling are some of these advantages.

Figure 2 illustrates the process flow for SAWLIT that is mod-

ified to include faraday cage metallization around each die. In this process, first the Si interposer is etched using deep reactive ion etcher (DRIE) with cavities slightly larger than the size of the chips that are to be integrated. $4\ \mu\text{m}$ Au/Al metallization is sputtered on the backside of the Si interposer to cover the sidewalls as well as the backside as shown in Figure 2(a). The interposer is attached to a handling substrate using soft-baked photoresist and various analog and digital chips are inserted in to their corresponding cavities as shown in Figure 2(b). Each chip is inserted upside down to its corresponding cavity whose size is optimally chosen to self position the chip with a placement error of only a few micrometers. The gap between the chips and Si substrate typically less than $10\ \mu\text{m}$ is filled with poly-di-methyl-silicone (PDMS) as shown in Figure 2(c). The interposer substrate containing the chips is separated from the handling substrate by dipping the wafers in acetone as shown in Figure 2(d). The process is completed by applying a planarization layer (SU-8), opening vias, and lithographically printing chip to substrate interconnects and embedded passive components as shown in Figure 2(e). Lithographic defined interconnect lines as narrow as $25\ \mu\text{m}$ are easily achieved in this process [10]. Figure 3 shows photomicrographs of the integration process for a single die as well as multiple dies (batch fabrication).

One of the advantages of this technology which has been proven in this article for the first time is the substrate crosstalk suppression. Crosstalk is simulated and measured using several two-port structures. Each two port structure consists of transmitter and receiver pads fabricated in a coplanar ground-signal-ground configuration. The separation distance between the transmitter pads on the Si interposer and receiver pads on a Si die is varied from $100\ \mu\text{m}$ to $400\ \mu\text{m}$. Identical structures are implemented on

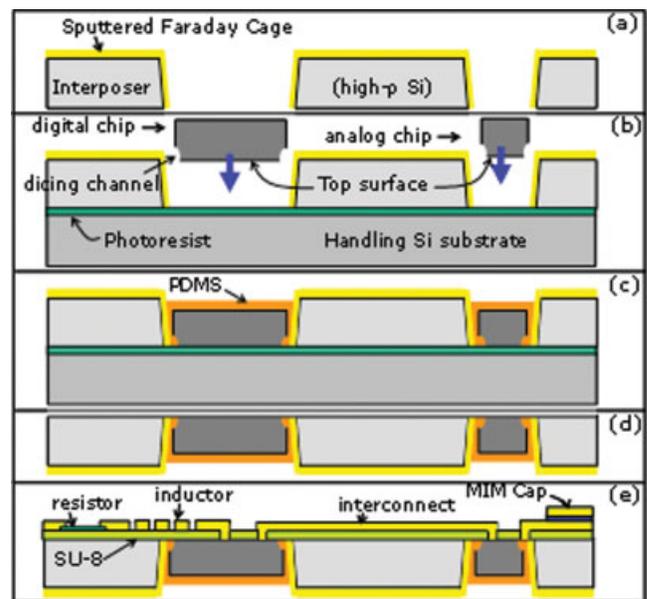


Figure 2 Process steps for the SAWLIT with faraday cage (a) Si interposer layer is etched all the way with cavities about $10\ \mu\text{m}$ larger than the size of each chip. Faraday cage metallization is sputtered on the interposer (b) The Si interposer is attached to a handling substrate and various chips are inserted upside down. The chips are positioned within a few microns of their ideal location in a self-aligned manner. (c) PDMS is applied and polymerized at room temperature to fill the gaps. (d) The interposer is separated from the handling wafer. (e) Planarization layer, vias, interconnects and embedded passives are defined using standard lithography, etching, and lift-off. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

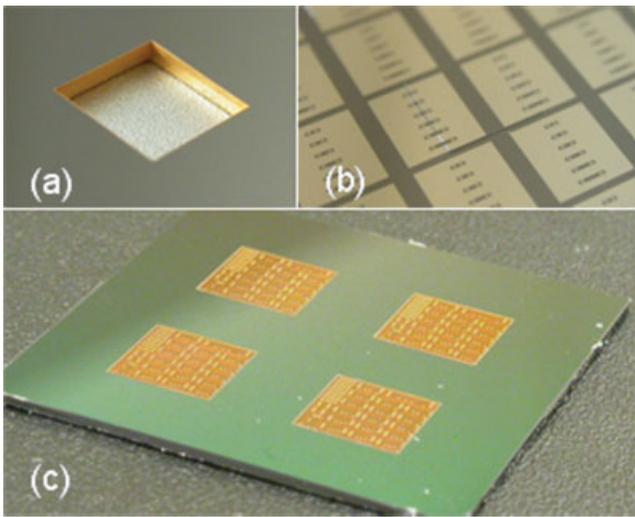


Figure 3 Photomicrographs of the integration process. (a) Metallized cavity formed inside the Si interposer substrate. (b) Transmitter and receiver pads with various distances (100–400 μm) are printed over the Si interposer substrate with a die embedded inside it. (c) Batch fabrication of four identical chips integrated inside the Si interposer. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

only the Si interposer substrate as a reference for comparison purpose [See Fig. 3(b)]. Two different Si interposer substrates, one with a resistivity of less than 10 $\Omega\text{ cm}$ and the other with a resistivity of more than 10 $\text{k}\Omega\text{ cm}$ have been used.

3. CHARACTERIZATION

Agilent 8722 network analyzer with on-wafer probe measurement is used to measure the S-parameters of the fabricated structures. Three-dimensional electromagnetic simulation using Ansoft HFSS is performed to simulate the fabricated structure for the sake of comparison. Figures 4(a) and 4(b) illustrate the simulation and measurement results of isolation for a two-port structure with the separation distance of 100 μm for a high-resistivity and a low-resistivity Si wafer, respectively. As the results show, the measured (Curves A) and simulated (Curves B) S_{21} for the reference structure match very well. The difference between the crosstalk on low resistivity Si and high resistivity Si is observed at lower frequencies (below 5 GHz) where the isolation for low-resistivity Si does not dip and remains at about -45 dB . Curves (C) illustrate the effect of PDMS on the crosstalk in a standard SAWLIT process. SAWLIT process without sidewall metallization in the cavities is an effective way of suppressing the cross talk at frequencies below 10 GHz for low resistivity Si substrate. This process when implemented on high resistivity Si substrate only marginally suppresses the crosstalk (by 2 to 3 dB in this case) when compared with the reference measurement made on high resistivity Si substrate. Curves (D) and (E) shows the measured and simulated results of the crosstalk, respectively, when SAWLIT process with sidewall metallization is used. As can be seen from the figure, a substantial improvement in crosstalk suppression is achieved for both low and high resistivity Si substrates. The measured result is slightly higher than the simulated results mainly because the crosstalk is very close to the noise floor of the system shown in Curves (F).

Figures 5(a) and 5(b) show the measured isolation (S_{21}) at 5 GHz when the separation distance between transmitter and receiver ports are varied from 100 μm to 400 μm on both high and

low resistivity silicon substrates, respectively. The reference measurements are also provided for comparison. As the distance between the two ports increases, the isolation generally improves. The isolation of the structures with faraday cage is always better than that of the reference measurement. The isolation measurement for the separation of 200 μm on high resistivity Si substrate with sidewall metallization is slightly worse than that of 100 μm separation. This is due to measurement uncertainties when very high isolation levels (approximately -70 dB) are being measured.

4. CONCLUSION

A new mixed-signal substrate crosstalk suppression technique has been demonstrated using a recently-developed SAWLIT. Analog and digital chips can be separately fabricated and then integrated using this heterogeneous integration technology. A truly grounded faraday-cage structure has been realized by sidewall metallization of each cavity in the Si interposer that is used as the integrating substrate. In this technique, substrates with any thickness can be used. The results show significant substrate crosstalk suppression

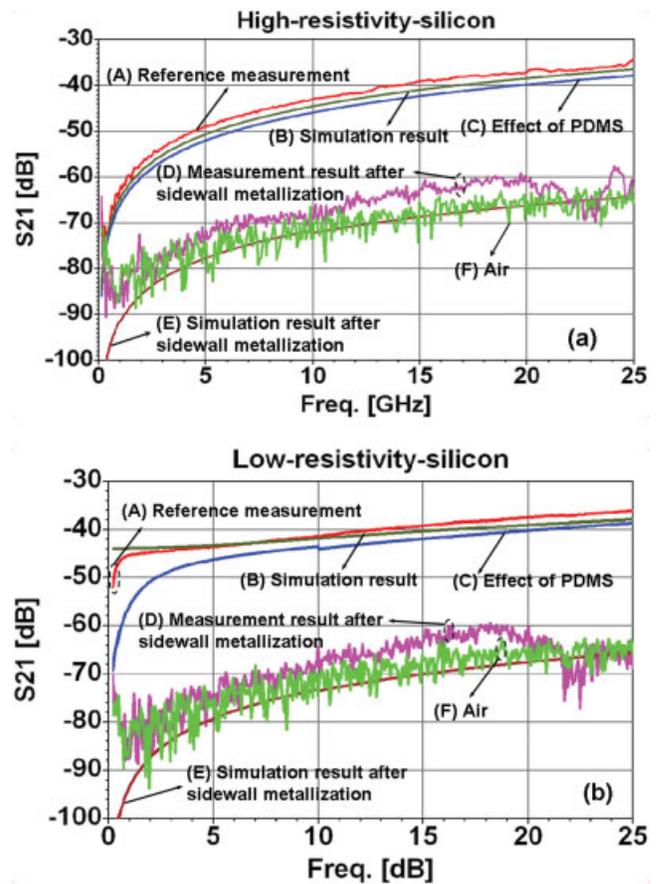


Figure 4 Simulation and measurement results of isolation for a two-port structure with the separation distance of 100 μm on (a) a high-resistivity and (b) a low-resistivity silicon substrate. Curves (A) show the reference measurement and curves (B) show the simulation results of the isolation of the reference structure fabricated on the Si interposer without any embedded chip. Curves (C) show the simulated isolation of the structure laid out on the Si interposer and the chip with PDMS filling the gaps but without any sidewall metallization. Curves (D) and (E) show measured and simulated isolation of the structure overlaying the Si interposer and the chip with both PDMS and sidewall metallization filling the gaps. Curves (F) show the measured isolation when the probes are lifted slightly above the substrate. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

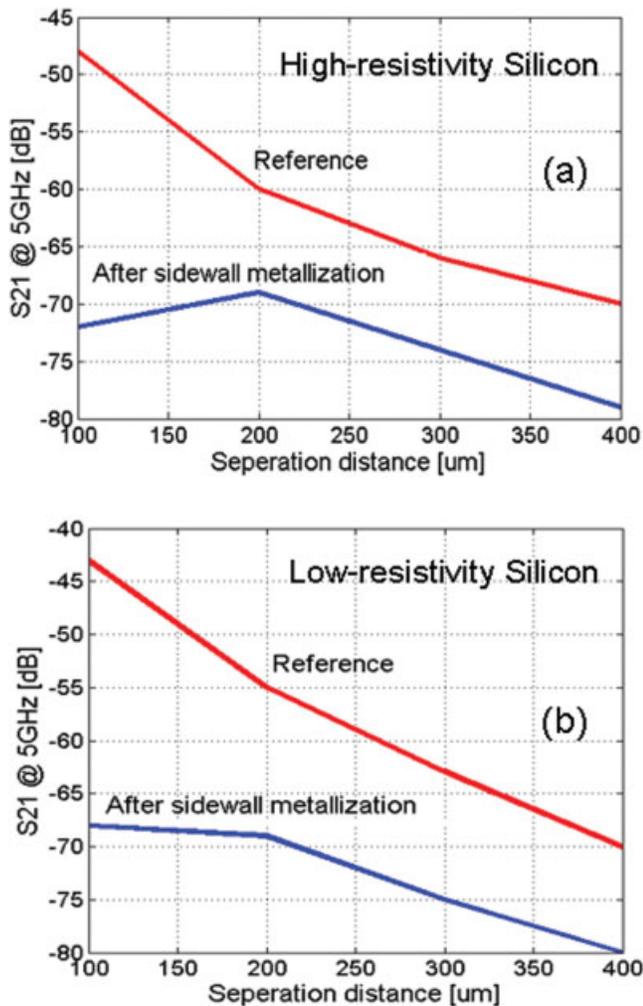


Figure 5 Isolation (S_{21}) of reference structure and structures with sidewall metallization measured at 5 GHz when the separation distance between the two ports is varied from 100 μm to 400 μm . Results for both high resistivity Si substrate (a) and low resistivity silicon substrate (b) are shown. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

to levels comparable with the noise floor of the system over the entire frequency range. To our best knowledge, these results are the best reported crosstalk suppression implemented on thick silicon substrate.

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SOLUTION OF ELECTROMAGNETIC SCATTERING PROBLEMS BY TRANSFORMATION INTO HIGH ORDER IMPEDANCE BOUNDARY CONDITION

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ABSTRACT: In this study, electromagnetic scattering from inhomogeneous impedance cylinder of arbitrary shape have been solved by means of transformation of problem into equivalent problem, that is scattering from circle represented by high order inhomogeneous impedance boundary condition (IBC). High order impedance functions are determined by using shape of object and its surface impedance. Then, equivalent problem is solved by means of series expansion method. This transformation makes the problem simple formulation, which can be solved computational effectively. Results and computational times obtained by transform method and those obtained by Method of Moment (MoM) technique are compared. Good agreements are observed in results. It is also observed that transform method needs less computational time than MoM method. © 2008 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 50: 832–836, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23200

Key words: electromagnetic scattering; impedance boundary condition; Radar Cross Section

1. INTRODUCTION

Scattering of electromagnetic waves from objects is one of the research topics in electromagnetic theory and establishes physical background of some practical application, such as radar cross