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Theoretical investigation of surface roughness scattering in silicon nanowire transistors

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Using a full three-dimensional (3D), quantum transport simulator, we theoretically investigate the effects of surface roughness scattering (SRS) on the device characteristics of Si nanowire transistors (SNWTs). The microscopic structure of the Si/SiO₂ interface roughness is directly treated by using a 3D finite element technique. The results show that (1) SRS reduces the electron density of states in the channel, which increases the SNWT threshold voltage, and (2) the SRS in SNWTs becomes less effective when fewer propagating modes are occupied, which implies that SRS is less important in small-diameter SNWTs with few modes conducting than in planar metal-oxide-semiconductor field-effect-transistors with many transverse modes occupied. © 2005 American Institute of Physics. [DOI: 10.1063/1.2001158]

The silicon nanowire transistor (SNWT) is attracting broad attention as a promising structure for future electronics. Therefore, understanding carrier transport in Si nanowires becomes increasingly important. Careful studies are needed to experimentally explore transport in SNWTs, but it is also clear that a theoretical understanding is similarly important. In this letter, we present a theoretical exploration of the Si/SiO₂ interface roughness scattering, or surface roughness scattering (SRS), in SNWTs.

It is well-known that scattering due to Si/SiO₂ interface roughness is important in planar silicon metal-oxide-semiconductor field-effect transistors (MOSFETs). It is expected to be even more important in ultrathin-body silicon-on-insulator (UTBSOI) MOSFETs. For bulk MOSFETs, electrons are confined at the Si/SiO₂ interface by an electrostatic potential well. Under high gate bias, the potential well is thin, electrons are confined very near the interface, SRS increases, and the effective mobility decreases. For UTBSOI MOSFETs, the confining potential is determined by the film thickness, and SRS can be enhanced by the roughness at the two interfaces. In a SNWT, the channel is surrounded by the Si/SiO₂ interfaces, so one might expect SRS to dominate transport. We will show, however, that SRS may be less important in SNWTs than in planar devices because of the one-dimensional (1D) nature of the SNWT channel.

In Ref. 6, we developed a full three-dimensional (3D), quantum transport simulator of SNWTs based on the effective-mass approximation. In this work, to investigate the effects of SRS on small-diameter (~3 nm) SNWTs with physically rough Si/SiO₂ interfaces, we make use of this previously developed simulator. The simulated structure is a gate-all-around SNWT with a rectangular cross section and a [100] oriented channel (see Fig. 1). Following previous work on SRS, we assume an abrupt, randomly varying interface between the Si and SiO₂, parametrized by a root mean square (rms) amplitude and an autocovariance function. The statistical nature of the roughness will depend on the nanowire fabrication methods and may differ considerably from that arising during the high temperature oxidation of a planar Si surface. Nevertheless, since our objective is to discuss general insights into the physics of SRS in SNWTs, we will employ the roughness parameters for a planar (100) Si/SiO₂ interface obtained from Ref. 7. Our use of a continuum level description may be questioned, but we believe that it is a valid approximation.
domain with a 3D finite element mesh; each element is
the following procedure. We first discretize the simulation
roughness is implemented into the 3D simulator according to
scattering rate, we treat the physically rough structure di-
rectly.

The microscopic structure of the Si/SiO$_2$ interface
roughness is implemented into the 3D simulator according to
the following procedure. We first discretize the simulation
domain with a 3D finite element mesh,$^6$ each element is a
triangular prism with $2\text{ Å}$ height and edge length, compa-
able to the size of roughness at the (100) Si/SiO$_2$ interface.$^7$
Next, we generate a two-dimensional (2D) random distribu-
tion across the whole Si/SiO$_2$ interface (unfolding the four
interfacial planes into a sheet) according to an exponential
autocovariance function,$^7$

$$C(x) = \Delta_m^2 e^{-x^2/L_m^2},$$

(1)

where $L_m$ is the correlation length, $\Delta_m$ is the rms fluctua-
tion of the roughness, and $x$ is the distance between two sampling
points at the interface. Based on the 2D random distribution,
the types of the elements at the Si/SiO$_2$ interfaces may be
changed from Si to SiO$_2$ or reversely, to mimic the rough
interfaces [see Fig. 1(b)]

After the roughness is implemented, electron transport
through the rough SNWT is simulated by using the nonequi-
librium Green’s function approach.$^9$ With a coupled mode
space (CMS) representation,$^6,10-12$ the wave function defor-
mation due to the roughness is treated. (The simulation
methodology has been described in detail in Refs. 6 and 10.)
To emphasize the role of SRS on electron transport, we do
not include any other scattering mechanisms, so coherent
transport is assumed inside the device. (Oscillations in the
current due to quantum interference might be expected, but
the averaging over a thermal distribution of wavelengths that
occurs is sufficient to suppress them.) The length of the
channel (10 nm) is long enough to ensure that sufficient av-
ergaging takes place so that sample specific effects are not
observed. The simulated results for the rough SNWT are
then compared with those for a device with the same geo-
metrical parameters (e.g., nominal oxide thickness and Si
body thickness) but smooth Si/SiO$_2$ interfaces. By doing this,
the effects of SRS on SNWT device characteristics can be
clearly identified.

Figure 2 plots the electron subband profile (left column)
at the ON-state ($V_{GS}=0.4 \text{ V}$) in the simulated SNWT
with rough and smooth Si/SiO$_2$ interfaces. The corre-
sponding transmission coefficients (right column) for both
the rough and smooth SNWTs are also shown. Note that
the modes are coupled in the simulation; we show them sep-
arrately for illustrative purposes only. It is clearly seen in
the energy versus $X$ plot that the presence of the roughness
introduces significant fluctuations in the electron subbands,
which lead to fluctuating elements in the diagonal terms of
the device Hamiltonian [for details, see Eq. (7) in Ref. 6] and
act as a scattering potential. At the same time, the shape of
the confined wave function also varies from slice to slice
along the wire in the rough SNWT [see Fig. 1(c) for an
example], which produces deformation and coupling ele-
ments in both diagonal and off-diagonal terms of the device
Hamiltonian [for details, see Eqs. (7), (8b), and (8c) in Ref.
6], and consequently lowers the transmission. (This effect
has been named “wavefunction deformation scattering,”$^{13-15}$

To examine the significance of wave function deformation
scattering, we plot an energy versus transmission curve (dotted-
dashed) for the rough SNWT calculated by the uncoupled
mode space (UMS) approach,$^8$ in which only the variations
in the electron subbands are included while the deformation
and coupling terms are discarded. The fact that the UMS
approach significantly overestimates the transmission for the
rough device infers that wave function deformation scatter-
ing dominates the transport. This is an important finding be-
cause common perturbation theory treatments$^3-5$ of SRS
scattering typically treat the subband energy fluctuations but
not the wave function deformation scattering.

From the energy versus transmission plot, we find that
the difference between the transmission curve for the rough
SNWT and that for the smooth device becomes more and
more noticeable as energy increases. This occurs because as
energy increases, more subbands (modes) become conduc-
tive and the coupling between different modes efficiently re-

FIG. 2. Electron subband profile [for the (010) valleys] and the cor-
responding transmission coefficients for the simulated SNWT ($W_S=3 \text{ nm}$) with
smooth and rough Si/SiO$_2$ interfaces. The roughness parameters used are
$L_m=0.7 \text{ nm}$ and $\sigma_m=0.14 \text{ nm}$ (Ref. 7). The device is at the ON-state ($V_{GS}=0.4 \text{ V}$), so the source and drain Fermi levels are equal to 0 eV
and $-0.4 \text{ eV}$, respectively.

FIG. 3. $I_{DS}$ vs $V_{GS}$ curves for the simulated SNWT ($W_S=3 \text{ nm}$) with
smooth (solid) and rough (dashed with symbols) Si/SiO$_2$ interfaces. ($V_{GS}=
0.4 \text{ V}$). Three samples (triangles, crosses, and circles) of the rough SNWT
are generated based on the same roughness parameters ($L_m=0.7 \text{ nm}$ and
$\sigma_m=0.14 \text{ nm}$) but different random number seeds. The SNWT threshold
voltage ($V_T$) is defined as $V_T=V_{GS}, V_{DS}=0.4 \text{ V}$) = $2 \times 10^{-7} W_S(A)$, where $W_S$ is in nm. The inset illustrates the reduction of electron DOS at
low injection energies caused by SRS.
duces the transmission in the rough SNWT. In other words, SRS becomes more significant as more modes conduct. As we will show later, this effect has an important impact on the role of SRS on SNWT device characteristics.

Figure 3 plots the $I_{DS}$ vs $V_{GS}$ curves in a semilogarithmic scale for both the rough and smooth SNWTs. The results show that there is a distinct threshold voltage ($V_T$) increase caused by SRS. In the low gate bias region, the lateral displacement of the smooth and rough characteristics implies a $V_T$ increment of $\approx 30$ mV for the roughness parameters we used ($L_m=0.7$ nm and $r_m=0.14$ nm) and varies little from sample to sample. The increase in $V_T$ due to SRS was unexpected and the reason for it is as follows. Due to SRS, injections at low energies are blocked in the rough SNWT, which reduces the density-of-states (DOS) near the band edge (see the Fig. 3 inset). The lowered DOS near the band edge reduces the charge density in the subthreshold regime, and consequently increases $V_T$ in the rough SNWT. This effect would be modest in a conventional MOSFET with an energy-independent DOS above the band edge, but it becomes pronounced in a 1D wire with a singularity in the DOS at the band edge.

Finally, we explore the effects of SRS on the SNWT drain current above threshold. To do this, we compute a current ratio $\beta=I_{DS}^{\text{rough}}/I_{DS}^{\text{smooth}}$ at the same gate overdrive, $V_{GS}-V_T$, for both rough and smooth SNWTs. By comparing currents (rough versus smooth) at the same gate overdrive, the effect of the $V_T$ increasing induced by SRS is removed. This allows us to examine whether the roughness can cause a significant reduction of SNWT ON-current by backscattering. Figure 4 shows the $\beta$ vs gate overdrive curves for the SNWTs with different wire widths and roughness parameters. Several interesting phenomena are observed. First, all the simulated structures display a decreasing $\beta$ with an increasing gate overdrive. This occurs because more modes become conductive under higher gate bias, which, as described earlier, enhances SRS in the SNWTs.

Second, based on the roughness parameters we used, $L_m=0.7$ nm and $r_m=0.14$ nm, which are typical of an oxidized Si/SiO$_2$ interface, the SNWT with $W_{Si}=3$ nm (solid) achieves a surprisingly high $\beta=0.9$ at a typical ON-state condition (gate overdrive =0.3 V for a 0.4 V supplied voltage). The same amount of surface roughness scattering severely degrades the mobility of a planar MOSFET under a high gate bias. To explore the effects of $L_m$, two additional values (1.4 nm for circles and 3.0 nm for triangles) were examined. The results show that $\beta$ is insensitive to $L_m$, as expected from the averaging over a distribution of wavelengths that occurs at room temperature and high drain bias ($V_{DS}=0.4$ V). In contrast, doubling the rms (diamonds) clearly degrades $\beta$ at the same gate overdrive, indicating the importance of maintaining relatively smooth Si/SiO$_2$ interfaces for the high performance application of SNWTs.

Third, increasing the wire width reduces the strength of quantum confinement and thus increases the number of conducting modes in the SNWT. Our results (solid versus dashed) clearly show that with a larger number of conducting modes in the wider ($W_{Si}=9$ nm) SNWT, SRS is much stronger than in the narrower ($W_{Si}=3$ nm) device. This observation also suggests that SRS is more serious in a planar MOSFET, which can be viewed as a SNWT with a very large wire width.

In summary, we theoretically investigated SRS in SNWTs by using a full 3D, self-consistent, quantum mechanical simulator. The microscopic structure of the Si/SiO$_2$ interface roughness was implemented into the simulator using the 3D finite element method. We found that (1) SRS reduces the electron density of states in the channel, which increases the SNWT threshold voltage, and (2) SRS in SNWTs becomes less serious when fewer propagating modes conduct, implying that SRS will be less important in small-diameter SNWTs than in planar MOSFETs with many transverse modes occupied. This work provides important insights into the nature of SRS in SNWTs and suggests that SRS may not be as important in small-diameter nanowires as it is in conventional, planar MOSFETs.

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