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Physics of ultrathin-body silicon-on-insulator Schottky-barrier field-effect transistors

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ABSTRACT In this article we give an overview over the physical mechanisms involved in the electronic transport in ultrathin-body SOI Schottky-barrier MOSFETs. A strong impact of the SOI and gate oxide thickness on the transistor characteristics is found and explained using experimental as well as simulated data. We elaborate on the influence of scattering in the channel and show that for a significant barrier the on-state current is insensitive to scattering once the mean free path for scattering is larger than a characteristic length scale. In addition, recent efforts to lower the Schottky barrier at the source/drain channel interfaces are presented. Using dopant segregation during silicidation significantly lower effective Schottky barriers can be realized that allow for high performance SB-MOSFET devices.

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1 Introduction

Schottky barrier (SB) MOSFETs have recently attracted a renewed interest as an alternative to conventional MOSFETs with doped source and drain contacts [1–4]. This is due to the fact that in the near future the continued down-scaling of transistor dimensions calls for highly conductive source and drain electrodes since otherwise the current through the device will be limited by the contacts. In addition, very steep doping profiles are necessary in order to realize channel lengths in the sub-50 nm regime. SB-MOSFETs meet these requirements associated with source/drain engineering due to the replacement of the doped areas with metals. However, at the metallic source/drain-channel interfaces a Schottky barrier builds up and it was found that negative SB are required for an SB-MOSFET to exhibit the same performance as a conventional field-effect transistor [5]. In experimental devices on the other hand, positive SB are found that reduce the carrier injection into the channel. As a result, SB-MOSFETs show an inferior off-state with inverse subthreshold slopes significantly exceeding 60 mV/dec and lower on-currents if compared to conventional devices [6, 7]. It is therefore desirable to achieve Schottky barriers as low as possible and render the tunneling probability through the barrier as large as possible.

In the present paper we elaborate on the physics of current transport in ultrathin-body (UTB) silicon-on-insulator (SOI) Schottky barrier MOSFETs. Experimental and simulation results related to the injection of carriers through the SB and to the dependence on scattering in the channel are presented. It is shown that decreasing the SOI and gate oxide thicknesses leads to an increased screening of the potential inside the channel which in turn yields highly transparent Schottky barriers. In addition, we discuss the use of dopant segregation during silicidation that enables the formation of thin, highly doped layers at the contact–channel interfaces again strongly increasing the carrier injection through the Schottky barriers. As a result, high-performance SB-MOSFETs become feasible.

2 Ultrathin-body SOI SB-MOSFETs

Figure 1 shows a cross-section of the device geometry under consideration. A thin SOI film of thickness d_{soi} serves as the channel of length L and width W which is connected to metallic source and drain contacts. A gate oxide of thickness d_{ox} separates the channel from the gate electrode. The lower part of Fig. 1 shows the conduction and valence bands along current transport direction at the interface between gate oxide and channel. A Schottky barrier of height Φ_{SB} builds up at the source/drain–channel interfaces such that for a certain gate voltage V_{gs} and drain-source voltage V_{ds} the bands in the channel look qualitatively as depicted.

Figure 2 shows experimental transfer characteristics of a SB-MOSFET with nickel silicide source/drain contacts [8]. An ambipolar behavior, typical of SB-MOSFETs, can be seen with an inverse subthreshold slope $S = 250$ mV/dec in the electron branch, far in excess of the thermal limit of $S = 60$ mV/dec. Two different inverse subthreshold slopes can be identified in the hole branch indicating that the Fermi level is pinned more closely to the valence band thus leading to a thermal emission dominated region within a small gate voltage range. The inset shows the conduction and valence bands for three different gate voltages indicated with the symbols \circ , \square and \times . Between gate voltages belonging to the bands \times and \square , electron injection is suppressed and the injection of holes is mediated by thermal emission leading to the small S seen in the experimental data. For more negative and more positive gate voltages, the injection of carriers is determined by the change of the tunneling probability through the SB

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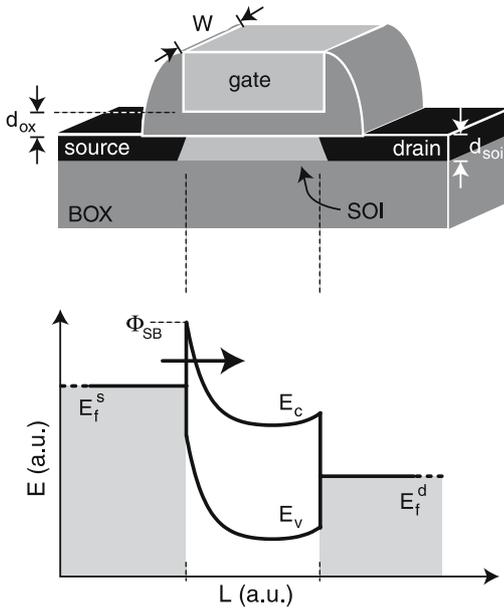


FIGURE 1 Schematics of an SOI Schottky-barrier MOSFET. The lower part shows the conduction and valence bands in the channel along current transport direction for positive bias and V_{gs}

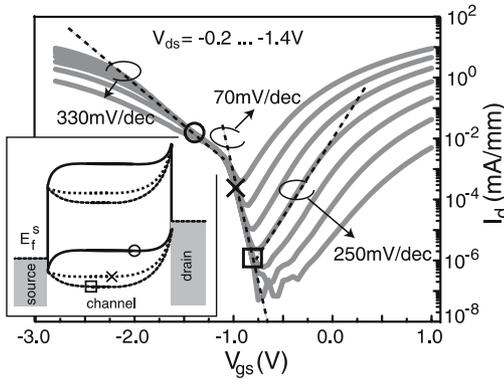


FIGURE 2 Experimental transfer characteristics of an SB-MOSFET with $d_{ox} = 3.5$ nm and $d_{soi} = 25$ nm; the width $W = 40$ μm and the channel length $L = 2$ μm . The inset shows band profiles for three different gate voltages as indicated in the figure

with altering V_{gs} [6]. As a result, SB-MOSFETs exhibit inverse subthreshold slopes larger than 60 mV/dec and lower on-currents if compared to conventional devices with doped source/drain contacts.

3 Simulation results

In order to gain a better understanding of the current transport mechanisms that determine the behavior of Schottky-barrier MOSFETs we have performed simulation as well as analytical studies of such devices. A proper simulation requires a two-dimensional solution of the Poisson and Schrödinger equation. However, it has been shown that the electrostatics of fully-depleted SOI devices is well captured by a modified, one-dimensional Poisson equation [9, 10]. This equation is given by

$$\frac{d^2\phi_f}{dx^2} - \frac{\phi_f - \phi_g + \phi_{bi}}{\lambda^2} = \frac{e(\rho(x) \pm N)}{\epsilon_0\epsilon_{si}}, \quad (1)$$

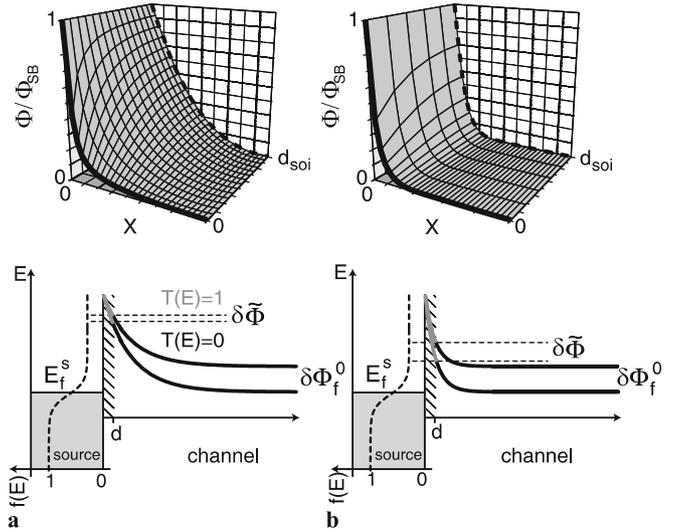


FIGURE 3 Two-dimensional potential distribution of the source Schottky diode for (a) a thick and (b) a thin SOI film but the same d_{ox} . The lower part shows the conduction band profile at the source contact again for a thin and a thick SOI film for two different gate voltages. For the analytical approximation the tunneling probability $T(E) = 1$ for energies above $\tilde{\phi}$ and zero otherwise

where Φ_f , Φ_g and Φ_{bi} are the surface potential, the gate potential and the built-in potential, respectively; $\lambda = \sqrt{\frac{\epsilon_{si}}{\eta\epsilon_{ox}}d_{ox}d_{si}}$ where $\eta \approx 1.3$ accounts for the non-uniformity of the lateral field across the SOI thickness [11]. Furthermore, $\rho(x)$ is the density of free carriers and N represents the density of fully ionized dopants.

Equation (1) allows easy access to a number of insights into the SB-MOSFET device characteristics. For instance, considering the limit $\rho \approx 0$ which corresponds to the transistor's off-state, (1) can be solved analytically leading to a solution of the form $\Phi_f(x) \propto \exp(-x/\lambda)$. This means that λ determines the length scale on which potential variations are being screened. The screening becomes more effective if devices exhibit ultrathin bodies d_{soi} and ultrathin gate oxides d_{ox} . In particular, (1) predicts that the Schottky barriers can be made thin if λ is made small yielding an increased tunneling probability through the SB. The upper part of Fig. 3 shows the two-dimensional potential distribution of the source Schottky diode for (a) a thick SOI film and (b) for a thin d_{soi} but the same gate oxide thickness [6]. It is apparent that in case of the thin SOI film, the field situation at the buried oxide-channel interface extends over the entire thickness of the SOI and thus leads to a thinner Schottky-barrier. The same is true if d_{ox} is made smaller (not shown here, see [6]). This means that the one-dimensional, modified Poisson equation captures the impact of the SOI and gate oxide thickness on the potential distribution in the channel of SOI SB-MOSFETs. Throughout the paper, the theoretical analysis is based upon (1).

3.1 Analytical approximations

Analytical expressions for the current in the off-state and hence for the inverse subthreshold slope S of SOI SB-MOSFETs can be derived by replacing the real potential distribution of the source Schottky diode with an effective potential barrier $\tilde{\phi}$ for thermal emission alone. This means the

tunneling probability is set to $T(E) = 1$ above $\tilde{\Phi}$ and zero below as illustrated in the lower part of Fig. 3. In other words we define a tunneling distance d such that if the potential barrier is larger than d , $T(E)$ is set to zero. An estimation for d can be obtained if the Schottky barrier is approximated with a triangularly shaped potential of height Φ_{SB} and width λ . Using the transmission probability calculated with the WKB approximation, an expression for d can be calculated that shows a weak dependence on Φ_{SB} as well as d_{soi} and d_{ox} . Therefore, assuming d to be constant, Fig. 3 reveals that the current on the transistor's off-state will strongly depend on λ . In particular, the inverse subthreshold slope will depend on λ since a smaller λ leads to a better gate control of the effective barrier $\tilde{\Phi}$ as becomes apparent when comparing the lower parts of Fig. 3a and b. To be specific, since in the off-state the density of mobile carriers is small, i.e. $q \approx 0$ the Poisson equation (1) can be solved analytically as was already mentioned above leading to $\tilde{\Phi} = \Phi_f(d) = (\Phi_{\text{SB}} - \Phi_f^0) \exp(-d/\lambda) + \Phi_f^0$ for a given d where $\Phi_f^0 = \Phi_g + \Phi_{\text{bi}}$ is the surface potential in the channel several λ away from the contact interface (see Fig. 3). Then, for large V_{ds} and $\tilde{\Phi} > k_B T$ the current in the off-state is proportional to $I_d \propto \exp\left(-\frac{\tilde{\Phi} - E_f^s}{k_B T}\right)$ and with $S = \ln(10) \left(\frac{\partial I_d}{\partial \tilde{\Phi}} \frac{\partial \tilde{\Phi}}{\partial V_{\text{gs}}} \frac{1}{I_d}\right)^{-1}$ a closed expression for S is obtained. Since in general $\lambda > d$ the result can be expanded leading to:

$$S = \frac{k_B T}{q} \ln(10) \frac{1}{1 - \exp(-d/\lambda)} \approx \frac{k_B T}{q} \ln(10) \left(\frac{1}{2} + \frac{\lambda}{d}\right). \quad (2)$$

Equation (2) means that in an SOI SB-MOSFET, even in the long channel case, S scales as the square-root of the SOI and the oxide thickness. Hence UTB SOI and ultrathin gate oxides are beneficial for the performance of SB-MOSFETs as we will see below.

3.2 Simulation approach

Next, we want to investigate the on-state of SB-MOSFETs. To this end, a numerical computation of the current through the device is necessary. For the calculation of the charge in and current through the transistor we employ the non-equilibrium Greens function formalism. Together with the modified Poisson equation (1) our model allows the self-consistent calculation of the electronic transport in SOI SB-MOSFETs.

To numerically compute the Greens functions we make use of Datta's approach [12]. We consider a one-dimensional finite difference scheme with lattice constant a and nearest neighbor hopping parameter t as illustrated in Fig. 4. A quadratic dispersion relation in the conduction and valence band is used. In order to describe the complex band structure in the band gap we make use of Flietner's dispersion relation [13]. Because UTB SOI is considered, we assume that the first subband contributes most to the current and hence the expressions for charge and current are averaged over the direction of W only (see [14] for details). Higher subbands are accounted for by a numerical factor as in [15].

Scattering is taken into account by attaching Buettiker probes via appropriate self-energy functions to each site of

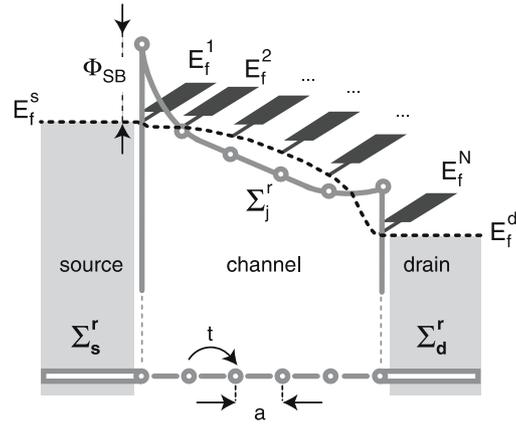


FIGURE 4 Incorporation of scattering by attaching floating Buettiker probes at each grid point. The resulting Fermi levels in the probes constitute the quasi-Fermi-level distribution along the current transport direction. The lower part shows the finite difference grid with lattice spacing a and nearest neighbor hopping

the finite difference grid [16] which is also shown in Fig. 4. Each Buettiker probe has its own Fermi level E_f^j such that the dotted line in Fig. 4 represents the position-dependent quasi-Fermi level in the channel. The Fermi energies of the Buettiker probes are not fixed by a certain terminal voltage but individually float to values such that the total current flowing into and out of each Buettiker probe sums up to zero. During the self-consistent calculations the appropriate Fermi energies in the probes are found by an iterative procedure [16]. Since carriers can enter one probe at a particular energy and leave it at another energy each Buettiker probe represents a dissipative scattering site whose effectiveness is mediated by the coupling γ of the probe to the channel. As was shown by Venugopal (see appendix of [16]) one can associate the mean free path of carriers in the channel l_{scat} with the parameter γ : $l_{\text{scat}} = 2a \times 1/\gamma$. This means, if γ is large, i.e. if the Buettiker probe is tightly bound to the channel, the mean distance between scattering becomes short and vice versa. After self-consistency between the Poisson equation and the equations for the Greens functions, including scattering, is achieved, the current flowing from source to drain is computed as follows [16]

$$I_d = M_e \frac{2e}{h} W \int dE \sum_j T^{d,j}(E) \left[f(E - E_f^d) - f(E - E_f^j) \right], \quad (3)$$

where M_e accounts for the degeneracy of the conduction/valence band and also includes the estimation of the contribution of higher subbands [15]. Note that the transmission coefficient T has been averaged over the direction of the width W of the device [14].

3.3 Simulation results

Figure 5a shows simulated data points for S as well as results from the analytical calculation for devices with $d_{\text{ox}} = 3.5$ nm (light gray stars and dashed line), $d_{\text{ox}} = 1.5$ nm (black squares and straight line) and $d_{\text{ox}} = 0.5$ nm (gray circles and dashed line). In the present case, a SB of $\Phi_{\text{SB}} =$

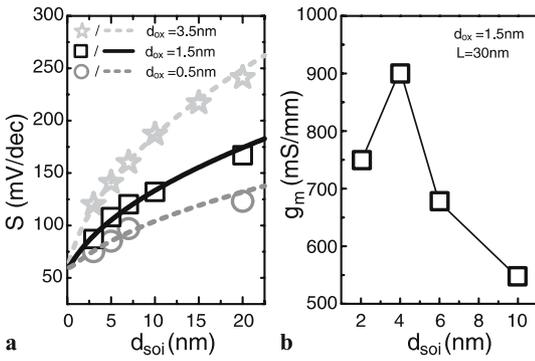


FIGURE 5 (a) S versus SOI thickness extracted from simulations for devices with $d_{\text{ox}} = 3.5$ nm (light gray stars), $d_{\text{ox}} = 1.5$ nm (black squares) and $d_{\text{ox}} = 0.5$ nm (gray circles). The corresponding results of the analytical approximation are shown as well. (b) g_m at $V_{\text{gs}} - V_{\text{th}} = 0.75$ V versus d_{soi} for a device with $d_{\text{ox}} = 1.5$ nm, $L = 30$ nm and $\Phi_{\text{SB}} = 0.28$ eV

0.64 eV as appropriate for NiSi and ballistic transport were assumed. The assumption of ballistic transport, however, is irrelevant for the extraction of S . Since the tunneling distance d is not exactly known it was chosen as a constant fit parameter in order to get the best agreement with the simulated (and experimental data, see Sect. 4.2) data. For all three different gate oxide thicknesses best results were obtained with $d = 3.7$ nm, consistent with the range calculated from a WKB approximation [7]. The excellent agreement between analytical results and simulated data is obvious, showing that the analytical approximation describes the dependence of S on d_{soi} and d_{ox} in SOI SB-MOSFETs very well. Since λ is approximately proportional to $\sqrt{d_{\text{soi}}d_{\text{ox}}}$ this gives rise to the strong square-root dependence of S on d_{soi} as seen in Fig. 5a.

This has the important implication that devices with rather thick oxides can still exhibit steep inverse subthreshold slopes if the body is scaled to an extremely small thickness, such as in a nanowire or nanotube. In fact, carbon nanotube FETs – a special case of UTB SB-MOSFETs – show an excellent off-state even in the case of a rather thick d_{ox} (see e.g. [17]). However, in the case of a rather large gate oxide, S depends sensitively on the exact body thickness. In addition, the confinement of carriers in the SOI film due to vertical quantization leads to an energetic separation of the first subband from the bottom of the conduction/valence band in UTB SOI. As a result, devices with a larger gate oxide and UTB SOI exhibit a non-monotonic dependence of the threshold voltage on d_{soi} as has been discussed in detail in [7]. Hence, small body thickness fluctuations may lead to significant V_{th} -shifts. It is therefore desirable to make d_{ox} as small as possible even in long-channel devices in contrast to conventional MOSFETs where to first order d_{ox} should be as large as possible, while still avoiding short channel effects.

Figure 5b shows simulated transconductances g_m of a SB-MOSFET with a channel length of $L = 30$ nm and $d_{\text{ox}} = 1.5$ nm [6]. In the present case a Schottky-barrier height of $\Phi_{\text{SB}} = 0.28$ eV was assumed as appropriate for e.g. ErSi source/drain contacts [4]. Again, a ballistic simulation is used in order to give an upper estimation of possible device performance. It can be seen, that g_m strongly depends on d_{soi} and increases as the SOI thickness is scaled down to 4 nm. This is expected since a smaller body thickness yields a thinner SB

and hence implies an increased carrier injection. Only for SOI thicknesses below 4 nm, g_m drops again, although the inverse subthreshold slope still gets improved. The reason for this was already mentioned above: for such small SOI films vertical quantization leads to an increase of the SB height. Whereas for S the exact barrier height is irrelevant as long as Φ_{SB} is significantly larger than $k_B T$ the on-state as measured by g_m sensitively depends on the exact barrier height. In other words, for the on-state the benefit of a thinner SB is overcompensated by the increase of the SB height, if $d_{\text{soi}} \lesssim 4$ nm.

Next, we study the impact of scattering on the on-state performance of SB-MOSFETs using the Buettiker-probe approach presented in the last section. Devices with a $\Phi_{\text{SB}} = 0.5$ eV and $\Phi_{\text{SB}} = 0$ eV exhibiting different channel lengths L and scattering mean free paths l_{scat} are simulated. If not stated otherwise, $d_{\text{soi}} = 5$ nm and $d_{\text{ox}} = 1$ nm in all cases. Figure 6a shows results for a constant channel length of $L = 25$ nm. The solid circles belong to devices with $\Phi_{\text{SB}} = 0.5$ eV, the hollow squares belong to devices with $\Phi_{\text{SB}} = 0$ eV. It can be seen that in both cases the on-current rises and then saturates for $l_{\text{scat}} > 4$ nm. This can be understood within the framework of the so-called $k_B T$ -layer concept [18]. Under quasi-ballistic transport conditions, the probability for backscattering is approximately $r \approx \frac{L_{\text{kT}}}{L_{\text{kT}} + l_{\text{scat}}}$ where L_{kT} is the length over which the channel potential has dropped by $k_B T/q$. However, in the present case the characteristic length scale over which the potential varies is λ . Since for the given d_{soi} and d_{ox} $\lambda \approx 3.8$ nm, Fig. 6a suggests that in the case of SB-MOSFETs in the quasi-ballistic regime $r \approx \frac{\lambda}{\lambda + l_{\text{scat}}}$. A more detailed an-

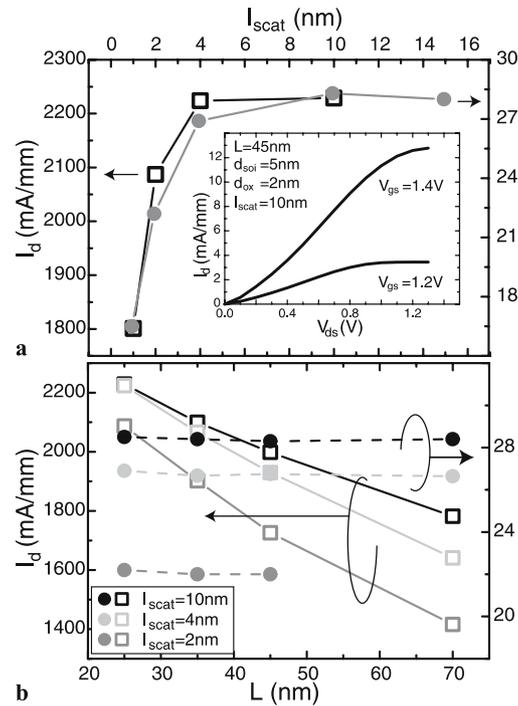


FIGURE 6 (a) Simulated on-currents for SB-MOSFETs with $\Phi_{\text{SB}} = 0.5$ eV (solid circles) and $\Phi_{\text{SB}} = 0$ eV (hollow squares). The inset shows a typical output characteristic exhibiting the typical S-shaped curve for low V_{ds} . (b) Simulated on-currents for $l_{\text{scat}} = 2$ nm, 4 nm and 10 nm for different channel lengths; $V_{\text{ds}} = 1.3$ V and $V_{\text{gs}} = 1.2$ V in all cases if not stated otherwise

alysis of the interplay between d_{ox} , d_{soi} , the SB height and scattering will be published elsewhere. Looking at Fig. 6b one observes a clear dependence of the on-current on the channel length for the devices with $\Phi_{\text{SB}} = 0 \text{ eV}$. Here the on-currents as calculated for devices with $l_{\text{scat}} = 2 \text{ nm}$ (gray hollow squares), $l_{\text{scat}} = 4 \text{ nm}$ (light gray hollow squares) and $l_{\text{scat}} = 10 \text{ nm}$ (black hollow squares) are plotted. Increasing L decreases the on-current in all three cases. In contrast, for the devices with $\Phi_{\text{SB}} = 0.5 \text{ eV}$ and the same different l_{scat} (solid circles) the channel length is irrelevant (for the channel lengths considered here). What limits the on-current is only scattering that occurs within the characteristic length scale λ at the source-channel interface, i.e. within the spatial region where the carrier injection occurs. In other words, for an SB of 0.5 eV, even for a thin gate oxide of 1 nm and a $d_{\text{soi}} = 5 \text{ nm}$ the Schottky barrier is the main scattering event rendering the mobility of the channel material irrelevant in this case.

4 Experimental results

In the following we present experimental results on the impact of the SOI film and gate oxide thickness on the injection of carriers in SB-MOSFETs. In addition, the use of dopant segregation during silicidation is introduced that allows strong improvement of the performance of SOI SB-MOSFETs with fully nickel silicided source/drain electrodes.

4.1 Device fabrication

Commercially available 4" SOI wafers with a p -type doping of $1 \times 10^{15} \text{ cm}^{-3}$ are used as the starting material to fabricate devices with different SOI film and gate oxide thicknesses. Body thicknesses in the range of 7–55 nm are realized by a cycle of dry/wet oxidation and subsequent HF-stripping. In addition, a modified standard clean (1 : 8 : 64 = $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ at 65 °C for 10 min) followed by diluted HF-stripping is used several times [19] in order to get a well controlled d_{soi} . After a standard mesa isolation and RCA cleaning, gate oxides in the range of 3.5 nm–24 nm are grown. Subsequently, 200 nm n -type poly-Si and 50 nm SiO_2 are deposited by LPCVD. The SiO_2 on top of the poly-Si is patterned with optical lithography, followed by reactive ion etching (RIE). Samples with $d_{\text{soi}} = 25 \text{ nm}$ and $d_{\text{ox}} = 3.5 \text{ nm}$ are implanted with arsenic at a dose of $5 \times 10^{14} \text{ cm}^{-2}$ and an energy of 5 keV and are called hereafter ‘segregation devices’. The other samples are left without any implantation. Figure 7a and b show a schematic illustration of the fabrication process. Note that only in case of the segregation devices, ion implantation is used. Next, gate spacers are formed and nickel is deposited. For the subsequent silicidation step, a temperature of 450 °C and a time of 20 s was chosen in order to facilitate the occurrence of dopant segregation and the encroachment of NiSi into the channel region as depicted in Fig. 7b. This ensures that there is no void between the contact and the beginning of the gate area. The unreacted nickel is selectively removed using Piranha. Figure 7c shows a cross-sectional TEM image. One can clearly see the NiSi encroachment underneath the spacer ensuring a good electrostatic control over the potential distribution at the Schottky contacts.

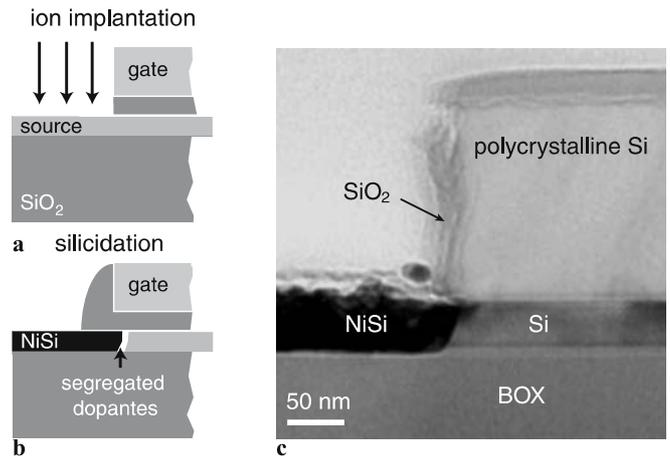


FIGURE 7 Schematics of the SB-MOSFET fabrication. (a) As implantation into the contact regions, (b) spacer formation and silicidation. (c) TEM image of a readily processed device

4.2 Dependence on gate oxide and SOI body thickness

Figure 8 shows typical transfer characteristics of devices with different gate oxide (a) and body thicknesses (b). Both the off-state in terms of the subthreshold swing (extracted as indicated by the dashed lines in Fig. 8a and b) as well as the on-state current are strongly improved on decreasing d_{ox} . An improvement of S and the on-state is also seen for decreasing SOI thickness as expected from the simulations presented in Sect. 3.3. However, the on-state does not provide a good measure to quantify the impact of d_{ox} and d_{soi} on the electrical behavior of the devices since it sensitively depends on source/drain series resistances and the ex-

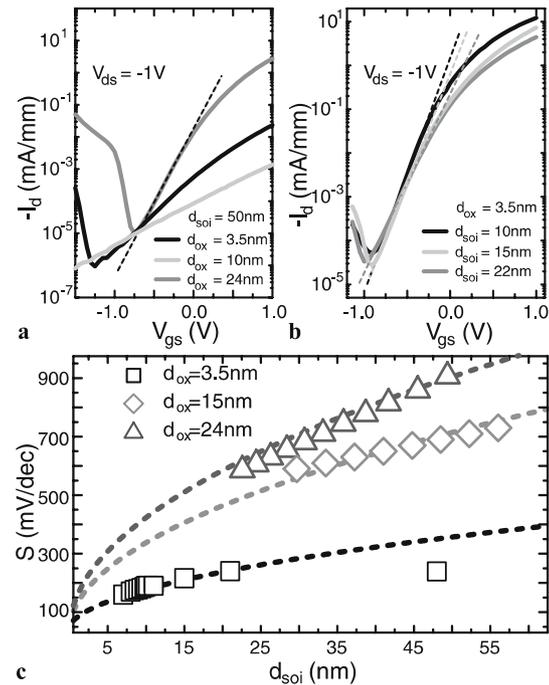


FIGURE 8 Transfer characteristics of SB devices with (a) different d_{ox} and (b) varying d_{soi} . Decreasing d_{ox} and/or d_{soi} improves both, the on-current as well as the inverse subthreshold slope. (c) S versus d_{soi} for different d_{ox} . The dotted lines belong to the analytical approximation presented above

act SB height, as we have seen above. The subthreshold swing is insensitive to process-induced variations and source/drain resistances: if I_d is subdivided into a thermionic I_{th} and tunneling contribution I_T , the subthreshold swing can be written as $S = \ln(10) \times ((\partial I_{th}/\partial V_{gs} + \partial I_T/\partial V_{gs}) \times (1/I_{th} + 1/I_T))^{-1}$. Since NiSi has a SB of $\Phi_{SB} = 0.64$ eV, much larger than $k_B T$, the terms related to I_{th} can be neglected and hence S is exclusively determined by the change of the tunneling probability through the SB with changing V_{gs} . Note, that this also renders S insensitive to process-induced changes of the actual SB height which is reflected by the fact that the extracted S values of different devices having the same d_{ox} and d_{soi} are nearly identical although they exhibit a different on-state current.

In order to investigate the influence of d_{soi} and d_{ox} on the carrier injection in more detail, devices with SOI thicknesses in the range between 7 nm and 55 nm on different sample chips exhibiting three different gate oxide thicknesses are measured and S is extracted. Figure 8c summarizes the dependence of S on d_{soi} for devices with $d_{ox} = 3.5$ nm, 15 nm and 24 nm, respectively. In the case of the device with $d_{ox} = 3.5$ nm and $d_{soi} \leq 22$ nm, S decreases with decreasing SOI thickness. However, for $d_{soi} > 22$ nm the inverse subthreshold slope saturates at a value independent of d_{soi} . However, for larger d_{ox} , S shows an increasing dependence on d_{soi} . The dotted lines in Fig. 8c belong to calculated S values based upon the analytical computation of S given above. The analytical and the experimental results deviate from each other only in the case of $d_{ox} = 3.5$ nm and $d_{soi} > 22$ nm. In all other cases an excellent agreement is found reconfirming that for decreasing SOI and gate oxide thickness an improved carrier injection is indeed obtained.

The reason why for large SOI thicknesses and small d_{ox} , S only weakly depends or even becomes independent of d_{soi} is that for a thin gate oxide the impact of the electric field at the BOX on the potential distribution of the SB becomes less and less important for increasing SOI body thickness and the electric field at the gate oxide mainly determines the potential landscape. On the other hand, if the device exhibits a thicker gate oxide, the influence of the gate oxide on the SB is diminished such that even in the case of larger d_{soi} the BOX influences the potential distribution of the SB and hence the carrier injection through the SB. As a result, SOI SB-MOSFETs show an improvement of the carrier injection if $d_{soi} \leq 6 - 7 \times d_{ox}$.

4.3 Effective Schottky-barrier height lowering using dopant segregation

The use of ultrathin SOI and gate oxides allows improvement of the carrier injection in SB-MOSFETs. Another way to do this is to highly dope the semiconductor in contact with the metal [8, 20]. However, as can be inferred from (1), as long as the SOI is fully depleted, doping the channel only results in a shift of the threshold voltage but the potential distribution is still determined by λ , i.e. the carrier injection is unaffected by doping the channel. What is needed is a non-uniform doping profile with a highly doped layer only at the source/drain-channel interfaces. Such a non-uniform doping profile can be generated

by dopant segregation (DS) during silicidation. During the silicidation step, the dopants are found to redistribute between the silicide and the silicon which affects the electrical properties of the resulting Schottky contact [21]. In order to investigate the effect of dopant segregation in more detail, arsenic is implanted into the source and drain areas (see above) and the contacts are fully nickel silicided. The segregation of arsenic at the silicide-silicon interface has been confirmed by bulk-silicon test samples using secondary ion mass spectroscopy and it was found that dopant concentrations larger than $1 \times 10^{26} \text{ m}^{-3}$ can be obtained for an initial implantation dose $\geq 5 \times 10^{14} \text{ cm}^{-2}$ [8].

Transfer characteristics of SB-MOSFETs with dopant segregation are shown in the main panel of Fig. 9. The device exhibits asymmetric ambipolar conduction with the hole branch being suppressed (compare with Fig. 2) and the device behaves like an n -type transistor. The most prominent feature of the transfer characteristics, however, is that the inverse subthreshold slope of the n -branch is $S = 70 \text{ mV/dec}$, close to the thermal limit. This means that the device behaves like a “bulk-switching”, conventional MOSFET, where thermionic emission of carriers over the source bulk potential barrier in the channel is responsible for the current flow instead of tunneling through a SB. The reason for this is a strongly decreased effective SB height due to the highly doped area at the silicide-silicon interface [22]. The highly doped layer leads to a strong band bending at the interface. If the dopant concentration is high enough the SB becomes so transparent that the effective Schottky barrier $\bar{\Phi}$ introduced in Sect. 3.1 is smaller than the bulk potential Φ_f^0 in the channel over a large gate voltage range (the V_{gs} -range indicated in the inset of Fig. 9 with \circ and \times). In this case an ideal off-state and improved on-state can be expected as is actually observed experimentally. The on-state current is determined by the effective Schottky barrier $\Phi_{SB}^{eff} = \bar{\Phi}$ which should certainly be as small as possible. Temperature dependent measurements of the I - V -characteristics revealed that $\Phi_{SB}^{eff} \approx 0.1$ eV, significantly smaller than the original SB height of NiSi of 0.64 eV for electron injection [23]. Hence, dopant segregation is a very effective means to drastically increase the carrier injection and therefore improve the device characteristics of SB-MOSFETs.

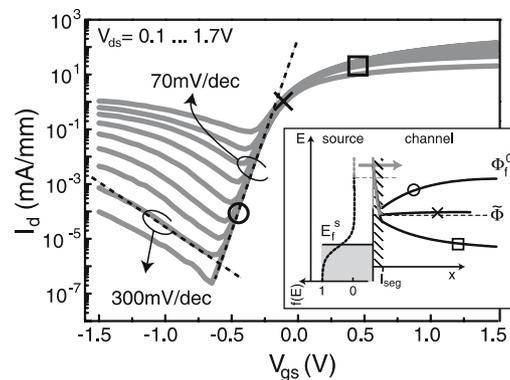


FIGURE 9 Transfer characteristics of a SB-MOSFET with DS. The inset shows the conduction band at the source Schottky diode. The highly doped segregation layer leads to a strong band bending yielding a low effective SB $\bar{\Phi}$, smaller than the bulk potential Φ_f^0 over a large V_{gs} -range

4.4 Scaling issues of SB-MOSFETs with dopant segregation

The formation of a highly doped interface layer allows strong decreasing of the effective SB. However, the important thing here is that the segregation layer has a small spatial extend and that the dopant concentration rapidly falls off away from the contact electrode–channel interface since otherwise the particular benefits of the SB-MOSFET architecture are lost. The inset of Fig. 10 shows a schematic of the device cross section together with the dopant concentration on a logarithmic scale. A concentration N_{seg} within the segregation layer of extend l_{seg} is assumed. Towards the middle of the channel the dopant concentration falls off on a length scale ζ given in nm/dec.

We have simulated SB-MOSFETs exhibiting such a doping profile and have varied the channel length. To be specific, devices with $N_{\text{seg}} = 1 \times 10^{26} \text{ m}^{-3}$, $l_{\text{seg}} = 2 \text{ nm}$, $d_{\text{soi}} = 5 \text{ nm}$ and $d_{\text{ox}} = 1 \text{ nm}$ have been simulated. A rather large $\zeta = 18 \text{ nm/dec}$ is assumed in order to clearly show the effect of a long dopant tail without being masked by the onset of short channel effects. The main panel of Fig. 10 shows transfer characteristics for segregation devices with $L = 28 \text{ nm}$ (black line), $L = 31 \text{ nm}$ (light gray line) and $L = 38 \text{ nm}$ (gray line). The dotted black line belongs to an SB-MOSFET with $L = 28 \text{ nm}$ but without dopant segregation. One can clearly see that with decreasing channel length, the curves are shifted towards more negative gate voltages. The reason for this is that the dopant tails of the source and drain segregation layers overlap and constitute a dopant density in the channel that leads to a shift of the threshold voltage like in a conventional device [24]. Looking more closely at the transfer characteristics it becomes apparent that besides a V_{th} -shift the inverse subthreshold slope increases with decreasing channel length. For the longest devices an almost ideal S -value is found, as expected in a segregation device. However, the shortest device

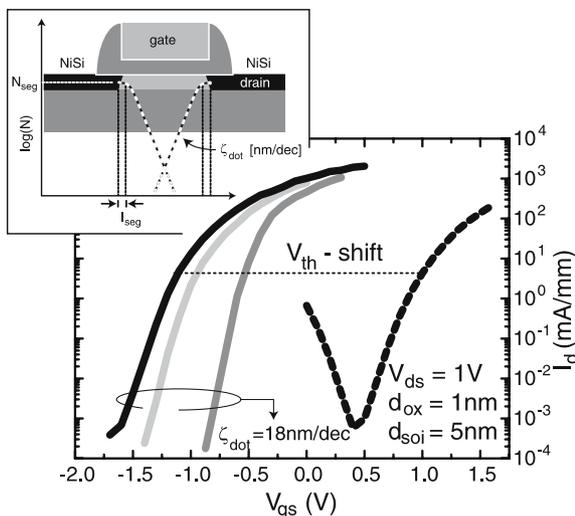


FIGURE 10 Transfer characteristics of SB-MOSFETs with dopant segregation and $L = 28 \text{ nm}$ (black), $L = 31 \text{ nm}$ (light gray) and $L = 38 \text{ nm}$ (gray); $\zeta_{\text{dop}} = 18 \text{ nm/dec}$. The black dotted line belongs to a device without dopant segregation and $L = 28 \text{ nm}$

exhibits the same subthreshold swing as the SB-MOSFET without dopant segregation (black dotted line). As has already been mentioned, in the case of the shortest channel the dopant concentration appears to be almost constant and thus only leads to a V_{th} -shift, whereas the potential profile of the barrier is determined by the screening length λ . In this case dopant segregation does not improve the injection of carriers. In turn this means that in SB-MOSFETs with dopant segregation steep doping profiles are required for ultimately scaled devices.

5 Conclusion

In conclusion, we studied the electronic transport in ultrathin-body SOI SB-MOSFETs. Simulation as well as experimental results on the dependence of the electrical characteristics on the SOI and gate oxide thicknesses show that an improved switching behavior for either ultrathin gate oxides and/or ultrathin SOI bodies is obtained. Furthermore, if a significant Schottky barrier is present at the contact–channel interfaces the resulting on-current is largely independent of scattering once the mean free path is larger than the characteristic length scale λ . We also studied the impact of dopant segregation during silicidation on the performance of SB-MOSFETs and found an almost ideal off-state and strongly improved on-state in segregation devices.

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