

3-1-2007

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Zhang, M; Knoch, Joachim; Appenzeller, Joerg; and Mantl, S, "Improved carrier injection in ultrathin-body SOI Schottky-barrier MOSFETs" (2007). *Other Nanotechnology Publications*. Paper 166.  
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# Improved Carrier Injection in Ultrathin-Body SOI Schottky-Barrier MOSFETs

M. Zhang, J. Knoch, Joerg Appenzeller, *Senior Member, IEEE*, and S. Mantl

**Abstract**—The impact of the gate oxide and the silicon-on-insulator (SOI) body thickness on the electrical performance of SOI Schottky-barrier (SB) MOSFETs with fully nickel silicided source and drain contacts is experimentally investigated. The subthreshold swing  $S$  is extracted from the experimental data and serves as a measure for the carrier injection through the SBs. It is shown that decreasing the gate oxide and body thickness allows to strongly increase the carrier injection and hence, a significantly improved ON-state of SB-MOSFETs can be obtained.

**Index Terms**—Carrier injection, Schottky-barrier (SB)-MOSFET, ultrathin-body silicon-on-insulator (SOI).

SCHOTTKY-BARRIER (SB) MOSFETs have recently received an increasing attention because of their inherent advantages associated with source/drain engineering [1]–[3]. However, it is known that a negative SB is needed for an SB-MOSFET to exhibit the same performance as a conventional-type device [4]. On the other hand, positive SB heights are present in experimental devices yielding a significantly degraded ON- and OFF-state of SB-MOSFETs. Hence, improving the carrier injection in SB-MOSFETs is indispensable to further improve their electrical performance. In a recent simulation study, we found that the SB can be made very thin, i.e., the carrier injection is significantly improved, if devices are based on ultrathin body (UTB) silicon-on-insulator (SOI) [5]. The reason for the improvement is the electric field situation at the buried oxide (BOX)-channel interface that leads to an exponential dependence of the potential distribution at the contact interfaces inside the channel region. In turn, the improved carrier injection leads to devices with steeper subthreshold swings and higher transconductances. In this letter, we experimentally study the impact of the channel thickness ( $t_{\text{si}}$ ) and the gate oxide thickness ( $t_{\text{ox}}$ ) on the electrical characteristics of fully nickel silicided source/drain SOI SB-MOSFETs. Although NiSi is not preferable for real applications due to its high SB, it allows to use the subthreshold swing as a measure to quantify the carrier injection independent of process variations as will be discussed in detail below. Furthermore, we compare

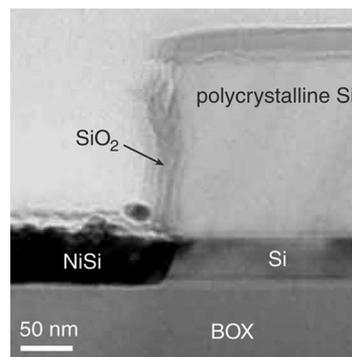


Fig. 1. Cross-sectional TEM image of a readily fabricated SB-MOSFET on 50-nm SOI. The image shows that the silicide/Si interface is directly underneath the gate.

the experimental data with an analytical approximation that confirms our interpretation of an improved device performance due to the use of UTB SOI and ultrathin gate oxides.

SB-MOSFET devices were fabricated on weakly doped ( $10^{15} \text{ cm}^{-3}$ ),  $p$ -type  $\langle 100 \rangle$  SOI wafers with an initial thickness of 100 nm. In order to investigate the impact of  $t_{\text{si}}$  and  $t_{\text{ox}}$  on the transistor performance, we prepared two series of devices: The first all have a  $t_{\text{ox}} = 3.5 \text{ nm}$  but different  $t_{\text{si}}$ .<sup>1</sup> Body thicknesses in the range of 7–55 nm are realized by a cycle of dry/wet oxidation and subsequent HF stripping. In addition, a modified standard clean (1 : 8 : 64 =  $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$  at 65 °C for 10 min) followed by diluted HF stripping is used several times [6] in order to get a well controlled  $t_{\text{si}}$ . Devices of the second series have different  $t_{\text{ox}}$  grown by wet thermal oxidation [7] (using different temperatures and time) on SOI wafers with an initial silicon thickness of  $\sim 50$ –60 nm. Immediately after the gate oxide formation, 200-nm  $n$ -doped polycrystalline silicon and 50-nm  $\text{SiO}_2$  are deposited by low-pressure chemical vapor deposition and subsequently patterned by reactive ion etching. After sidewall spacer formation and a diluted HF dip, nickel is deposited by e-beam evaporation and annealed. The unreacted nickel is removed with a mixture of  $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2 = 2 : 1$ . Only long-channel devices with a channel length of 2  $\mu\text{m}$  and a width of 40  $\mu\text{m}$  were fabricated to exclude any influence of the drain field on the source Schottky diode, i.e., to exclude short channel effects for all body and gate oxide thicknesses. Fig. 1 shows a transmission electron microscope (TEM) cross section of a readily fabricated device. Source and drain are fully

Manuscript received November 15, 2006; revised December 19, 2006. The review of this letter was arranged by Editor M. Ostling.

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Digital Object Identifier 10.1109/LED.2007.891258

<sup>1</sup>The rather thick oxide was chosen to suppress gate leakage in the present long channel devices.

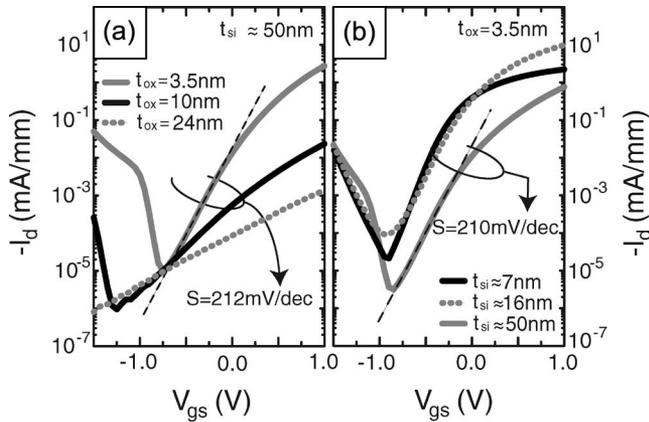


Fig. 2. Transfer characteristics of SOI SB-MOSFETs with (a) different gate oxide thicknesses on thick SOI. (b) Shows devices with different SOI body thicknesses but the same  $t_{ox}$ .  $V_{ds} = -1$  V in all cases.

silicided and the silicide/Si interface is directly underneath the gate which ensures a good electrostatic control of the Schottky contact.

Fig. 2 shows typical transfer characteristics of devices with different 1) gate oxide and 2) body thicknesses. Both the OFF-state in terms of the subthreshold swing (extracted as indicated in Fig. 2) as well as the ON-state current are strongly improved for decreasing  $t_{ox}$ . An improvement of  $S$  is also seen for decreasing SOI thickness. The ON-state current, however, first increases but then decreases again as  $t_{si}$  is scaled down to 7 nm. In this case, two point measurements of the silicide contacts—although not ideal for measuring the sheet resistance—indicate an unexpectedly large sheet resistance ( $\sim 10$  times larger) overcompensating the improvement expected for the thinnest  $t_{si}$ . Note, however, that this can be avoided using selective silicon epitaxy prior to the nickel deposition in order to increase  $t_{si}$  in the source/drain areas. Thus, the best ON-state performance is expected for the thinnest SOI if the source/drain contacts are designed properly. In the present case though, the ON-state does not provide a good measure to quantify the impact of  $t_{ox}$  and  $t_{si}$  on the electrical behavior of the devices. On the other hand,  $S$  is insensitive to process-induced variations and source/drain resistances: If  $I_d$  is subdivided into a thermionic  $I_{th}$  and tunneling contribution  $I_T$ , the subthreshold swing can be written as  $S = \ln(10) \left( \frac{\partial I_{th}}{\partial V_{gs}} + \frac{\partial I_T}{\partial V_{gs}} \times \left( \frac{1}{I_{th} + I_T} \right) \right)^{-1}$ . Since NiSi has an SB of  $\Phi_{SB} = 0.64$  eV, much larger than  $kT$ , the terms related to  $I_{th}$  can be neglected and hence  $S$  is dominated by the change of the tunneling probability through the SB with changing  $V_{gs}$ .<sup>2</sup> Note, that this also renders  $S$  insensitive to process-induced changes of the actual SB height. This is reflected in the fact that the extracted  $S$  values of two different devices with  $t_{ox} = 3.5$  nm and  $t_{si} \approx 50$  nm [gray lines in Fig. 2(a) and (b)] are nearly identical although they exhibit a different ON-state current. At this point, it is important to mention that  $S$  is influenced by

<sup>2</sup>Note, that for a given SB height  $I_{th}$  can become of the same order as  $I_T$  if  $t_{ox}$  becomes very large. In the present case, however,  $I_T$  is still the dominant current contribution. Interchanging the source and drain contacts leads to slightly different  $S$ -values ( $\sim 5\%$ ) only in the case of  $t_{ox} = 24$  nm.

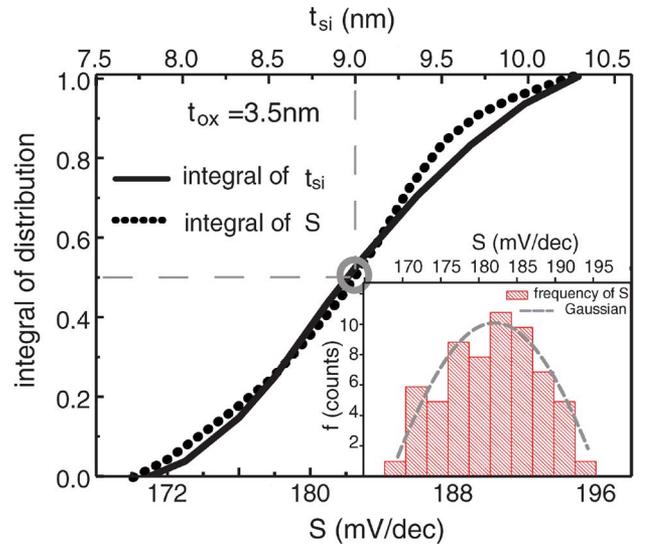


Fig. 3. Integral of the  $S$ -value distribution of randomly selected  $\sim 60$  devices (gray line) and of the distribution of the SOI body thickness (black line) for  $t_{ox} = 3.5$  nm. The inset shows the measured distribution of  $S$  together with a Gaussian curve fitting.

changes of the depletion charge as well as by trapped charges  $Q_{it}$  at the silicon/SiO<sub>2</sub> interface with changing  $V_{gs}$ . However, due to the low doping level of the SOI all devices in this letter are fully depleted. In addition, even for  $t_{ox} = 24$  nm, the capacitance associated with the interface trapped charge  $dQ_{it}/dV_{gs}$  [8] is estimated to be an order of magnitude lower than the oxide capacitance  $\epsilon_0\epsilon_{ox}/t_{ox}$  and hence has only a minor effect on  $S$ . As a result,  $S$  represents a robust measure to investigate the impact of  $t_{si}$  and  $t_{ox}$  on the carrier injection in SB-MOSFETs. Although the following discussion will be restricted to  $S$ , keep in mind that an improved  $S$  implies a better electrostatic gate modulation of the SB and hence it also implies an improved ON-state of the SB devices [5].

In order to investigate the influence of  $t_{si}$  and  $t_{ox}$  on the carrier injection in more detail, devices with  $t_{si}$  in the range between 7–55 nm on different sample chips exhibiting  $t_{ox} = 3.5, 10, 15,$  and  $24$  nm, respectively, are measured and  $S$  is extracted. Whereas  $t_{ox}$  can be determined precisely with an ellipsometer measurement, the exact SOI thickness of each individual device is not known due to body thickness variations of the initial SOI material. However, having confirmed for a few devices with TEM images that  $S$  increases with increasing  $t_{si}$  and since  $t_{si}$  is the only device-to-device variation that has an impact on the devices' OFF-state it is possible to correlate the distribution of  $S$  values extracted from measuring randomly chosen  $\sim 60$  devices with the distribution of  $t_{si}$  as measured with ellipsometry prior to the fabrication process. An example of such a distribution of  $S$  values (for  $t_{ox} = 3.5$  nm and  $t_{si} \approx 9$  nm) is shown in the inset of Fig. 3. The main panel of Fig. 3 shows the integral of the  $S$ - and the  $t_{si}$ -distribution. The gray circle, e.g., indicates that 50% of the devices exhibit an  $S$  of 183 mV/dec and below and 50% of the devices exhibit a  $t_{si}$  of 9 nm and below. Therefore, a certain  $S$  value can be associated with a certain SOI thickness, i.e., in the present case a device with a  $t_{si} = 9$  nm can be correlated with an  $S = 183$  mV/dec.

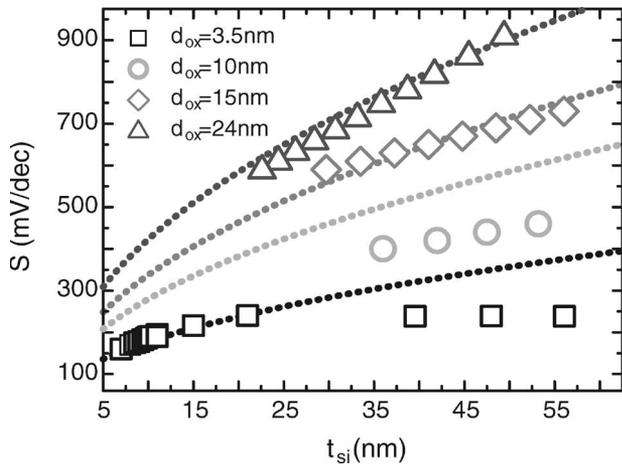


Fig. 4. Inverse subthreshold slope versus  $t_{si}$  for different oxide thicknesses. The dotted lines belong to an analytical approximation the dependence of  $S$  on  $t_{si}$  and  $t_{ox}$ .

Fig. 4 summarizes the dependence of  $S$  on  $t_{si}$  for devices with  $t_{ox} = 3.5, 10, 15,$  and  $24$  nm, respectively. In case of the device with  $t_{ox} = 3.5$  nm and  $t_{si} \leq 21$  nm,  $S$  decreases with decreasing SOI thickness. However, for  $t_{si} > 21$  nm the subthreshold swing saturates at a value independent of  $t_{si}$ . On the other hand, for larger  $t_{ox}$ ,  $S$  shows an increasing dependence on  $t_{si}$ . The dotted lines in Fig. 4 belong to calculated  $S$  values based upon an analytical computation of  $S$  for a fully depleted SOI SB-MOSFET as appropriate for the experimental situation [9]. This expression is given by<sup>3</sup>

$$S \approx \frac{kT}{q} \ln(10) \left( 1 - e^{-d/\sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} t_{si} t_{ox}}} \right)^{-1} \quad (1)$$

which approaches the thermal limit of 60 mV/dec if  $t_{ox} \rightarrow 0$ . Here,  $d$  is the thickness of the SB beyond which tunneling can be neglected; all other symbols have their usual meaning. Since  $d$  only very weakly depends on  $t_{ox}$  and  $t_{si}$  it is considered as constant ( $d = 3.7$  nm in the present case). The analytical expression reproduces well the experimental data in the case of  $t_{ox} = 3.5$  nm and  $t_{si} \leq 21$  nm as well as for  $t_{ox} = 15$  nm and  $t_{ox} = 24$  nm. Equation (1) suggests  $S$  values smaller than 100 mV/dec for, e.g.,  $t_{ox} = 1.5$  nm and  $t_{si} = 5$  nm implying a good carrier injection and therefore an improved ON-state.

The reason why for large  $t_{si}$  and small  $t_{ox}$ ,  $S$  is only weakly dependent (in the case of  $t_{ox} = 10$  nm) or even becomes independent of  $t_{si}$  (for  $t_{si} > 20$  nm and  $t_{ox} = 3.5$  nm) is that for a thin gate oxide the impact of the electric field at the BOX on the potential distribution of the SB becomes less and less important for increasing  $t_{si}$  and the electric field at the gate oxide mainly determines the potential landscape. On the other hand, if the device exhibits a thicker gate oxide, the influence of the gate oxide on the SB is diminished such that even in the case of larger  $t_{si}$  the BOX influences the potential distribution of the SB

<sup>3</sup>A similar dependence of  $S$  on  $t_{ox}$  has been found with simulations by Heinze and co-workers in case of carbon nanotube FETs [10].

and hence the carrier injection through the SB. As a result, SOI SB-MOSFETs show an improvement of the carrier injection if  $t_{si} \leq 6 - 7 \times t_{ox}$ . This has the important implication that devices with rather thick  $t_{ox}$  can still exhibit steep subthreshold swings if the body is scaled to an extremely small thickness, such as in a nanowire or nanotube. In fact, carbon nanotube FETs—a special case of UTB SB-MOSFETs—show an excellent OFF-state even for a rather thick  $t_{ox}$  (see, e.g., [11]). However, for small bodies and larger gate oxide thicknesses,  $S$  exhibits a strong dependence on  $t_{si}$  and thus small body thickness fluctuations lead to a significant variation  $\delta S = (dS/dt_{si}) \propto \sqrt{t_{ox}/t_{si}}$  of the subthreshold swing. Hence,  $t_{ox}$  should be as small as possible in order to achieve small values for  $S$ , insensitive to changes in  $t_{si}$ . On the other hand, in case of UTB SOI vertical quantization of carriers leads to an effectively increased SB height that deteriorates the device's ON-state performance [5] and yields a shift of the threshold voltage [9]. Consequently, to obtain a good carrier injection in SOI SB-MOSFETs,  $t_{si}$  should not be less than  $\sim 4$  nm and  $t_{ox}$  should be as small as possible enabling steep subthreshold swings with only small fluctuations of  $S$ .

In conclusion, we experimentally studied the impact of the gate oxide and channel thickness on the electrical performance of fully silicided SOI SB-MOSFETs. The extracted subthreshold swing served as a measure for the carrier injection through the SB. An improved switching behavior for either ultrathin gate oxides or ultrathin SOI bodies is found. However, a gate oxide as thin as possible is required in order to realize excellent device characteristics insensitive to fluctuations of the SOI body thickness.

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