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Comparative passivation effects of self-assembled mono- and multilayers on GaAs junction field effect transistors

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Control of semiconductor interface state density with molecular passivation is essential for developing conduction-based biosensors. In this study, GaAs junction field effect transistors (JFETs) are fabricated and characterized before and after passivation of the GaAs surface with self-assembled mono- and multilayers. The JFETs functionalized with 1-octadecanethiol monolayers and two types of self-assembled organic nanodielectric (SAND) multilayers exhibit significantly different threshold voltage (V_{th}) and subthreshold slope (S_{sub}) characteristics versus the unpassivated devices and provide useful information on the quality of the passivation. Two-dimensional device simulations quantify the effective density of fixed surface charges and interfacial traps and argue for the importance of the type-III SAND ionic charges in enhancing GaAs JFET response characteristics. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2899965]

Achieving reliable molecular passivation of semiconductor surfaces and understanding semiconductor surface–organic adsorbate interactions are of interest for a variety of applications, including biosensors.[1–3] GaAs is of particular interest because it allows easy, direct covalent organic thiol attachment in addition to its importance in microelectronics. Well-organized self-assembled alkanethiol monolayers on GaAs exhibit minimal surface oxidation,[4] but a dense monolayer does not guarantee high-quality electrical passivation, especially for surfaces having large inherent surface state densities.[5] GaAs surface states pin the Fermi level near midgap on unpassivated surfaces, as commonly observed for metal contacts to *n*-type GaAs and typically yield Schottky barrier heights of ~0.8 eV, regardless of the metal work function.[6] Hence, it is important to achieve effective electrical passivation from molecular monolayers, i.e., low interface state densities, for efficient modulation of the GaAs channel.

These issues are particularly important in conductance-based biosensors, since interface states can degrade device response and sensitivity to environmental changes. While nanowire-based devices offer advantages in sensitivity,[7] three-terminal planar devices with surface-immobilized molecular layers provide attractive model systems to study semiconductor–organic/biomolecule electronic interactions due to well-established device physics and well-developed fabrication processes. Achieving maximum coupling between molecular species and the semiconductor channel requires an unmetallized surface, especially in the receptor immobilization region. Conventional surface state characterization methods such as capacitance-voltage measurements and deep level transient spectroscopy can provide interface information, but require a top gate, typically a metal on top of the molecular layer. Studies on unmetallized test structures can avoid changes/distortion of signals arising from specific semiconductor surface–organic molecule interactions and can provide information on molecular-level events.

To this end, we investigate here the effects of self-assembled organic mono-/multilayer adsorbates on GaAs junction field effect transistor (JFET) characteristics and quantify the effects of molecular passivation on device response from threshold voltage (V_{th}) shifts and subthreshold slope (S_{sub}) changes, aided by two-dimensional (2D) device simulation. Chemisorption of 1-octadecanethiol (ODT) or self-assembled organic nanodielectrics (SANDs) are used to modify the GaAs JFETs since these treatments yield dense, structurally well-defined, and pinhole-free self-assembled mono- and multilayers on GaAs surfaces.[4,8] While SANDs are fabricated using silane precursors requiring hydroxyl-terminated surfaces, ODT monolayers use thiol groups which covalently bind to either Ga or As surface sites. The molecular structures of ODT, type-I SAND, and type-III SAND are shown in Fig. 1(a) and SAND properties are summarized elsewhere.[9] The JFETs utilize near-surface channel configuration to maximize device channel–surface layer interactions

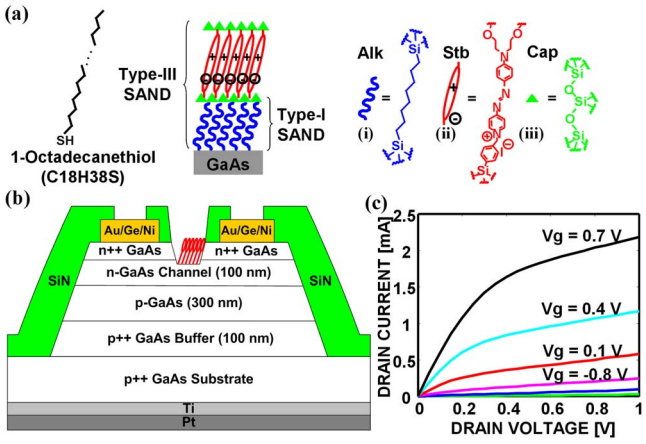

FIG. 1. (Color online) (a) Molecular structures of ODT, type-I SAND, and type-III SAND with components Alk, Stb, and Cap. (b) Cross-sectional view of a GaAs JFET (c) Output characteristic of a representative as-fabricated device.

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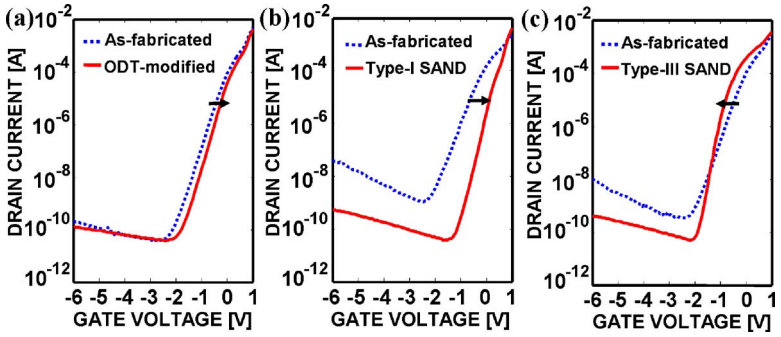

FIG. 2. (Color online) Transfer characteristics of GaAs JFETs modified with (a) ODT, (b) type-I SAND, and (c) type-III SAND. A negative threshold voltage shift (~0.3 V) with a steep subthreshold slope (178 mV/decade) is observed with type-III SAND passivation. V_{DS} was set to 0.1 V. The profiles of each subfigure refer to the same device.

and a back gate to modulate GaAs surface state occupancy as well as bulk channel conductivity. This structure enables quantification of adsorbate-semiconductor interactions and provides insights into conduction-based sensing mechanisms. We demonstrate that the different types of GaAs surface passivation result in dramatically different and well-defined V_{th} shifts and S_{sub} changes, and that the type-III SAND achieves the most effective passivation.

Figure 1(b) shows the GaAs JFET device structure. The epilayer structure consists of a 100 nm *n*-GaAs (2×10^{19} cm^{-3}) layer, a 100 nm *n*-GaAs (5×10^{17} cm^{-3}) channel layer, a 300 nm *p*-GaAs (5×10^{16} cm^{-3}) layer, and a 100 nm *p*-GaAs (1×10^{18} cm^{-3}) buffer layer, all of which are grown on a p^{++} GaAs substrate by molecular beam epitaxy. Device isolation is achieved by mesa etching, and a backside gate contact formed by e-beam deposition of Pt/Ti. Source/drain Ohmic contacts are defined by e-beam deposition of Au/Ge/Au/Ni/Au films and lift off, followed by 400 °C rapid thermal annealing in N_2 for 30 s. A Si_3N_4 passivation layer (300 nm, by plasma-enhanced chemical vapor deposition) is deposited, and active device and contact regions are exposed using a SF_6/O_2-based plasma reactive ion etch. In order to adjust V_{th}, a recess is formed by wet etching the *n*-GaAs layers. The length and width of the recess, 2 and 200 μm, respectively, determine the channel dimensions.

As-fabricated JFETs showed typical depletion-mode output characteristics [Fig. 1(c)]. For ODT deposition, the devices were immersed in concentrated HCl for 1 min to remove surface oxide, rinsed with de-ionized water, and then immersed in a 1 mM ethanol solution of ODT for 24 h. The devices were next rinsed with ethanol and dried under N_2. ODT solutions are reported to displace the thin surface oxide layer that reforms during the air exposure between steps.[4] For the SAND deposition, the devices were immersed in $NH_4OH:H_2O$ (1:1) for 5 min to terminate the surface with hydroxyl groups. NH_4OH exposure yields a thin oxide layer on the GaAs surface[10] and increased rates for digital etching (separate oxidation/etching steps) versus HCl.[11] Thus, NH_4OH treatment should lightly etch the GaAs surface, resulting in minor channel thickness reduction. For type-I and type-III SAND depositions, Alk/Cap and Alk/Cap/Stb/Cap reagents [Fig. 1(a)], respectively, were sequentially deposited using solution self-assembly techniques previously described.[8,9]

Figure 2 shows the transfer characteristics of representative GaAs JFETs before and after molecular passivation. Each subfigure refers to the same device before and after surface modification. Compared to the S_{sub} (334 mV/decade) of as-fabricated devices, type-I and type-III SAND passivations result in S_{sub} values of 245 and 178 mV/decade, respectively, while ODT-modified devices do not exhibit significant S_{sub} changes (300 mV/decade). Within each device type, a standard deviation of ~20% is observed for the S_{sub} values. Although some device-to-device variations in V_{th} and leakage current levels are observed within as-fabricated devices for each sample type (attributable to variations in the recess-etching process), a consistent and distinctive trend in modulation of device characteristics is observed without exception (for >15 devices of each type) after the surface modifications. Considering that S_{sub} is directly correlated with surface state density, ODT passivation appears to be less effective in reducing GaAs surface states than either type of SAND. Previous studies indicate that ODT passivation on GaAs causes a tenfold reduction in surface states only in the upper half of the band gap, leaving a high surface state density at midgap and the Fermi level pinned.[12] Type-III SANDs appear to be more efficient in electrically passivating GaAs surfaces than type-I, even though both type-I and type-III SANDs should provide nominally identical interfaces to GaAs via the Alk layer [Fig. 1(a)].

In addition to S_{sub} changes, ODT and type-I SAND passivations induce *positive* V_{th} shifts (ΔV_{th}) of 0.2 and 0.4 V, respectively, while type-III SAND induces a *negative* ΔV_{th} of 0.3 V. The standard deviations in ΔV_{th} for ODT, type-I SAND, and type-III SAND are 19%, 7%, and 11% of the mean values, respectively. The positive ΔV_{th} values for ODT and type-I SAND are attributed to a decrease in channel thickness accompanying the cleaning process prior to surface modification. A comparable ΔV_{th} is observed in a control sample subjected to the same cleaning process without subsequent surface modification. Air-oxidized *n*-type GaAs is known to have a large density of surface states (~10^{13} eV^{-1} cm^{-2}) that pin the surface Fermi level at E_C −0.8 eV and induce surface band bending,[5] corresponding to a surface depletion width of ~47 nm for GaAs JFET channel layers. Substantial reduction in GaAs surface states is expected to decrease surface band bending and accordingly the depletion width, causing a negative ΔV_{th}, i.e., a greater negative gate bias to completely shut off the channel. In comparison to type-I SAND, the type-III SAND utilizes the same cleaning process but deposition of additional Stb and Cap layers. Therefore, the Stb layer appears to play a critical role in reducing surface state density, resulting in a net negative ΔV_{th} of 0.7 V.

To quantitatively estimate changes in "effective" surface state density after the various passivation layers are applied, a 2D device simulator (MEDICI) was used to simulate the transfer characteristics of as-fabricated and modified GaAs JFETs. The interfacial trap density (Q_{IT}) and fixed charge density (Q_F) were varied,[13] reasonably assuming the charge

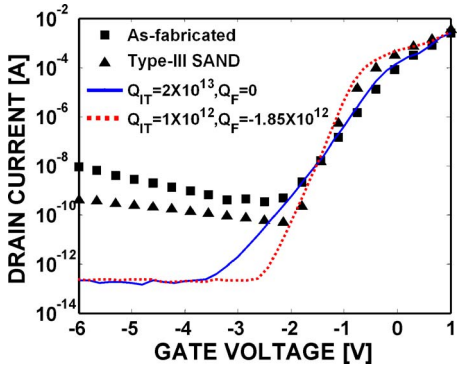

FIG. 3. (Color online) Transfer characteristics from experimental data for (i) as-fabricated (squares) and type-III SAND-modified (triangles) GaAs JFETs and (ii) MEDICI simulations for as-fabricated (solid lines) and type-III SAND-modified (dotted lines) GaAs JFETs. Fitting parameters are fixed surface charges (Q_F) and interfacial traps (Q_{IT}).

states are present at the GaAs-molecule interface. Note that since the GaAs surface is readily oxidized in air,[11] the data and simulations for the as-fabricated devices correspond to an oxidized surface. Since the molecular charge states should be 1–2 nm above the surface,[9,14] the extracted Q_{IT} and Q_F should be viewed as equivalent values at the GaAs surface. It is difficult to estimate the exact positions of molecular charged states experimentally, and the present approach provides a practical tool for comparing electrical passivation effects of various molecular layers. Although a comprehensive description of GaAs surface states is challenging due to different sources of states such as deep donors "EL2" and donorlike/acceptorlike surface states,[15] acceptorlike surface states appear to determine the surface Fermi level position and dominate *n*-GaAs device electrical characteristics.[16] Hence, in the simulation, acceptorlike traps were used to represent the GaAs surface states. Acceptorlike traps are negatively charged when filled with electrons and neutral when empty, resulting in a negative V_{th} shift and S_{sub} depression. Simulation results for the type-III SAND passivation are shown in Fig. 3 with the solid and dotted lines representing approximate best-fit values to as-fabricated (squares) and type-III SAND-modified (triangles) devices, respectively. The difference between the curves below $V_G=-2$ V is due to nonideal leakage currents through reverse-biased *pn* junctions,[17] not included in the simulation. The best-fit values for the data (Fig. 2) are $Q_{IT}=2\times10^{13}$ eV^{-1} cm^{-2} and $Q_F=0$ cm^{-2} for the as-fabricated device, $Q_{IT}=9\times10^{12}$ eV^{-1} cm^{-2} and $Q_F=0$ cm^{-2} for ODT passivation, $Q_{IT}=5\times10^{12}$ eV^{-1} cm^{-2} and $Q_F=0$ cm^{-2} for type-I SAND passivation, and $Q_{IT}=1\times10^{12}$ eV^{-1} cm^{-2} and $Q_F=-1.85\times10^{12}$ cm^{-2} for type-III SAND passivation. Comparison of the Q_{IT} values for various device types indicates that a molecular layer employing the silane surface chemistry along with the Stb/cap layers (type-III SAND) provides significantly better electrical passivation than the thiol chemistry, while the silane chemistry with just a cap layer (type-I SAND) shows a more modest effect. The Q_{IT} difference between type-I and type-III SAND passivation can be explained by considering defects in the film structures. We speculate that, in the case of type-III SANDs, subsequent Stb and cap layer deposition on the type-I SAND fills vacant sites on the GaAs surface and/or seals defects via the cross-linked network, rendering the type-III SAND essentially pinhole-free. The 20-fold decrease in Q_{IT} observed upon passivation with the type-III SAND is consistent with a previous study in which GaAs metal-insulator-semiconductor FETs with a type-III SAND gate insulator exhibited Q_{IT} as small as $\sim10^{12}$ eV^{-1} cm^{-2} with enhanced capacitance-voltage modulation.[8] For the type-III SAND, the large reduction in Q_{IT} induces a substantial negative V_{th} shift ($\sim$7 V), so that negative fixed charges ($Q_F=-1.85\times10^{12}$ cm^{-2}) must be incorporated to fit the data. The negative fixed charges are tentatively attributed to the negative I^- ions in the π-conjugated Stb layer which create a strong local electrical field oriented toward the underlying GaAs surface.[14]

The observed changes in surface state densities upon molecular binding likely explain a mechanism contributing to responses of sensor devices involving molecular interactions with bare semiconductor surfaces. For sensors involving initial deposition of molecular receptors and subsequent binding of target molecules to the receptors, the passivation effects observed in this study can provide insights for selection of suitable surface chemistries. Minimizing surface state densities and subsequent effects due to ions in the solution are important to minimizing background effects. High-quality molecular GaAs surface passivation and modulation of device characteristics by molecular dipole moments should pave the way for application of GaAs-based sensors.

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