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Externally assembled gate-all-around carbon nanotube field-effect transistor

Zhihong Chen
IBM Corp

Damon Farmer
Harvard University

Sheng Xu
Harvard University

Roy Gordon
Harvard University

Phaedon Avouris
IBM Corp

See next page for additional authors

Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor

Zhihong Chen, *Member, IEEE*, Damon Farmer, Sheng Xu, Roy Gordon, Phaedon Avouris, *Member, IEEE*, and Joerg Appenzeller, *Senior Member, IEEE*

***Abstract*—In this letter, we demonstrate a gate-all-around single-wall carbon nanotube field-effect transistor. This is the first successful experimental implementation of an off-chip gate and gate-dielectric assembly with subsequent deposition on a suitable substrate. The fabrication process and device measurements are discussed in the letter. We also argue in how far charges in the gate oxide are responsible for the observed nonideal device performance.**

***Index Terms*—Carbon nanotube (CN), field-effect transistor (FET), gate-all-around (GAA).**

I. Introduction

SINGLE-WALL carbon nanotubes (CNs) are considered to be one of the most promising candidates for post-CMOS applications, mainly owing to their smallness and ballistic transport properties [1]. The ultrathin body of CNs (of the order of a few nanometers) allows for aggressive channel length scaling while maintaining excellent gate control [2]. In general, a gate-all-around (GAA) structure is expected to be the ideal geometry that maximizes electrostatic gate control in FETs [3], [4]. Combining the ultrathin body of a CN with an GAA device geometry is a natural choice for ultimate device design. Dai *et al*. [5] have shown a CNFET with an "Ω" shaped dielectric coating exhibiting improved electrostatics. However, a real GAA layout requires both the dielectric and the gate metal to completely wrap around the semiconducting channel.

THE surface of CNs is known to be chemically inert to most reactions. Thin (<3 nm) uniform coating of a CN with a dielectric can only be achieved after modifying the CN surface by introducing some type of functional layer such as *deoxyribonucleic acid* (DNA), as shown in [5]. In order to obtain an GAA structure, the CN needs to be freestanding prior to the dielectric and gate metal deposition. Without the assistance from the substrate, dielectric deposition becomes even more challenging. In this paper, we demonstrate for the first time a GAA-CNFET, consisting of a functionalized nanotube wrapped by an Al_2O_3 dielectric and tungsten nitride (WN) gate metal using atomic layer deposition (ALD). This is the first successful experimental attempt of an off-chip transistor assembly, which allows for the placement of arrays of transistors on chip at maximum densities [6].

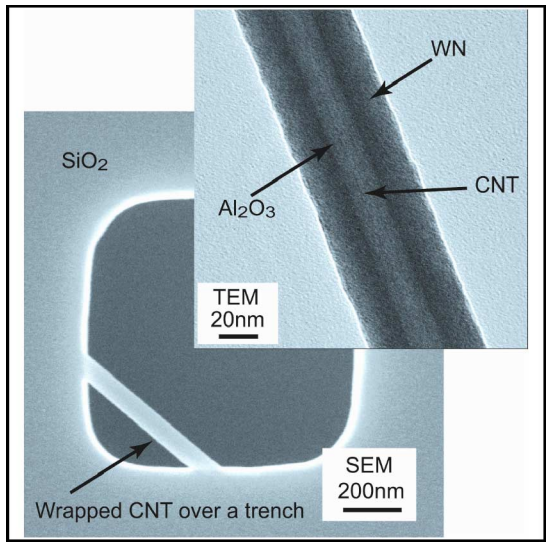

Fig. 1. Bottom image: An SEM of a wrapped CN suspended over a trench. Upper image: A TEM image of a NO_2 functionalized nanotube wrapped with a 7 nm ALD Al_2O_3 dielectric and a 20 nm ALD WN gate metal. The total diameter of the final structure is about 54 nm.

II. Device Fabrication

The details of the wrap around process can be found in [7]. After functionalizing the nanotube with NO_2, an ALD process is used to deposit a uniform Al_2O_3 film of 7 nm around the tube. A WN gate of 20 nm, also deposited by the ALD, is then wrapped around the dielectric. Fig. 1 shows an SEM and a TEM image of a uniformly wrapped CN. The wrapped CNs are then dispersed into solution and drop cast onto the desired substrate.

Fig. 2(A) shows the schematic of the GAA-CNFET. The WN and Al_2O_3 are removed everywhere from the CN by wet chemical etching,[1] except in the gate area. Source/drain (S/D) contacts are made at the ends of the CN, leaving uncovered tube segments for chemical or electrostatic doping. The part of the CN under the gate is kept undoped.

Depending on the type of doping in the outer segments, we can create a p/i/p or n/i/n profile. Fig. 2(B) and (C) displays the

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Z. Chen and P. Avouris are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: zchen@us.ibm.com; avouris@us.ibm.com).

D. Farmer is with the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138 USA (e-mail: dfarmer@us.ibm.com).

S. Xu and R. Gordon are with the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138 USA (e-mail: shengxu@fas.harvard.edu; gordon@chemistry.harvard.edu).

J. Appenzeller is with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907-2035 USA (e-mail: appenzeller@purdue.edu).

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[1]WN gate is etched with NH_4OH and H_2O_2 solution, and Al_2O_3 dielectric is etched with H_3PO_4 solution.

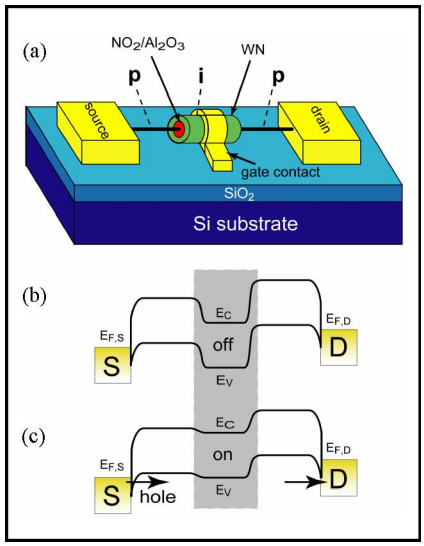

Fig. 2. (a) Schematic of a GAA-CNFET. A MOSFET like p(n)/i/p(n) structure is realized by gating only the middle segment of the CN with an all-around WN metal gate and Al_2O_3 dielectric. Extended S/D segments are electrically p-doped by the Si back gate. (b) Band diagram in the OFF-state. (c) Band diagram in the ON-state.

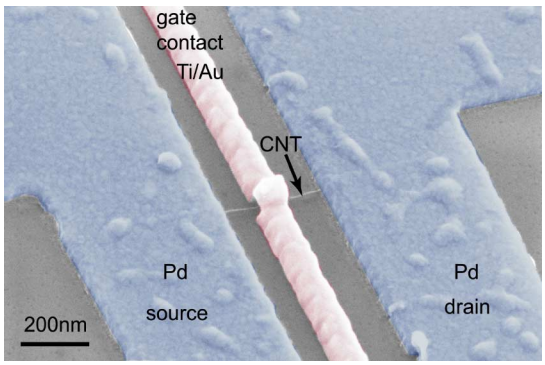

Fig. 3. SEM image of a p/i/p GAA-CNFET located on a heavily p-doped Si substrate with 100 nm SiO_2. The CN is contacted by high work function Pd S/D contacts for hole injection, and the extended S/D segments are electrically p-doped by the Si back gate. The actual gate length is shorter than the designed length due to overetching along the tube axis, resulting in a partially hollow tunnel, shown in the SEM.

band diagrams of a p/i/p transistor in the "OFF" and "ON" state. An SEM image of a GAA-CNFET device with *Pd* S/D contacts locating on a 100 nm SiO_2 substrate is shown in Fig. 3. A Ti/Au electrode makes electrical contact to the WN gate, and at the same time serves as the etch mask for the gate definition. The designed WN gate length and extended S/D segments are 100 nm. However, it was found that the etch rate of both WN and Al_2O_3 along the tube axis is faster than in the radial direction. Therefore, the actual gate length turned out to be much shorter than the designed length.

III. Characterization Results

The functionalization group NO_2, serves as the reaction center and facilitates the ALD Al_2O_3 growth on free standing CNs. One important question is, whether this NO_2 group introduces

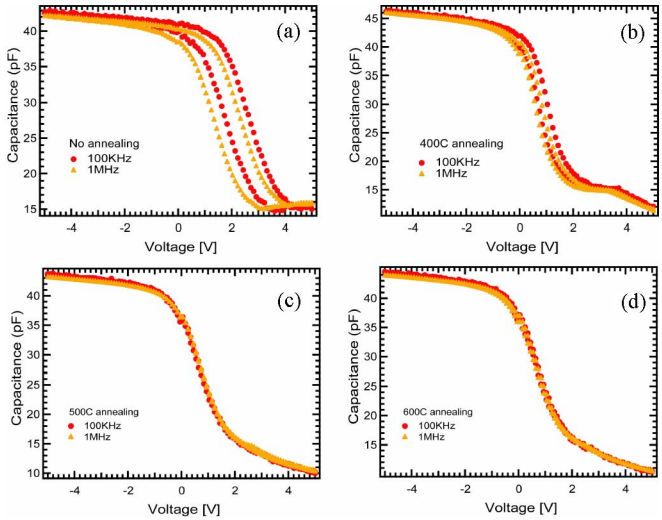

Fig. 4. *CV* measurements on Al–Al_2O_3/NO_2–Si test structures at various annealing temperatures. Our analysis suggests that a 500 °C postdeposition annealing step is necessary to remove the majority of *the oxide trapped charges and fixed oxide charges*. No significant further improvement has been observed for temperatures beyond 500 °C.

extra charges. To explore this aspect, a test capacitor was fabricated on a Si substrate using the same functionalization and 10 nm ALD Al_2O_3 process, followed by Al counter electrode definition. The *CV* measurements for as-grown films show strong frequency dependence and hysteresis [see Fig. 4(A)], which indicate the existence of a substantial amount of fixed oxide charges and oxide trapped charges. In order to improve this situation, we have performed a post-ALD annealing in Ar at various temperatures for 2 h. Temperatures above 500 °C were found to be sufficient to significantly improve quality of the oxide stack. Since the slope of the *CV* characteristics is unaffected by the annealing process, we conclude that the interface trapped charges remained the same before and after the treatment. The positive impact of the annealing was also confirmed from device characteristics of the GAA-CNFETs that become less noisy and show less hysteresis after annealing.

Fig. 5 shows the subthreshold and output characteristics of a GAA-CNFET. A back gate voltage of $V_{\rm bg} = -20$ V was applied to the Si substrate to achieve a high doping level in the extended S/D regions that enables hole carrier injection. The threshold voltage $V_{\rm th}$ is about 2 V, which is a result of some remaining fixed oxide charges and the use of a high work function WN metal gate. The OFF-state is reached at more positive voltages [see Fig. 2(B)]. The diameter of the CN is rather large (>2 nm), corresponding to a band gap of about 300 meV. For increasing gate voltage, the conduction band of the channel can move beyond the valence band of the extended source region, resulting in a band-to-band tunneling leakage current [8]. Using nanotubes with slightly smaller diameters will enable larger ON/OFF ratios and will allow the use of larger drain biases. The nonideal subthreshold slope (250 mV/dec) is probably due to the finite amount of interface trapped charges and short-channel effects caused by the overetching mentioned earlier. The interface trapped charge contribution to these GAA-CNFETs is

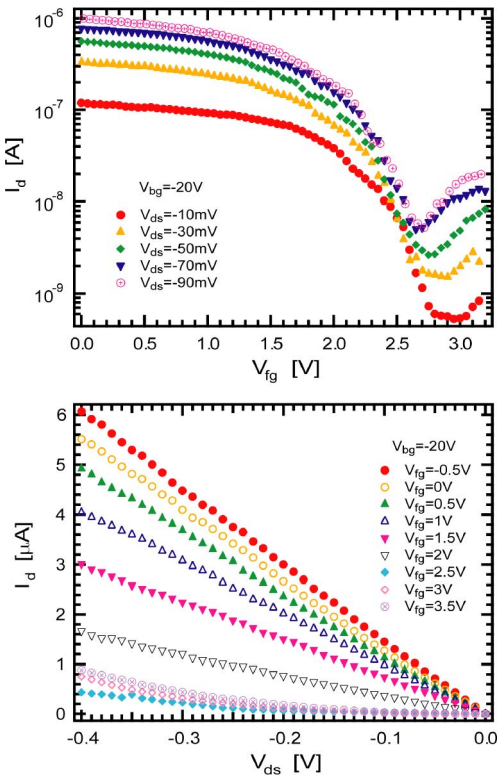

Fig. 5. Subthreshold and output characteristics of a GAA-CNFET. A Si back gate voltage of $V_{\rm bg} = -20$ V is applied to create the desired p/i/p profile.

similar to Si MOSFETs. However, the depletion capacitance is zero and transport mechanisms in nanotube devices are fundamentally different from Si [2]. Future studies will focus on correlating the actual gate length and device characteristics and on efficiently removing interface trapped charges.

IV. Conclusion

In conclusion, we demonstrated the fabrication process and measurements of the first externally assembled GAA-CNFET. Improvement of the interface between the CN channel and gate stack by means of various annealing conditions was shown.

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