ON NONLINEAR CIRCUIT COMPONENTS WITH N-SHAPED CONDUCTANCE CHARACTERISTICS

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CONDUCTANCE CHARACTERISTICS

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ABSTRACT


Currently, three-terminal devices with N-shaped I-V characteristics are being fabricated for switching and multi-valued logic applications. The purpose of this study is to investigate switching speed improvements and potential problems of circuit designs employing these nonlinear devices. In this work, both two-terminal and three-terminal devices are analyzed. A design methodology is developed for a second-order two-terminal device circuit and a novel method of I-V characterization is presented. For the three-terminal device, a simple PSpice macromodel is developed and a new figure of merit for switching speed improvement is given. A practical chaotic synthesis method is proposed for this device in a third-order autonomous feedback circuit. The success of this synthesis approach leads to a prediction of possible chaotic behavior in switching configurations.
1. INTRODUCTION

1.1 Motivation

Nonlinear circuits are an interesting and increasingly important area of circuit theory, but the availability of nonlinear design techniques limits their practical application. While electrical engineers are well educated in the area of linear circuits, many lack an understanding of nonlinearities and how to manage or apply them effectively. The result is often a one to one association of nonlinearity with undesirable behavior. With successful design methods and performance predictions, an engineer could be comfortable with nonlinearities and manipulate or even create them to his advantage. Of course, a general set of nonlinear design tools is well outside the scope of one study and probably one lifetime; but the development of a toolkit for a general type of nonlinearity with emphasis on a base application may be possible.

Why would an engineer leave a comfortable linear world? The theory is well known and the results speak for themselves. Mainly, engineers pursue nonlinear approaches to obtain performance that linear circuits cannot provide. Several DC nonlinear functionals [1] such as analog multipliers and comparators are fairly common. Diodes have been used extensively to clip, clamp, block, rectify, etc. [2, 3], and transistors are the key element in digital electronics [4]. More recently, nonlinear DC transfer functions have been synthesized by the approaches of [5, 6, 7].

In the realm of dynamic circuits, linear circuit theory has a much greater foothold. In the DC domain, a nonlinear system is explained by nonlinear algebraic equations which can be solved graphically or by numerical methods. For dynamic circuits, coupled nonlinear differential equations must be solved. This is generally not possible in closed form. Good circuit simulators such as PSpice can numerically give accurate performance prediction, but a designer gains much less insight by this approach. A goal of this work is to demonstrate that supplementing linear techniques with nonlinear analysis can lead to practical nonlinear synthesis methods.
As a motivational example, I cite the simple linear second-order autonomous system of Equation 1.1.

\[ \ddot{x} + ax + bx = 0 \]  

(1.1)

Linear systems theory predicts a stable oscillation (assuming nonzero initial conditions) if the system characteristic equation gives a pair of complex conjugate poles lying on the imaginary axis. For this condition to occur, the damping term \( a \) must be exactly zero and the constant \( b \) positive. This design is not robust or practical since any deviation from the first requirement results in an instability or a decaying oscillation.

By designing the circuit with nonlinear damping, it is possible to obtain a second-order oscillation which is structurally stable and practical. Consider the case where the linear damping term \( a \) is replaced by the nonlinear damping of Equation (1.2) and let \( b \) equal one. The result is Van der Pol's equation [8].

\[ a(x) = -\epsilon(1 - x^2), \quad \epsilon > 0 \]  

(1.2)

Since the only equilibrium point of the system, \( x \) equal to zero, is locally unstable and the system is globally bounded, an oscillation is expected.

The linear oscillator (\( a=0 \)) and the nonlinear oscillator are functionally different in terms of energy and oscillation amplitude. The linear oscillator is a conservative system: the system energy remains constant for all time. The amplitude of the oscillation is determined by the system initial conditions, thus there exists an infinite number of possible oscillation trajectories in the phase plane.

This nonlinear oscillator example is not conservative. The steady state condition for the system is the same limit cycle for all initial conditions and the system may lose or add to its initial energy to achieve the stable oscillation. Over the steady state limit cycle, the system energy may still change with time, but the net change in one period is zero. For \(-1 < x < 1\) the system gains energy, and for \( |x| > 1 \) the system loses energy. The oscillation amplitude is determined by the steady state trajectory which gives the energy balanced condition. Conservative nonlinear oscillators are also possible, but they suffer from the same practical downfalls as the linear oscillator.

As an extension to this example, consider the same two oscillators driven by a sinusoidal forcing function. For nonzero initial conditions, the linear oscillator shows both a natural and a forced response. If the forcing function is at a different frequency than the
natural oscillation frequency, a periodic or almost periodic system results. For zero initial conditions, the linear system response is at the same frequency as the forcing function or can be considered locked to the forcing function for all amplitudes and frequencies.

For the nonlinear oscillator example, the natural oscillation will exist and may or may not lock to the excitation as a function of amplitude and frequency. An interesting and important study is to predict the locked condition. This phenomenon is a property only of nonlinear oscillators. The details of this section can be found in [8].

1.2 Linear Oscillator Circuits: A Brief Review of Techniques

Since oscillators are a recurring theme in this work, a review of a few linear circuit techniques is worthwhile. Although these techniques give limited information for nonlinear systems, they do give insight into the possibility of an oscillation. As a vehicle for investigation, consider a linear two-port network terminated in a linear inductor and capacitor as shown in Figure 1.1. The two-port network contains only zero-order elements (resistors, controlled sources, ideal transformers, etc) and can be characterized in terms of h-parameters.

![Fig. 1.1. Linear second-order circuit model.](image)

1.2.1 A time domain approach

The time domain approach to analyzing the system of Figure 1.1 begins by formulating the linear state equations.

\[
\begin{bmatrix}
-I_L
\end{bmatrix}
= 
\begin{bmatrix}
-h_{11} & h_{12} \\
L & -L \\
h_{21} & -h_{22}
\end{bmatrix}
\begin{bmatrix}
I_L \\
V_C
\end{bmatrix}
\]  

(1.3)
Decomposing the matrix of Equation (1.3) into its eigenvalues and associated eigenvectors, a solution can be obtained given the initial conditions [9]. For a simple second-order system, the results of this method can be demonstrated in the two dimensional state space plot. Equation (1.4) gives the characteristic equation which defines the eigenvalues for the system, and Figure 1.2 shows the associated eigenvectors in the state space. This theory predicts a stable oscillation (assuming nonzero initial conditions) as in Figure 1.2(e) if the system characteristic equation gives a pair of complex conjugate poles lying on the imaginary axis. Again this design is not practical since it is the boundary case between Figures 1.2 (d) and (f).

\[ \lambda^2 + \lambda \left( \frac{h_{11}}{L} + \frac{h_{22}}{C} \right) + \frac{h_{11}h_{22} - h_{12}h_{21}}{LC} = 0 \]  

(1.4)

![Fig. 1.2. Linear second-order system state space eigenvectors](image)

### 1.2.2 Frequency domain approaches

Another popular approach to predicting autonomous oscillation in linear systems is to consider the sinusoidal steady state circuit model and enforce the Barkhausen criterion [10]. In the circuit of Figure 1.1, the inductor and capacitor are replaced with their respective sinusoidal steady state impedances and the hybrid [11] algebraic Equation (1.5) is obtained.
To obtain a nontrivial solution, the circuit matrix of (1.5) must have a determinant of zero. This requirement is the Barkhausen criterion and it generates a pair of equations in terms of frequency \( \omega \) and the circuit parameters. Solving these equations gives the frequency as a function of circuit parameters and the required relationship between parameters to provide a conservative system. Applying this method gives the same results as the time domain approach for Figure 1.2(e).

Another useful frequency domain approach is to consider terminating a one-port network of zero-order devices, capacitor and inductors to obtain an oscillation \([12]\). In the frequency domain, the one-port input immittance can be reduced to frequency dependent real and imaginary parts. By terminating the system in its negative compliment immittance, an oscillation is obtained. Writing a Kirchoff equation at the input port shows this is just a scalar application of the Barkhausen criterion.

### 1.3 Nonlinear Resistance and Conductance Devices

Nonlinear resistance and conductance devices have been studied since the vacuum tube era \([8]\). The fact that tubes and solid state devices are very nonlinear makes this a requirement not a novelty. The most commonly studied applications of these elements involve a linearization analysis about a bias point and an investigation of the linear small signal excitation response \([13, 14]\). For many devices and circuit configurations, this approach is highly successful and the nonlinearity effects are observed as distortion in the actual response signal. As discussed previously, this analysis fails to give a designer much information for certain nonlinear device applications such as oscillators. At best, the linear analysis predicts that an oscillation may exist and gives a reasonable frequency estimate. The rest of the important information lies in the nonlinearities. Thus, a successful nonlinear circuit analysis technique may be both application and nonlinearity specific.

Often devices with interesting nonlinearity lead to new or improved applications, but the desired nonlinear characteristics may also lead to undesirable dynamic behavior. Specifically, an N-shaped conductance or resistance device as in Figure 2.1 is interesting since it exhibits a negative differential resistance (NDR) region. This device has many possibilities, but it also has the potential to give an unwanted oscillation in the presence of...
stray inductance and capacitance. Therefore, it is essential to be able to predict problems and understand them for the successful application of these devices.

N-shaped conductance and resistance oscillators have been heavily investigated in the past. Van der Pol's classic work in the 1920's [8] began as a model for a vacuum tube oscillator circuit. With the invention of solid state transistors, some interest was pulled away from negative resistance since these state of the art devices did not have the NDR regions. In 1958, Esaki reinvented NDR regions with solid state: tunnel diodes [15]. These devices were popular in the 1960's and early 1970's and were the typical example in early nonlinear circuits works [16, 17]. Various applications were proposed for these devices with switches, oscillators, and negative resistance amplifiers being the most popular [18, 19, 20, 21]. A more recent work in this area for microwave applications is given in [22].

Recently, new solid state Resonant Tunneling Devices (RTD) have become hot topics in the research literature. Both diodes and transistors have been presented which exhibit single and multiple negative resistance regions [23, 24, 25]. Researchers in this area have speculated on a wide variety of potential applications for these new devices: RF oscillation, high speed switching, multi-valued logic, and A/D conversion [26, 27, 28, 29].

The primary goal of this research is to analyze a two-terminal N-shaped conductance and a three-terminal N-shaped conductance and show that nonlinear analysis techniques can be used to predict unwanted behavior and interesting new behavior. Furthermore, the results here are intended to be a heads up to researchers investigating the previously mentioned applications.

1.4 The Problem

In this work, two fundamental problems of using these devices in practice are addressed. The first problem concerns the I-V characterization of these devices. Often, basic laboratory techniques lead to characteristic measurements similar to Figure 1.3 [24, 25]. Is this a correct characterization? If not, can a simple experimental method be proposed to reconstruct a correct characterization?

The second problem concerns the three-terminal device and has three parts. Since the three-terminal devices are being considered for high speed switching and logic applications, can a figure of merit be developed for them similar to those used to compare speed of transistors? Second, in the proposed applications, effects of parasitic inductance and capacitance are often ignored or only first-order models are considered. Figure 1.4(a) gives an example of a simple switching network with a three-terminal device and Figure
1.4(b) gives a more complete model. Does a model which includes these components in a practical design configuration show the possibility of undesirable dynamics such as chaos? Third, can a design method be developed to synthesize a practical chaotic modulator from these devices?

Figure 1.3. Typical I-V characterization seen in research literature.

Fig. 1.4. Circuit configurations under investigation.

In the effort of solving these problems, several issues popped up which were equally interesting and their solutions are included in this study. For example, the I-V characterization method proposed in this work comes from a special case of a more general analysis of the system.
1.5 The Structure of This Document

This study has been organized into two major portions. Chapters 2 through 5 investigate the two-terminal N-shaped conductance device. This work is done to set up a background for attacking the three-terminal device and also to rework many concepts from the standpoint of circuit design rather than analysis. Chapter 2 offers a stability plot approach to understanding and predicting the dynamics of the naturally arising second-order model of the two-terminal conductance. In Chapter 3, a method is given for predicting amplitude, frequency, and stability of autonomous and nonautonomous oscillations of the two-terminal device. In Chapter 4, a novel current-voltage characterization method is derived from the results of Chapters 2 and 3. Finally in Chapter 5, a quick look is taken at the implications of replacing the linear capacitance of the second-order model with a nonlinear one.

Chapter 6 begins the three-terminal device work with the mathematical model and PSpice macromodel developed for this study. Chapter 7 takes a look at predicting switching times and switching figures of merit for these new devices. Chapter 8 provides a parallel development to the work of Chapter 3 for predicting autonomous and nonautonomous oscillations. In Chapter 9, a novel application of these devices is proposed and a design procedure developed for the practical synthesis of chaotic circuits. The results are further investigated to show direct impact on the results of Chapters 7 and 8. In Chapter 10, a design criterion is developed to determine whether an available three-terminal device is a candidate for a prescribed chaos design.

All proposed ideas are verified throughout this work with PSpice simulation, and laboratory work is being presented as one separate chapter. Chapter 11 serves as a summary of the experimental demonstrations performed for this study. Finally, Chapter 12 reviews and concludes the heart of this work.
2. A TWO-TERMINAL DEVICE WITH AN N-SHAPED CONDUCTANCE CHARACTERISTIC

2.1 Introduction

Although devices with negative differential conductance (NDC) regions are potentially useful, their practical characterization and application are often difficult [26, 30]. A systematic design and analysis method would be very helpful to the engineer in predicting behavior. The goals of this chapter are to provide a design approach based on the local stability method of Liapunov [31]. The results of the analysis are presented in a stability plane similar to [20, 32] but from a circuit designers point of view.

2.2 The N-Shaped Conductance Characteristic

The current-voltage characteristic of a typical two-terminal N-shaped conductance is shown in Figure 2.1.

![N-shaped I-V characteristic](image)

Fig. 2.1. N-shaped I-V characteristic.
In this work, the device is modeled by the nth-degree polynomial in voltage as given by Equation (2.1). The device is termed a conductance device since it can be expressed only as a single valued function of voltage.

\[ I = f(V) = \sum_{i=1}^{n} \alpha_i V^i \]  \hspace{1cm} (2.1)

From a modeling standpoint, this relationship is convenient since Spice circuit simulators have polynomial controlled sources and the derivatives of the function with respect to voltage are continuous. Furthermore, many I-V solid state models are exponential functions and Equation (2.1) could represent a truncated expression [33].

Although this model satisfactorily describes the equilibrium N-shaped conductance, it is often not sufficient in modeling dynamic applications of the practical device. The circuit of Figure 2.2 is considered in this chapter as the simplest practical design model. The extra linear circuit parameters may be parasitics or components chosen by the circuit designer. A bias voltage is also shown in the circuit model. As the analysis in this chapter develops, it will become apparent these components are a necessary consideration due to the NDC region.

\[ V_{Bias} \]
\[ R \]
\[ L \]
\[ I_L \rightarrow \]
\[ + \]
\[ V \]
\[ - \]
\[ C \]
\[ I = f(V) \]

Fig. 2.2. N-shaped conductance circuit model with applied bias.

### 2.3 Second-Order Differential Equation Model and a Global Stability Plot

Standard circuit analysis techniques are used to obtain the following differential equation models for the nonlinear conductor voltage and inductor current of Figure 2.2.

\[ \frac{dV}{dt} = \frac{1}{C} (I_L - f(V)) \]  \hspace{1cm} (2.2a)

\[ \frac{dI_L}{dt} = \frac{1}{L} (-RI_L - V + V_{Bias}) \]
2.3.1 Equilibrium points

The first step in understanding this circuit is to evaluate the equilibrium points for an applied bias voltage. A useful approach is the graphical load line method which can be arrived at by considering the equilibrium condition of Equation (2.2). This approach is equivalent to the usual DC steady state analysis with the inductor a short circuit and the capacitor an open.

\[
\frac{d^2V}{dt^2} + \frac{dV}{dt} \left( \frac{R}{L} + \frac{1}{C} \frac{df}{dV} \right) + \frac{V}{LC} + \frac{R}{LC} f(V) = \frac{V_{Bias}}{LC}
\]  

(2.2b)

Figure 2.3 shows the load line intersections with the nonlinear resistance characteristic for two distinctly different values of series resistor \( R \). \( R_1 \) is selected to give a load line with either one or three equilibrium solutions depending on \( V_{Bias} \). \( R_2 \) is chosen to give only one equilibrium point over the entire bias range.

![Load line approach to equilibrium point determination.](image)

A natural question to answer first concerns the critical value of the series resistor which separates these two different equilibrium results. This value corresponds to the
minimum slope (since negative) of the nonlinear conductance characteristic and occurs at its inflection point. This value is denoted as $g_{\text{min}}$ and the following relationship guarantees a single equilibrium point for all bias voltages.

$$R < -\frac{1}{g_{\text{min}}} = R_{\text{critical}}$$  \hspace{1cm} (2.4)

### 2.3.2 Linearized stability of equilibrium and nonequilibrium points

The next step in this analysis is to look at the local stability of both equilibrium and nonequilibrium points. To begin, the differential equation is normalized by defining

$$r = \frac{1}{\sqrt{L/C}} t \quad \text{and} \quad z_0 = \frac{L}{\sqrt{C}}$$  \hspace{1cm} (2.5)

The time scaled differential equations become

$$\frac{dV}{d\tau} = z_0(I_L - f(V))$$

$$\frac{dI_L}{d\tau} = \frac{1}{z_0}(-RI_L - V + V_{\text{Bias}})$$  \hspace{1cm} (2.6a)

$$\frac{d^2V}{d\tau^2} + \left(\frac{R}{z_0} + \frac{df}{dV}\right) \frac{dV}{d\tau} + V + Rf(V) = V_{\text{Bias}}$$  \hspace{1cm} (2.6b)

A perturbation analysis is performed on Equation (2.6) and the local stability of equilibrium and nonequilibrium points determined by the eigenvalues of the linearized variational equations as suggested by Liapunov [31]. Equation (2.7) gives these eigenvalues where $g$ denotes the incremental conductance evaluated at the point of interest.
It is clear from the form of the eigenvalue expression there are different types of stability and instability dependent on circuit parameters and the incremental conductance. One observation is that for \( g > 0 \), the eigenvalues are guaranteed to have negative real parts; thus, equilibrium points lying on the I-V characteristic in a positive differential conductance region are locally stable. The following relationships define the basic stability results over the entire range of \( g \).

Case 1. Complex eigenvalues and \( g < 0 \).

\[
\frac{R}{Z_0} < 2 + gZ_0 = h_2(g)
\]  

(2.8)

In this underdamped case, the equilibrium point is locally stable if the real parts of the eigenvalues are negative. The following relationship defines the stable subregion.

\[
\frac{R}{Z_0} > -gZ_0 = h_1(g)
\]  

(2.9)

Case 2. Real eigenvalues and \( g < 0 \).

\[
\frac{R}{Z_0} > 2 + gZ_0 = h_3(g)
\]  

(2.10)
a. Overdamped subregion I.

At most one eigenvalue is positive. Equation (2.11) defines this subregion and (2.12) defines the condition for stability.

\[
\frac{R}{Z_o} > -gZ_o = h_1(g) \tag{2.11}
\]

\[
\frac{R}{Z_o} < -\frac{1}{gZ_o} = h_3(g) \tag{2.12}
\]

b. Overdamped subregion II.

Both eigenvalues are real and at least one of them is positive. This subregion is never stable and is defined by Equation (2.13). Equation (2.14) defines the condition for two positive eigenvalues.

\[
\frac{R}{Z_o} < -gZ_o = h_1(g) \tag{2.13}
\]

\[
\frac{R}{Z_o} < -\frac{1}{gZ_o} = h_3(g) \tag{2.14}
\]

Case 3. Underdamped and \( g > 0 \).

This region is always stable.

\[
h_4(g) = -2 + gZ_o < \frac{R}{Z_o} < 2 + gZ_o = h_2(g) \tag{2.15}
\]
Case 4. Overdamped and $g > 0$

This region is always stable.

$$\frac{R}{Z_o} < -2 + gZ_o = h_4(g) \quad \text{or} \quad \frac{R}{Z_o} > 2 + gZ_o = h_2(g)$$

(2.16)

2.3.3 Stability results

The results of this analysis can be summarized in the stability plane of Figure 2.4.

Fig. 2.4. The stability plane for the second-order circuit model.

The four characteristic equalities $h_i(g)$ are plotted on a dimensionless axis versus $-g$ and the inequality relationships applied to define different regions of clamping and stability. By this approach, the dimensionless quantity $R/Z_0$ becomes a fundamental design parameter and is a horizontal line in the stability plane. Looking at different placements of $R/Z_0$, the performance of a given design can be predicted as a function of the incremental conductance. The derived inequality constraints lead to the following six regions in this stability plane.
Region A. Underdamped and stable - stable foci
Region B. Underdamped and unstable - unstable foci
Region C1. Overdamped and stable - stable nodes
Region C2. Overdamped and unstable - saddle points
Region D1. Overdamped and unstable - saddle points
Region D2. Overdamped and unstable - unstable nodes

2.3.4 A design approach

The stability plane of Figure 2.4 can now be used to design different types of steady state dynamic behavior. This plane has been created irrespective of the $g_{\text{min}}$ value, and large signal behavior can be predicted by looking at placements of $g_{\text{min}}$ relative to the other circuit parameters. The local damping of equilibrium points is predicted by placing this value on the $g$ axis and looking at its location on the $R/Z_0$ line. For stable equilibrium point designs, the local conductance must lie in one of the locally stable regions. For oscillatory designs, the voltage across the negative conductance is going to be varying. In this case, the conductance term will be dynamic. With $R$ and $Z_0$ given, the local stability of both equilibrium and nonequilibrium points is confined to the $R/Z_0$ line. Thus, oscillation quality can be predicted based on location of $g_{\text{min}}$. Different simple modes of operation are now investigated based on the stability plot.

The first type of behavior is the switch mode of operation where the series resistance is chosen greater than the critical value and gives at least one stable equilibrium point for each bias voltage. As the bias voltage is slowly varied back and forth across the nonlinear conductance, the circuit has memory and displays DC hysteresis as shown in Figure 2.5. Although this mode of operation is of least importance in designing oscillators, it is a good beginning since it gives a practical way to develop an estimate of $g_{\text{min}}$. As the series resistance value approaches $R_{\text{critical}}$, the amount of hysteresis will decrease.
The second mode of operation is a single, stable equilibrium point for all bias voltages. This is the mode required for a typical DC characteristic measurement. The first requirement is that $R < R_{\text{critical}}$, which eliminates the $C_2$ and $D_1$ regions (saddle points) of the stability plot from the system dynamics. To obtain globally stable equilibrium points for all $V_{\text{Bias}}$ requires $-g_{\text{min}} < 1/Z_0$ and suggests a selection of $Z_0$. Now with $g_{\text{min}}$ estimated from the hysteresis and $Z_0$ chosen, the $R/Z_0$ ratio is selected to give a globally stable scheme. These ideas are illustrated in Figure 2.6.
The third and fourth modes of operation are steady state autonomous oscillations. The approach used here is to design for a single equilibrium point which is unstable. To obtain a nearly sinusoidal oscillation it becomes intuitive to design the equilibrium point to have underdamped instability and that $g_{\text{min}}$ be limited to underdamped regions. More specifically, as $g$ oscillates along the horizontal $R/Z_0$ line, the linearized eigenvalue (damping) should attain both positive and negative real parts over one cycle of the periodic motion. This means energy is being dissipated and supplied by the device over different times of the oscillation. Also to obtain a nearly sinusoidal oscillation, the imaginary part of the eigenvalues should remain fairly constant over the dynamic range of $g$. By choosing $Z_0$ appropriately, the dynamics of $g$ can be confined from entering the $D_2$ region of the stability plot for a given $g_{\text{min}}$. By a similar argument, $g_{\text{min}}$ needs to be well into the overdamped unstable region for a relaxation oscillation. Figure 2.7 gives a sample design of a nearly sinusoidal oscillator.

![Fig. 2.7. A nearly sinusoidal oscillator design.](image)

The design method presented here can be summarized as follows.

1. Estimate $g_{\text{min}}$ of the nonlinear conductance.
2. Choose the value of $Z_0$ based on the desired dynamic performance.
3. Choose $R/Z_0$ to achieve the correct type of stability.
4. Set $V_{\text{Bias}}$ in the load line diagram to obtain the correct equilibrium point.
5. Frequency and magnitude scale as required.

2.3.5 Notes on the stability plot

Several interesting observations can be made about the stability plot of Figure 2.4. They are listed here since they provide insight into the system behavior.

1. The \( h_1(g) \) line corresponds to the linearized Barkhausen oscillation condition, real part of the eigenvalues is zero.
2. \(-g_{\text{min}}\) less than \(1/Z_0\) is a necessary condition to obtain global stability.
3. \( R/Z_0 \) less than unity is a necessary condition to obtain autonomous oscillation.
4. Regions \( C_2 \) and \( D_1 \) are not important for \( R<\text{critical} \).
5. There exists an upper bound on \( R/Z_0 \) to obtain a single equilibrium point for all bias voltages.
6. The intersection point of \( h_1(g), h_2(g), \) and \( h_3(g) \) is determined solely by \( Z_0 \) and always occurs at the value of one on the vertical axis.
7. By correct selection of parameters, it is possible to obtain autonomous oscillations about the DC hysteresis loop given when \( R>\text{critical} \). This mode requires all three equilibrium points to be unstable.
8. \( R/Z_0 \) represents a stability "load" line which qualitatively characterizes the time varying eigenvalues as a function of incremental conductance. It is important to note that an oscillation which covers the entire negative resistive range passes through \( g_{\text{min}} \) twice per cycle, and in general the range of \( g \) is not symmetric over each half cycle.

2.4 A Third Order Polynomial Example

Consider an n-type nonlinear conductance whose current-voltage characteristic is adequately modeled by Equation (2.17).

\[
I = f(V) = 0.25V^3 - 0.225V^2 + 0.06V
\]  

(2.17)
External device parameters dominate any parasitics and include an inductance of 1uH and a capacitance of 0.1nF. The series resistance is left as a design variable to demonstrate the use of the stability plot.

2.4.1 The stability plot

The first step to analyzing this problem is to generate the stability plot of Figure 2.8 based on the given parameters.

\[ Z_0 = \sqrt{\frac{L}{C}} = 100 \text{ ohm} \]  
\[ g_{\text{min}} = -0.0075 \text{ mho} \]  
\[ V = 0.3 \text{ Volts} \]  

From the stability plane the following observations can be made.

1. By choosing \( R/Z_0 \) between 0.75 and 1.333, global stability is predicted.
2. A relaxation type of oscillation is not expected for any choice of \( R/Z_0 \).
3. Choosing \( R/Z_0 \) less than 0.75 and applying a suitable bias voltage should result in a nearly sinusoidal oscillation.
4. Oscillation amplitude predictions are available in the next chapter.

2.4.2 Simulation results

PSpice is used to show that the stability plot method successfully predicts the circuit dynamics. For the first simulation, \( R/Z_0 \) is chosen to be unity and the bias slowly swept to show that all equilibria are globally stable. The stability is demonstrated by the successful transient mapping of the I-V characteristic in Figure 2.9.
Fig. 2.9. I-V characteristic reproduction with slowly swept bias voltage.

For the second simulation, $R/Z_0$ equals 0.25 and the circuit is held at constant bias to show that a nearly sinusoidal oscillator exists as predicted. This result is shown in Figure 2.10.

Fig. 2.10. Nearly sinusoidal oscillator design results.
2.5 Summary

The results of this chapter show that by using a stability plot approach a straightforward design procedure can be developed for the second-order N-shaped conductance model. It also showed that a straight linearization about the equilibrium points and application of the Barkhausen criterion gives a marginally successful oscillator design at best and is more likely not to work at all. A stability plot approach is far superior.
3. A SECOND-ORDER N-SHAPED CONDUCTANCE: OSCILLATOR

3.1 Introduction

N-shaped conductance circuits make useful autonomous oscillators and can also be locked to a driving source. For autonomous applications, it is important to be able to predict the frequency and amplitude of the oscillation. For nonautonomous applications, it is necessary to predict the required driving amplitude and the frequency range of locking. This work is also a good beginning into the modeling of coupled autonomous oscillators [34] and optically driven oscillators [35, 36, 37, 38].

In the previous chapter, a method for designing a second-order autonomous oscillation was presented, but little information was obtained for its amplitude and frequency. Also, the limit cycle was assumed to be stable. For this unforced circuit, stability is easily argued based on the structure of the I-V characteristic, the load line placement, and the global stability of the system. In this chapter, a mathematical prediction of the amplitude, frequency, and stability of an autonomous oscillation is presented. Also, the nonautonomous oscillator is studied and amplitude and frequency range of locking to the driving source is derived.

3.2 Application of the Harmonic Balance Method

A first-order Harmonic Balance Method (HBM) [31] is applied to predict the existence of limit cycles and their local stability for both the autonomous oscillator and the sinusoidally driven circuit. The unforced circuit is treated as special case where the driving source has zero amplitude. Two circuits of interest are shown in Figures 3.1 and 2. By a source transformation, the two circuits are functionally equivalent after a frequency domain gain normalization and can be studied at the same time. The circuit of Figure 3.1 will be investigated in this chapter. A complimentary method to this approach is presented in a classic paper by Kurokawa [39].
3.2.1 The basics

The state equations for the circuit of Figure 3.1 are given by Equation (3.1).

\[
\begin{align*}
\dot{I}_L &= \frac{1}{L} [V_{\text{Bias}} + V_s - R I_L - V_1] \\
\dot{V}_1 &= \frac{1}{C} [I_L - f(V_1)]
\end{align*}
\]  

(3.1)

where

\[
f(V_1) = \sum_{i=1}^{n} \alpha_i V'_i
\]

(3.2)

Applying a time scaling and change of variable, the normalized circuit equation becomes

\[
\begin{align*}
\frac{dV_X}{dt'} &= V_{\text{Bias}} + V_s - \gamma V_X - V_1 \\
\frac{dV_1}{dt'} &= V_X - Z_0 f(V_1)
\end{align*}
\]

(3.3)

where

\[
t' = \frac{t}{\sqrt{LC}}, \quad Z_0 = \sqrt{\frac{L}{C}}, \quad V_X = Z_0 I_L, \quad \text{and} \quad \gamma = \frac{R}{Z_0}
\]

(3.4)
To apply the first-order HBM, assume $V_x$ and $V_1$ are nearly sinusoidal and adequately represented by Equation (3.5). The coefficients are modeled as slowly time-varying to apply a local stability analysis in the neighborhood of an equilibrium limit cycle.

\[
\begin{align*}
V_1 &= A(t) \cos wt + B(t) \sin wt + C(t) \\
V_x &= D(t) \cos wt + E(t) \sin wt + F(t) \\
V_s &= V_a \cos wt + V_b \sin wt
\end{align*}
\] (3.5)

Substituting Equation (3.5) into (3.3) and gathering orthogonal terms leads to the following set of HBM equations.

\[
\begin{align*}
\dot{D} + \gamma D + wE + A - V_s &= 0 \\
\dot{E} - wD + \gamma E + B - V_b &= 0 \\
\dot{F} + \gamma F + C - V_{Bias} &= 0 \\
\dot{A} - D + wB + Z_0 f_{\cos} &= 0 \\
\dot{B} - E - wA + Z_0 f_{\sin} &= 0 \\
\dot{C} - F + Z_0 f_{\text{const}} &= 0
\end{align*}
\] (3.6)

Here $f_{\cos}$, $f_{\sin}$, and $f_{\text{const}}$ represent the coefficients of cosine, sine, and constants which are present after retaining only the fundamental frequency terms of the nonlinearity response.

3.2.2 Equilibrium solutions

The next step of the HBM is to obtain the equilibrium limit cycle solutions by setting the time derivatives of Equation (3.6) to zero and solving the resulting simultaneous nonlinear equations. The analysis is greatly simplified by letting the voltage of $V_1$ become the phase reference and making $B$ equal to zero. This approach forces the driving voltage to have an unknown phasing which is found by letting $V_b$ become a variable. Now (3.6) can be reduced to the set of three simultaneous nonlinear equations in $A$, $C$ and $V_b$ given by (3.7). $V_a$ and the frequency $\omega$ are specified for the driven case. For the autonomous case, $V_a$ and $V_b$ are zero and the three unknowns are $A$, $C$ and $\omega$. 
For the autonomous oscillation, this system reduces to the set of equations given by Equation (3.8).

\[
\begin{align*}
A(1-w^2) + \gamma Z_0 f_{\text{Cos}} &= V_a \\
-w(\gamma A + Z_0 f_{\text{Cos}}) &= V_b \\
C + \gamma Z_0 f_{\text{Const}} &= V_{\text{Bias}}
\end{align*}
\]  
(3.7)

For the driven circuit, a more useful set of equations is obtained by considering the total driving source amplitude at frequency \( \omega \).

\[
\begin{align*}
\omega^2 &= 1 - \gamma^2 \\
\gamma A + Z_0 f_{\text{Cos}} &= 0 \\
C + \gamma Z_0 f_{\text{Const}} &= V_{\text{Bias}}
\end{align*}
\]  
(3.8a, 3.8b, 3.8c)

With \( B \) equal to zero, expressions for \( f_{\text{Cos}} \) and \( f_{\text{Const}} \) are obtained by applying a Taylor expansion to the polynomial nonlinearity about \( C \).

\[
\begin{align*}
|V_s| &= \left\{ \left[ A(1-w^2) + \gamma Z_0 f_{\text{Cos}} \right]^2 + \left[ -w(\gamma A + Z_0 f_{\text{Cos}}) \right]^2 \right\}^{1/2} \\
C + \gamma Z_0 f_{\text{Const}} &= V_{\text{Bias}} \\
\tan \theta &= \frac{-w(\gamma A + Z_0 f_{\text{Cos}})}{A(1-w^2) + \gamma Z_0 f_{\text{Cos}}}
\end{align*}
\]  
(3.9a, 3.9b, 3.9c)

The equilibrium solutions of the autonomous oscillator are found by substituting the expressions of Equation (3.10) into (3.8). The resultant two nonlinear algebraic equations
in \( A \) and \( C \) give two level curves in the \( A-C \) plane and their intersections are the equilibrium solutions. The frequency \( \omega \) is independent of \( A \) and \( C \).

A similar result is obtained for the nonautonomous oscillator. Substituting Equation (3.10) into (3.9) gives two simultaneous nonlinear equations in \( A \) and \( C \). Equation (3.9b) is independent of \( V \) and frequency, and it is a level curve in the \( A-C \) plane. Equation (3.9a) represents a second level curve in the \( A-C \) plane which is dependent upon \( V \) and frequency. The intersections of the two curves give the equilibrium limit cycles' amplitudes and offsets. Equation (3.9c) determines the phase difference between the driving source and \( V_1 \).

### 3.2.3 Stability of equilibrium limit cycles

To complete the analysis, small perturbations about the equilibrium limit cycles are performed to predict stability. This requires the linearization of the system given by Equation (3.6) at the equilibrium limit cycle of interest denoted by \((A, C)\).

\[
\begin{bmatrix}
-\gamma & -w & 0 & -1 & 0 & 0 \\
-w & -\gamma & 0 & 0 & -1 & 0 \\
0 & 0 & -\gamma & 0 & 0 & -1 \\
1 & 0 & 0 & -Z_0 v_1 & -w & -Z_0 v_2 \\
0 & 1 & -w & -Z_0 u_1 & 0 & 0 \\
0 & 0 & 1 & -Z_0 y_1 & 0 & -Z_0 y_2
\end{bmatrix}
\]  

\((3.11)\)

where

\[
\begin{align*}
\nu_1 &= \frac{df_{\text{Const}}}{dA} \bigg|_{A = A_0, C = C_0} = \frac{df}{dv_1} \bigg|_{V = C_0} + \sum_{i=3, \text{odd}}^{n} i A_0^{-i} \frac{d^i f}{dv_1^i} \bigg|_{V = C_0} \frac{2}{i + 1} \prod_{j=2, \text{even}}^{1} \frac{1}{j^2} \\
\nu_2 &= \frac{df_{\text{Const}}}{dC} \bigg|_{A = A_0, C = C_0} = A_0 \frac{d^2 f}{dv_1^2} \bigg|_{V = C_0} + \sum_{i=3, \text{odd}}^{n} A_0^{-i} \frac{d^{i+1} f}{dv_1^{i+1}} \bigg|_{V = C_0} \frac{2}{i + 1} \prod_{j=2, \text{even}}^{1} \frac{1}{j^2} \\
u_1 &= \frac{df_{\text{Sin}}}{dB} \bigg|_{A = A_0, C = C_0} = \frac{df}{dv_1} \bigg|_{V = C_0} + \sum_{i=3, \text{odd}}^{n} A_0^{-i} \frac{d^i f}{dv_1^i} \bigg|_{V = C_0} \frac{2}{i + 1} \prod_{j=2, \text{even}}^{1} \frac{1}{j^2} \\
\nu_1 &= \frac{df_{\text{Const}}}{dA} \bigg|_{A = A_0, C = C_0} = \sum_{i=2, \text{even}}^{n} i A_0^{-i} \frac{d^i f}{dv_1^i} \bigg|_{V = C_0} \prod_{j=2, \text{even}}^{1} \frac{1}{j^2} \\
u_2 &= \frac{df_{\text{Const}}}{dC} \bigg|_{A = A_0, C = C_0} = \frac{df}{dv_1} \bigg|_{V = C_0} + \sum_{i=2, \text{even}}^{n} A_0^{-i} \frac{d^{i+1} f}{dv_1^{i+1}} \bigg|_{V = C_0} \prod_{j=2, \text{even}}^{1} \frac{1}{j^2}
\end{align*}
\]  

\((3.12)\)
The local stability of an equilibrium limit cycle is found by applying the Routh stability criterion to the characteristic equation of this linearized system. This approach is easily implemented in a spreadsheet and example results given in section 3.5.

3.3 Autonomous Oscillator Results

To fully appreciate the properties of the nonlinear autonomous oscillator, the results of the equilibrium analysis are further investigated. In Equation (3.8a), the expression for \( \omega \) is independent of the nonlinear coefficients. It implies that if the practical oscillation is nearly sinusoidal, then the frequency should be relatively insensitive to small changes in these coefficients. This result is identical to the oscillation frequency obtained from applying the Barkhausen criterion to the linearized small signal model at the DC bias point.

Equations (3.8b) and (3.8c) also give interesting results. Equation (3.8b) represents a constant level curve in the A-C plane and (3.8c) is a level curve which is dependent on \( V_{\text{bias}} \). Their intersections give the possible oscillation amplitudes and dynamic biases. Therefore, the major impact of the nonlinearities will be on the steady state oscillation amplitude and the bias voltage across the nonlinear conductance. Further manipulation of Equation (3.8c) into (3.13) helps in understanding the circuit performance.

\[
\sum_{i=2, \text{even}}^{n} A_i \left. \frac{d f}{d V_i} \right|_{V_C} \prod_{j=2, \text{even}}^{1} \frac{1}{j^2} = \frac{V_{\text{bias}} - C}{Y Z_0} - f(C)
\]  

This equation is interesting because the right hand side is the equilibrium point load line expression of Equation (2.3). So if \( C \) is equal to the DC value obtained by considering the inductor a short circuit and the capacitor an open, \( A \) equal to zero is a solution. If \( C \) is not equal to the DC value, then \( A \) equal to zero is not a solution. In general, these nonlinear expressions in \( A \) and \( C \) will provide more than one solution and the stability analysis must be performed to determine which limit cycles are stable.

This result concerning \( C \) needs to be further analyzed because it has serious implications on the circuit performance and the way we typically perceive oscillations to exist. A simple example is now presented as a vehicle to develop insight into the performance of a more complex I-V characteristic. Consider an \( N \)-type characteristic which is adequately modeled by the third-order polynomial \( (n=3) \) of Equation (3.14).
\[ I = f(V) = \alpha_3 V^3 + \alpha_2 V^2 + \alpha_1 V \]  

(3.14)

In this case, Equation (3.13) can be solved explicitly for \( A \) in terms of \( C \) and Equation (3.8b) provides the second supporting equation.

\[
A^2 = \frac{4 \left[ V_{\text{Bias}} - C \right.}{R} \left. - f(C) \right] \frac{d^2 f}{dV^2}_{v=C}
\]

(3.15)

\[
\gamma + Z_0 \frac{df}{dV}_{v=C} + A^2 \frac{Z_0}{8} \frac{d^3 f}{dV^3}_{v=C} = 0
\]

(3.16)

Several important conclusions can be drawn from Equation (3.15) and are listed here.

1. Under steady state oscillation, the only DC bias point which is equal to \( C \) occurs at the inflection of (3.14) and the amplitude of oscillation is determined by (3.16) evaluated at that bias point.

2. For all other nearly sinusoidal oscillation cases, the right side of Equation (3.15) must be positive. Therefore, the relative position of \( C \) can be understood by looking at the equilibrium point load lines on the characteristic curve as in Figure 3.3. For load lines intersecting the negative resistance region in unstable regions, \( C \) always tends toward the inflection point to satisfy Equation (3.15). In Figure 3.3, \( C_1 \) corresponds to load line 1 and a shift away from the DC equilibrium point is clearly seen. This result is due to the polarity of the curvature of the I-V characteristic for that load line. Load line 2 shows a shift in the other direction. The delta equation in Figure 3.3 is the numerator of Equation 3.15.

So in general, the dynamic bias \( C \) will not be equal to the DC bias point. This effect is referred to as back rectification in [40]. This result is unintuitive based on what is learned in linear circuit and small signal theory. So what does this mean to a circuit designer? I conclude this discussion of the dynamic bias with these points.

1. The equilibrium voltage and currents can never be completely "decoupled" from the dynamic response as in a usual linear method.
2. The stability plot boundaries become slightly fuzzy. To insure stability or instability, the designer should not design right at a boundary as the Barkhausen criterion suggests. An oscillation may exist or take quite a long time to die out because C must go to the equilibrium (nonoscillation) value. If an oscillation is expected, there will be a build-up time in C to achieve the stable oscillation.

3. The dynamic bias exists to satisfy energy balance requirements.

3.4 An Illustrative Example of an Autonomous Oscillator

Recalling the nearly sinusoidal oscillator design from the previous chapter, the following expression in oscillation amplitude, offset, and frequency are obtained from Equation (3.8).

\[
A^2 = -\frac{4}{25} \left( \frac{0.4 - C}{25} - \left( 0.25C^3 - 0.225C^2 + 0.06C \right) \right) \\
0.25A^2 + (C - 0.3)^2 = \frac{1}{150}
\]
Figure 3.4 gives the solution of Equation (3.17) plotted on the same curve as the PSpice simulation. It is evident from this plot that distortion is present but the approximation of a nearly sinusoidal waveform is sufficient. This result further verifies the design methodology presented in the previous chapter. Another interesting result is shown in Figure 3.5. The oscillator circuit is slowly swept by the DC voltage source as was done for the globally stable simulation of Figure (2.9). An interesting artifact is seen in Figure 3.5. The forward and reverse sweeps are different. This is another effect of the dynamic bias. This simulation demonstrates the build-up and wind-down time required for the oscillation to reach steady state. This effect has been misinterpreted as an intrinsic bistability in the characterization of such devices [41]. Other researchers have argued to the contrary [30, 42, 43, 44] but often without strong evidence. Further investigations into predicting this effect in mechanical systems have been done by Bajaj [45].

![Fig. 3.4. Nearly sinusoidal oscillator example.](image-url)
3.5 An Illustrative Example of a Nonautonomous Oscillator

Consider an N-shaped conductance modeled by the cubic expression of Equation (3.18) in the circuit of Figure 3.1. Using the stability plane method of the previous chapter, $Z_0$ equal to 5000 and $R$ equal to 2500 should give a nearly sinusoidal oscillation for the undriven system with $V_{Bias}$ set to zero. This setting of $V_{Bias}$ leads to a load line through the point of symmetry of this conductance and the oscillations of this circuit will have zero DC component. Although this is a special case, the results are sufficient to gain insight into the behavior of the driven dynamics.

$$f(V_1) = 0.0000667V_1^3 - 0.0002V_1$$

(3.18)

For an equilibrium DC component ($C_0$) equal to zero, the equilibrium amplitude of oscillation ($A_0$) can be determined for a given source amplitude ($V_s$) and frequency ($\omega$) from Equation (3.9a). Another approach to the analysis is to plot the required source amplitude at a fixed frequency as a function of equilibrium amplitude using (3.9a). On the same plot, the local stability results obtained from Equation (3.11) can be shown.

Figures 3.6, 3.7, and 3.8 give the results for this example. Similar results are obtained for a microwave system in [39] by an impedance locus approach. As expected, the required driving amplitude goes to zero as the resonant frequency is approached.
Fig. 3.6. Injection locking predictions for $0.10 < \omega < 0.70$.

Fig. 3.7. Injection locking predictions for $0.75 < \omega < 0.95$. 

---

Solid Lines Represent Stable Locking
Fig. 3.8. Injection locking predictions for $1.00<\omega<1.20$.

Figure 3.9 gives another interpretation of the same data. This curve represents the minimum required driving amplitude to obtain injection locking as a function of driving frequency.

![Graph showing required amplitude for locking vs. frequency.](image)

Fig. 3.9. Required amplitude for locking vs. frequency.

An interesting idea based on these curves is an AM signal amplifier. Consider the information waveform at much lower frequency than the carrier. For amplification of the
information signal, look at Figures 3.6, 3.7, and 3.8 to find a frequency curve where Equation (3.19) can be minimized with stable locking. For this circuit, a good choice is a normalized $\omega$ of 1.13 and a zero signal carrier amplitude of approximately 0.7 Volts. The PSpice verification of this idea is presented in Chapter 8. It is mentioned here to show the strength of the HBM.

\[
(gain)^{-1} = \left. \frac{dV_1}{dA} \right|_{A=A_0}
\]  

(3.19)

### 3.6 Summary

The focus of this chapter was to investigate the autonomous and nonautonomous nearly sinusoidal oscillations of a second-order N-shaped conductance circuit and give a method for predicting the existence and stability of equilibrium limit cycles. By applying a first-order Harmonic Balance Method, good predictions were obtained.
4. Experimental N-Shaped Conductance Characterizations

4.1 Introduction

Since a good characterization of an N-shaped device is a fundamental concern to the circuit designer, experimental testing issues need to be addressed. A simple and common lumped circuit approach is to set up a test circuit such as Figure 4.1 and choose R and $Z_0$ to give a single globally stable equilibrium point for the entire range of $V_{Bias}$. The values for steady state current and voltage can be read off the low frequency meters and the DC characterization is obtained. Now with the nonlinearity known, bridge or other convenient AC techniques can be used to approximate L and C. Unfortunately, this scenario is not always feasible. Often the parasitic inductance in the test fixture, wiring, or packaging is large enough to cause an autonomous oscillation. As developed in the previous section, these oscillations usually give rise to dynamic biases which ultimately throw off the characterization attempt.

![Fig. 4.1. Typical I-V characterization circuit.](image)

A solution to this problem, as implied by the stability plots of Chapter 2, is to add capacitance across the nonlinear conductance or reduce the series inductance. By doing so, the value of $Z_0$ is decreased. Historically, engineers have gone to painful extremes to reduce this series inductance [46, 47]. Others have tried mounting the device between capacitive plates to achieve stability. In many test circumstances, the correct nodes are not accessible and series inductance can only be reduced so far. One group has proposed
imbedding the devices in high-order broadband matching networks to squelch the oscillations, but this is clearly not a trivial or flexible approach [48]. A microwave measurement technique has been recently proposed in [49] to extrapolate to the non-oscillatory data. The goal of this chapter is to propose a new characterization method which anticipates the instability problem and makes use of it.

4.2 A Proposed N-Shaped Conductance Characterization Method

Consider using the same circuit configuration as in the simple characterization scheme and add a spectrum analyzer to monitor the voltmeter measurement. Assume if the circuit breaks into an oscillation it is nearly sinusoidal and adequately modeled by \( V = A \cos \omega t + C \). Applying the harmonic balance results to the inductor current of Equation (4.1) gives Equation (4.2) where the current is broken into a time varying component and an average value.

\[
I_L = f(V) + \frac{1}{Z_0} \frac{dV}{dt} \tag{4.1}
\]

\[
I_{AVE} = f(C) + \sum_{i=2, \text{even}}^n A^i \frac{d^i f}{dV^i} \bigg|_C \prod_{j=2, \text{even}}^i \frac{1}{j^2} \tag{4.2a}
\]

\[
I_{AC} = -\frac{wA}{Z_0} \sin \omega t + \left( A \frac{df}{dV} \bigg|_C + \sum_{i=3, \text{odd}}^n A^i \frac{d^i f}{dV^i} \bigg|_C \frac{2}{(i+1)} \prod_{j=2, \text{even}}^i \frac{1}{j^2} \right) \cos \omega t \tag{4.2b}
\]

If there is no oscillation, the measured DC current and voltage are accurate I-V data. When the bias reaches a level to cause oscillation, the current and voltage displayed by the meters no longer give accurate DC data. What I propose is to use the results of the harmonic balance approach to back out a polynomial fit over the unstable region. The current and voltage measured by the low frequency meters are \( I_{AVE} \) and the average voltage \( C \), and the fundamental component of oscillation given by the spectrum analyzer is related to amplitude \( A \). (Of course if the spectrum analyzer shows; the waveform to be highly distorted, the assumption of a nearly sinusoidal voltage is invalid). Therefore, an approach to modeling the unstable negative conductance region is to make \( n \) measurements, where \( n \) is the number of terms in the polynomial fit, and use Equation (4.2a) to obtain a system of linear equations in \( n \) unknowns which yield the polynomial coefficients.
By the substitution theorem [5], a new circuit model can be used to develop the measurement theory needed here. The capacitor and nonlinear resistor can be replaced by an ideal voltage source of $A \cos \omega t + C$ as in Figure 4.2.

Now by linear circuit theory and application of the frequency scaled version of Equation (3.8a), the voltage across the voltmeter is given by

$$V_m = C + \frac{AR}{Z_0} \cos (\omega t + \theta)$$

(4.3)

So if $Z_0$ is known, the amplitude $A$ can be easily calculated from the spectrum analyzer measurement.

The experimental measurement of $Z_0$ is a direct application of Equation (3.8a). Choose two different values of $R$ which will give a single equilibrium point which is unstable ($V_{\text{Bias}}$ will need to be changed to achieve same equilibrium biases) and measure the two different fundamental frequencies with the spectrum analyzer. Then $Z_0$ is found by the following expression.

$$Z_0^2 = \frac{R_1^2 - f_1^2}{f_2^2 - f_1^2} \frac{R_2^2}{1 - \frac{f_1^2}{f_2^2}}$$

(4.4)

4.3 Shortcomings to the Approach

Unfortunately, the inherent oscillations which may be present in the test configuration may not be suitably modeled by the fundamental component and average value alone. In this case, it may be possible to extend this procedure by adding the important higher harmonics, but I leave this effort as a research subject for someone else.
A simple example will now be presented which illustrates the proposed method. An experimental verification can be found in Chapter 11.

### 4.4 An Example by Simulation

Consider again, the example device used in the previous chapters with the following circuit parameters.

\[
I = f(V) = 0.25V^3 - 0.225V^2 + 0.06V
\]

\[
L = 1\mu H
\]

\[
C = 0.1nF
\]

\[
R = 25\Omega
\]

PSpice is used to simulate the results of a practical characterization attempt with an experimental setup of Figure 4.1. Table 4.1 gives the measurements of the DC meter and spectrum analyzer readings obtained under unstable bias conditions.

<table>
<thead>
<tr>
<th>(V_{\text{bias}} ) (Volts)</th>
<th>(V_m ) (Volts)</th>
<th>(I_{\text{Vgs}} ) (mAmps)</th>
<th>(AR/Z_0 ) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35</td>
<td>0.231</td>
<td>4.78</td>
<td>0.0205</td>
</tr>
<tr>
<td>0.36</td>
<td>0.245</td>
<td>4.60</td>
<td>0.0310</td>
</tr>
<tr>
<td>0.38</td>
<td>0.268</td>
<td>4.48</td>
<td>0.0380</td>
</tr>
<tr>
<td>0.41</td>
<td>0.298</td>
<td>4.50</td>
<td>0.0407</td>
</tr>
<tr>
<td>0.44</td>
<td>0.327</td>
<td>4.53</td>
<td>0.0390</td>
</tr>
<tr>
<td>0.47</td>
<td>0.362</td>
<td>4.34</td>
<td>0.0264</td>
</tr>
</tbody>
</table>

Figure 4.3 shows the results of filling in the negative resistance region with the DC meter measurements as typically shown in other works [30, 41, 42]. Now applying Equation (4.2a) and the data of Table 4.1, six simultaneous linear equations are obtained for the polynomial coefficients which model the negative conductance region. The improved characterization obtained by splicing the stable I-V data and the polynomial fit is given in Figure 4.4.
4.5 Summary

In conclusion to this section, I have formulated a procedure to measure I-V curves under a nearly sinusoidal autonomous oscillation. The simulated results demonstrate that the method shows marked improvement over the curves often seen in the literature.
5. NONLINEAR CAPACITANCE IN THE SECOND-ORDER MODEL

5.1 Introduction

In recent resonant tunneling device research, the device capacitance in the second-order N-shaped circuit model is shown to be nonlinear. In [23], the authors showed that the capacitance is more appropriately modeled by a Q-V curve similar to Figure 5.1. In this chapter, the nonlinear capacitance effects are imbedded into the stability plot to analyze its impact on the design of an autonomous oscillator.

![Fig. 5.1. Nonlinear capacitance charge-voltage model.](image)

5.2 The Stability Plot with Nonlinear Capacitance

The goal of this chapter is to include the nonlinear capacitance and maintain the design methodology presented in previous chapters. Analyzing the work in [23], it appears that the nonlinear capacitance can be referenced to the local conductance of the device. By creating a model based on this idea, the goal can be realized. Due to the similarity to the derivation of Chapter 2, a skeleton derivation is presented here.
5.2.1 The nonlinear capacitance model

For this study, the nonlinear capacitance model is chosen to be piecewise-continuous in the Q-V and C-V planes as described by Equation (5.1). By this definition, the peak capacitance value is coincident with \( g_{\text{min}} \).

\[
\text{Region 1. } 0 < V < V_p \quad Q(V) = C_0 V
\]

\[
\text{Region 2. } V_p < V < V_r \quad Q(V) = C_0 \left[ V + \frac{a}{g_{\text{min}}} f(V) \right] - C_0 \frac{a}{g_{\text{min}}} f(V_p), \quad a \geq 0 \quad (5.1)
\]

\[
\text{Region 3. } V > V_r \quad Q(V) = C_0 V + C_0 \frac{a}{g_{\text{min}}} \left[ f(V_r) - f(V_r) \right]
\]

5.2.2 The second-order differential equation model

The state equations of the system become

\[
\frac{dV}{dt'} = Z_0 \frac{1}{1 + \frac{a}{g(V)} \left( I_L - f(V) \right)} \\
\frac{dI_L}{dt'} = \frac{1}{Z_0} \left( V_{\text{Bias}} - I_L R - V \right)
\]

where

\[
t' = \frac{1}{\sqrt{LC_0}} t \quad \text{and} \quad Z_0 = \frac{L}{\sqrt{C_0}} \quad (5.3)
\]

The equilibrium points of this system are found by the same load line approach as given in Chapter 2.

5.2.3 Linearized stability of equilibrium points

Following the perturbation analysis of Chapter 2, the linearized eigenvalues of Equation (5.4) are obtained.
where

\[ g = \frac{df(V)}{dV} \bigg|_{V = \text{Eq. Pt.}} \]  

(5.5)

From this eigenvalue expression, the six regions of stability are defined.

Case 1. Complex eigenvalues and \( g < 0 \)

\[ \frac{R}{Z_0} < \frac{2}{1 + a \frac{g}{g_{\min}}} + \frac{gZ_0}{1 + a \frac{g}{g_{\min}}} = h_2(g) \]  

(5.6)

In this underdamped case, the equilibrium point is locally stable if the real parts of the eigenvalues are negative. The following relationship defines the stable subregion.

\[ \frac{R}{Z_0} > -\frac{gZ_0}{1 + a \frac{g}{g_{\min}}} = h_1(g) \]  

(5.7)

Case 2. Real eigenvalues and \( g < 0 \)

\[ \frac{R}{Z_0} > \frac{2}{1 + a \frac{g}{g_{\min}}} + \frac{gZ_0}{1 + a \frac{g}{g_{\min}}} = h_2(g) \]  

(5.8)
a. Overdamped subregion I

At most, one eigenvalue is positive. Equation (5.9) defines the subregion and (5.10) defines the condition for stability.

\[
\frac{R}{Z_o} > \frac{-gZ_o}{1 + \alpha \frac{g}{g_{\text{min}}}} = h_1(g) \tag{5.9}
\]

\[
\frac{R}{Z_o} < \frac{-1}{gZ_o} = h_3(g) \tag{5.10}
\]

b. Overdamped subregion II

Both eigenvalues are real and at least one of them is positive. This subregion is never stable and is defined by Equation (5.11). Equation (5.12) defines the condition for two positive eigenvalues.

\[
\frac{R}{Z_o} < \frac{-gZ_o}{1 + \alpha \frac{g}{g_{\text{min}}}} = h_1(g) \tag{5.11}
\]

\[
\frac{R}{Z_o} < \frac{-1}{gZ_o} = h_3(g) \tag{5.12}
\]

Case 3. Underdamped and \( g > 0 \)

This region is always stable.

\[
h_4(g) = \frac{-2}{\sqrt{1 + \alpha \frac{g}{g_{\text{min}}}}} + \frac{gZ_o}{1 + \alpha \frac{g}{g_{\text{min}}}} < h_2(g) < \frac{2}{\sqrt{1 + \alpha \frac{g}{g_{\text{min}}}}} + \frac{gZ_o}{1 + \alpha \frac{g}{g_{\text{min}}}} = h_2(g) \tag{5.13}
\]
Case 4. **Overdamped** and \( g > 0 \)

This region is always stable.

\[
\frac{R}{Z_0} < \frac{-2}{\sqrt{1 + a \frac{g}{g_{\text{min}}}}} + \frac{gZ_0}{1 + a \frac{g_{\text{min}}}{g}} = h_4(g) \quad \text{or} \quad \frac{R}{Z_0} > \frac{2}{\sqrt{1 + a \frac{g}{g_{\text{min}}}}} + \frac{gZ_0}{1 + a \frac{g_{\text{min}}}{g}} = h_2(g) \quad (5.14)
\]

### 5.2.4 Stability results

The results of this analysis can be summarized in a stability plane as in Chapter 2. Unfortunately, the value of \( g_{\text{min}} \) becomes a parameter in the expressions and the plane cannot be drawn irrespective of it, but the stability plane is still very valuable to the circuit designer. A typical stability plane is shown in Figure 5.2 and is generated from the example parameters of the next section. The characteristic equalities \( h_i(g) \) are plotted on a dimensionless axis versus \(-g\) and the inequality relationships applied to define different regions of damping and stability (only the negative conductance region is shown). The linear capacitance inequalities are plotted as dotted lines for reference. Again, the dimensionless quantity \( R/Z_0 \) becomes a fundamental design parameter. Notice that the **new characteristic curves** are just deformations of the characteristic lines obtained for the linear capacitance case and all the previous observations and design techniques hold.

![Stability plot with nonlinear capacitance.](image)

Fig. 5.2. Stability plot with nonlinear capacitance.
5.3 A Simulation Example

Consider the nearly sinusoidal oscillator design given in previous chapters.

\[ I = f(V) = 0.25V^3 - 0.225V^2 + 0.06V \]

\[ L = 1\mu\text{H} \]

\[ C_0 = 0.1\text{nF} \]

\[ R = 25\Omega \]

\[ V_{\text{Bias}} = 0.4 \text{ Volts} \]

(5.15)

Now a nonlinear capacitance with peak value of 3C_0 at the g_{\text{min}} voltage is used in the negative conductance region. From the new stability plot of Figure 5.3, it is clear the old design from Chapter 2 does not make a good oscillator. Lowering the series resistance to 10 ohms produces an oscillation. PSpice results concur with these predictions. Figure 5.4 is the PSpice simulation with the new series resistance and \( V_{\text{Bias}} \) adjusted to 0.35 Volts. Notice the large amount of waveform distortion resulting from the nonlinear capacitor.

Fig. 5.3. Stability plot for example design.
5.4 Summary

The results of this section show that a nonlinear capacitance does have a pronounced effect on the stability design method. By realizing the nonlinearity is just a deformation of the typical linear capacitor stability plot curves, a compensation can be made to obtain desired dynamic behavior.
6. A THREE-TERMINAL N-SHAPED CONDUCTANCE DEVICE

6.1 Introduction

In the previous chapters, an investigation of a simple N-shaped conductance was presented. The major difference in this study over previous ones was the use of nonlinear techniques to develop both an analysis and practical design methodology for the two-terminal device. By this approach, insight into the circuit dynamics was developed and novel ideas were proposed. These ideas likely would not have come to light by transient numerical analysis of the circuit. With this background, it is time to look at a new and more complex three-terminal device.

In recent research, three-terminal resonant tunneling devices have become a hot topic. Several authors have published results of transistors with single and multiple negative resistance regions [24, 25, 50, 51]. Proposed applications of these devices include high speed switching and multi-valued logic [24, 25, 50]. Researchers at Purdue have successfully developed a three-terminal resonant tunneling device with characteristics similar to Figure 6.1.

![Three-terminal N-shaped conductance characteristic](image)

Fig. 6.1. Three-terminal N-shaped conductance characteristic.
A device of this general nature is considered throughout the rest of this work. The three-terminals of the device will be referred to as drain, gate, and source due to its similarity to a field-effect transistor. Also, illuminated two-terminal devices as in [35, 36, 37, 38] can be considered a special type of three-terminal device and the methods herein apply.

6.2 A Three-Terminal N-Shaped Conductance Model

To successfully analyze the potential of this device, a mathematical model must be developed. For this study, the model must qualitatively describe the nature of the device and be suitable for circuit simulation. Physics based models have been developed such as [52], but they are relatively unsuitable for a basic circuit simulation. Complex piecewise linear models have been proposed for simulations, but these are destined to convergence problems and are avoided [53, 54] in this study. In this section, a simple macromodel is developed. The model is robust in that the device characteristics are decoupled and easily edited. Also, the new device model has roots in the simple modeling methods used for the two-terminal device.

6.2.1 The mathematical model

In this study, the drain to source current is defined to consist of two components. Maintaining commonality with the two-terminal device, the first component is a function of the drain to source voltage and is modeled by a polynomial expansion. From Figure 6.1, it is apparent that this approach requires the second conductance term to be a nonlinear function of both gate to source and drain to source voltage. This nonlinear transconductance has a maximum value near the negative differential conductance region and monotonically tapers to zero into the positive differential conductance regions. To capture this characteristic, the composite model of Equation (6.1) is selected. By choosing \( f(V_{DS}) \) as a function between 0 and 1, the desired model is obtained. An example \( f(V_{DS}) \) is shown in Figure 6.2.

\[
I_{DS} = \sum_{i=1}^{n} \alpha_i V_{DS}^i + g_m V_{DS} [1 - f(V_{DS})]
\]  

(6.1)
In this model, the transconductance is linear for fixed \( V_{\text{DS}} \). Since a separation of \( V_{\text{GS}} \) and \( V_{\text{DS}} \) in the nonlinear transconductance, the model can be easily changed. In this study, the theoretical results use the linear approximation.

### 6.2.2 PSpice macromodel

For PSpice simulation, a macromodel has been developed to support the proposed mathematical model. Figure 6.3 shows the PSpice functional implementation for this nonlinearity.

To explain the features of the model, it is worthwhile to breakdown the subcircuit listing and discuss the individual pieces. The asterisk lines in the PSpice deck are comments and the functional pieces are identified for the discussion.
* THREE-TERMINAL N-SHAPED CONDUCTANCE SUBCIRCUIT

* SUBCIRCUIT NODE DEFINITION
*  
.subckt gertd 1 1000 2000

* TWO COMPONENT NONLINEAR CONDUCTANCE MODEL
* Drain to Source Polynomial Conductance

g1 1 2000 poly(1) 1 2000 0 -.0002 0.00006667

* Nonlinear Transconductance (Composite Result)

gm 1 2000 poly(2) 1000 2000 32 2000 0.0003322 0 0 -.00047457 0

* NONLINEAR TRANSCONDUCTANCE MODEL ARCHITECTURE
*  
* Voltage corresponding to maximum gm placement
vx 200 2000 0

* Functional Block 1 - Generates the low end clamping of $g(V_{DD})$ by looking at the
* currents flowing through the dummy zero volt sources. The polarity of the
* sources
* is switched to obtain an absolute value function. In this example, the nonlinear
* conductance sources defining the outer slopes are diodes. Polynomial sources
* could also be used. Also the outer slopes are separated to allow individual control.
* Resistor $r_P$ can be varied to control the window of the lower saturation.

ga 2000 21 poly(2) 1 2000 200 2000 0 1 -1
rp 21 2000.4
d1 21 22 dlnxxx1
.model dlnxxx1 d (is=1e-14 n=1)
v+ 22 2000 0
d2 23 21 dlnxxx2
.model dlnxxx2 d (is=1e-14 n=1)
v- 2000 23 0
Functional Block 2 - This block generates the upper clamping characteristic of the \( f(V_{DS}) \).

\begin{verbatim}
  h1 31 2000 poly(2) v+ v- 0 1 1
  rd 31 32 100
  d3 32 2000 d1nxxx3
  .model d1nxxx3 d (is=1e-14 n=1)
  .ends
\end{verbatim}

Figure 6.4 demonstrates an I-V characteristic generated with the example parameters in the PSpice deck.

6.3 Translation of the Origin in the I-V Characteristic

In later chapters, many three-terminal N-shaped device examples are referenced to the origin of the \( I_{DS} - V_{DS} \) plane. Specifically, the NDC region of the \( I_{DS} - V_{DS} \) trace with \( V_{GS} \) equal to zero passes through the origin. There is no loss in generality with this approach since the origin can be translated anywhere in the plane [31].

This origin translation should not be confused with linear superposition approaches. In linear circuits, the translation usually corresponds to removing a DC component, computing the AC component, and determining the overall circuit response by adding the two. For nonlinear circuits in this study, this translation corresponds to separating the
equilibrium behavior from the dynamic behavior. Since superposition does not hold for general nonlinear circuits, assuming equilibrium solutions are DC components can lead to erroneous characteristics. As an example, recall the problems with measuring I-V characteristics of the two-terminal device.

6.4 Research Work on the Three-Terminal Device

In the following chapters, this new device will be analyzed for success in switching configurations and looked at as a potential chaos modulator. It will be shown that these two vastly different applications will tie together more tightly than may be expected. To begin the study, a method for predicting and comparing switching speeds is developed. Next, a look is taken at injection locking since digital switching falls under this domain. I have hypothesized that such a device might give a good practical implementation of chaos and a design method is developed and simulation and experimental verification is obtained. Injection locking is then reviewed in the context of the chaos results; Finally, a figure of merit is developed to predict if a device is suitable for a given chaos synthesis.

6.5 Summary

The purpose of this chapter was to introduce the three-terminal device and demonstrate that a suitable model for basic circuit simulation has been developed. Although this model is not adequate or accurate for production designs or exact modeling, it captures the qualitative behavior of these devices and allows for a circuit theoretic investigation.
7. A THREE-TERMINAL N-SHAPED CONDUCTANCE DEVICE AND SWITCHING

7.1 Introduction

Currently, three-terminal N-shaped conductances are being fabricated and much has been speculated concerning high speed switching and logic applications [24, 25, 50, 51]. In these works, the $g_{m}/C$ usually quoted for transistors seems to be the standard figure of merit for speed predictions. Unfortunately, this figure ignores the added benefit of the conductance nonlinearity. In this chapter, the switching behavior of these devices is investigated and new figure of merit is proposed. This new figure retains the $g_{m}/C$ ratio and adds an improvement factor dependent only on the nonlinear conductance.

7.2 Basic MOSFET Switching - A Review

Transistor switching circuits have been studied extensively [4]. By approximating the dynamic models as first-order networks, a separation of variable integration method is often used to predict switching times and to obtain "rule of thumb" figures of merit from the nonlinear characteristics and external circuit parameters. Another common method is to look at the linearized small signal model and develop figures of merit based on the optimum device frequency response. This approach is useful because it allows the device speed potential to be defined independent of external parameters. In this section, the frequency response method is investigated and a justification given to show why $g_{m}/C$ is a widely used figure of merit for high speed MOS transistors. Also, a separation of variable method is given for a simple resistor-transistor-logic (RTL) configuration to show the $g_{m}/C$ ratio is important there also.

Consider the capacitance loaded RTL circuit in Figure 7.1 and its Taylor expansion model in Figure 7.2. In this case, the MOSFET will be studied in its saturation region since this is where the best switching performance is obtained. The Taylor expansion will be considered about the two stable operating points denoted in the load line diagram of
Figure 7.3. This model has two transconductance terms, linear and nonlinear, due to the quadratic gate dependence of the MOSFET in the saturation region. The effect of the nonlinear transconductance is a nonsymmetric switching waveform.

Fig. 7.1. Capacitance loaded RTL model.

Fig. 7.2. Nonlinear small signal model from Taylor expansion.

Fig. 7.3. Load line diagram of RTL switching circuit.

For this analysis, the higher order conductance term and the gate to drain feedback capacitor are considered negligible. The Taylor model becomes the usual small signal
linearized model [13] and three expressions are obtained which describe the circuit performance.

\[
\begin{align*}
\text{DC Gain} & = H(0) = -g_m R \\
\text{Time Constant} & = \tau = RC \\
\frac{|H(0)|}{\tau} & = \frac{g_m}{C}
\end{align*}
\] (7.1)

From this development, the gain to time constant ratio becomes an important parameter. Notice that the time constant is decreased (bandwidth increased) by lowering the gain. For switching circuits where gates are loaded by similar gates, the minimum gain of consideration is unity; thus, a minimum time constant (maximum bandwidth) is given by:

\[
\tau_1 = \frac{C}{g_m}
\] (7.2)

The value of \(\tau_1\) corresponds to the time it takes the output of the small signal circuit to attain 63.21% of the step magnitude applied at the gate.

This approach only tells half the story, switching times are also dictated by slew rates. Consider again the linearized small signal circuit, the best possible performance is obtained when the load resistor is infinite. For this case, all current supplied by the transconductance goes to charge and discharge the load capacitance. So a design which couples a larger gain with a more moderate time constant can produce better results.

For a gain much greater than one, the approximate transfer function for small output voltages is given by Equation (7.3).

\[
\frac{\Delta V_{ds}}{\Delta V_{gs}} = -g_m R \frac{t}{\tau} = -\frac{g_m}{C} t
\] (7.3)

This circuit gets to the same logic threshold faster than the unity gain design since the load resistor is effectively ignored over the dynamic range of the switch. For a practical MOS RTL inverter, this leads to operation in the ohmic region and a more complicated analysis must be considered.
For the large signal RTL analysis, consider switching from a logic high to logic low at the output. At the time of switching the initial change in capacitor voltage can be calculated and is given by Equation (7.4). Again $g_m/C$ surfaces as a speed factor.

\[
\frac{dV_{DS}}{dt} = -\frac{k}{2} \frac{(V_{GS} - V_T)^2}{C} = -\frac{1}{2} \frac{g_m}{C} (V_{GS} - V_T)
\]  

(7.4)

This brief analysis demonstrates that the $g_m/C$ ratio represents a reasonable figure of merit for MOS transistors in switching applications regardless of the analysis approach.

7.3 The Benefit of A Circuit with Negative Conductance

Consider the circuit model of Figure 7.4. This circuit contains a linear negative conductance $g$, and better switching times are available since the negative conductance supplies an extra charge and discharge current component to the load capacitor. The overall response of this linear circuit is unbounded and does not represent a practical case since all physical devices are eventually passive [5], but important information is obtained by studying it.

![Fig. 7.4. Switching circuit with negative conductance.](image)

As a switching speed figure of merit, one can use the time required for the output of this circuit to give a voltage change of $AV$ where $AV$ is the magnitude of a voltage step applied to the circuit input. This switching time is given by Equation (7.5). It monotonically decreases from $C/g_m$ as the conductance goes more negative.

\[
t_s = \frac{C}{|g|} \ln \left(1 + \frac{|g|}{g_m}\right)
\]  

(7.5)
7.4 A Real Device with a Negative Differential Conductance Region

Since the N-shaped device has a negative conductance region and is eventually passive, it makes a good candidate for investigating the effects, a practical negative differential conductance device can have on switching performance. In the previous sections, the switched MOS device was analyzed in the saturation region. This approach was chosen since the three-terminal N-shaped device is going to contribute an enhancement to the MOS saturation behavior.

The first switching method to consider is a non-hysteresis switch where the static load line gives a single equilibrium point for all biases. This type of switching gives little advantage over the RTL MOS configuration since there is still a net positive resistance over the entire switching range. It does offer a slightly better performance than a unity gain RTL MOS inverter and may be useful to help combat Miller effect capacitance, but this realization method is no longer pursued here due to its limited improvement potential.

The second switching method involves manipulating the device about its load line and causing the system to undergo a bifurcation [55]. Consider the load line diagram of Figure 7.5. Assume the $V_{GS}$ setting gives the upper I-V characteristic. From the results of Chapter 2, the two outer load line intersections are the stable equilibria. To set up the switching example, let the left equilibria be the operating point. Now apply a change in $V_{GS}$ to give the lower I-V trace. This results in only one equilibrium point and the circuit must switch to it. Since the device transverses the NDC region it may be possible to obtain high switching speeds.

![Figure 7.5. The proposed switching configuration.](image)
A practical problem with this simple design is hysteresis. But since the main goal of this chapter is to give a way to compare speeds of similar devices, so I am defining performance based on this threshold switching analysis. This method allows the development of a performance figure which may be obtainable with a proper circuit configuration. Extensions of the work in [56] have been suggested by Dr. Janes as a possibility. Another potential application might be a high speed triggering circuit.

The circuit of Figure 7.6 is used in the development of the switching figure of merit. Again the circuit is in a common source configuration, but it is biased with a high impedance current source. The nonlinear device is broken into its two current components. The current source value is chosen to be negligibly less than the peak current value as depicted in Figure 7.5. Now the circuit can be analyzed for a high to low transition at the gate and the switching time predicted based on a piecewise linear model [17]. To begin the analysis, a few definitions must be made.

1. The average conductance from $V_1$ to $V_2$ is defined as

$$g_{ave} = \frac{1}{V_2 - V_1} \int_{V_1}^{V_2} \frac{dI}{dV} dV = \frac{I(V_2) - I(V_1)}{V_2 - V_1}$$ \hspace{1cm} (7.6)

2. The logic low and logic high levels are $V_p$ and $V_v$ as designated on Figure 7.5.
3. Over the range from $V_p$ to $V_v$, the conductance current is adequately modeled by a single piecewise linear segment.
4. Over the switching range of interest, the device transconductance is approximated as linear and denoted by \( g_m \).

Based on these assertions, an expression for the low to high switching time is obtained in Equation (7.7).

\[
   t_s = \frac{C}{g_m} \ln \left( 1 + \frac{I_p - I_v}{g_m \Delta V_{gs}} \right)
\]

(7.7)

In the limit as the second term in the natural log expression goes to zero, Equation (7.7) is equivalent to Equation (7.3). Now to define a more compact figure of merit, define the gate driving range to be exactly the digital noise margin, \( V_c - V_f \). The result for the switching time now becomes identical to Equation (7.5).

Equation (7.5) needs to be manipulated a little more to develop a feel for its performance predicting capability.

Define \( \alpha = \frac{|g_{ave}|}{g_m} \)

then

\[
   t_s = \frac{C}{g_m} \left[ \frac{1}{\alpha} \ln (1 + \alpha) \right]
\]

(7.8)

This result shows that the capacitance and transconductance set a baseline speed for the device, but improvements can be made by having an average conductance much larger than the transconductance. This threshold switching speed now can be used as a figure of merit since all the improvement parameters are easily taken from the static I-V characteristic.

Three more important results should also be mentioned here. Miller capacitance is always an issue in this design configuration. From the Miller approximation, an expression for the input capacitance becomes

\[
   C_m = C_f \left( 1 - \frac{1}{\alpha} \right), \quad \alpha > 1
\]

(7.9)
For a \( a \gg 1 \), the Miller capacitance effect is negligible. This result corresponds to the desired condition for good switching performance. Also for a practical design the value of \( g_m \), the noise margin, and the setting of the current supply are related and tradeoffs will be made which may degrade the switching performance. Lastly, the estimate of a linear transconductance gives a best possible switching speed if the maximum value over the switching range is chosen. Overall, this method and result give a reasonable way to compare similar devices and is dependent only on intrinsic properties of the devices.

### 7.5 An Alternative Method for Figure of Merit

For devices with very steep negative resistance regions and nonsymmetric structure about their inflection voltage, a second approach to determining speed may be useful. Consider modeling the negative conductance region as a switched constant current source with value of peak current for voltage less the inflection voltage and valley current for voltage greater than inflection voltage. Now applying the same approach as outlined in the previous section, the threshold switching time from peak to valley voltage is given by (7.10).

\[
t_s = \frac{C}{g_m} \left[ \frac{1 + \beta \alpha}{1 + \alpha} \right]
\]  

(7.10)

where

\[
\alpha = \frac{|g_{sve}|}{g_m} \quad \text{and} \quad \beta = \frac{V_l - V_p}{V_v - V_p}
\]  

(7.11)

Of course this result is very similar to Equation (7.8) and begs the question of what the relationship between the two are. An answer is obtained by looking at the ratio of the two results as given by Equation (7.12). The extra subscripts on the switching times denote method one and method two in order of their presentation.
\[ t_{s1} = \frac{(1 + \alpha) \ln(1 + \alpha)}{\alpha(1 + \beta \alpha)} \]

(7.12)

and \( \frac{t_{s1}}{t_{s2}} > 1 \) for \( \beta < \frac{(1 + \alpha) \ln(1 + \alpha) - \alpha}{\alpha^2} \)

By plotting the function of \( \alpha \) in Equation (7.12), the relationship of the switch times is known for a given \( \beta \). Figure 7.7 shows the graphical result.

Fig. 7.7. Relationship between switching time predictions

7.6 Simulation Examples

Consider a three-terminal device described by Equation (7.13) used in the common source configuration. The current-voltage characteristic is shown in Figure 7.8.

\[ I_{DS} = 0.25V_{DS}^3 - 0.225V_{DS}^2 + 0.06V_{DS} + 0.000625V_{GS} \]

(7.13)

From the proposed methods, the following switching parameters are calculated.

\[ |g_{sve}| = 0.005 \quad \alpha = 8 \quad \beta = 0.5 \]

(7.14)

The load capacitance in this simulation is \( C=1\text{nF} \), giving the \( C/g_m \) ratio of 1.6us. The first estimate predicts a switching speed of 440ns. The second method gives 888ns. From the
PSpice simulation of Figure 7.9, the actual switching time is approximately \textbf{550ns}. This result verifies that the methods presented here do give insight into the switching performance of a given device and shows the improvements realized by the addition of a negative conductance region.

Fig. 7.8. Example device I-V characteristic.

Fig. 7.9. Simulated switching time for example circuit.
7.7 Application to a Real Device

In this section, the estimate methods are applied to the devices presented in a recent research work [25]. From Figure 4 of [25], the parameter estimates of (7.15) are obtained.

\[ |g_{sc}| = 125 \mu \text{mho} \quad g_m = 20 \mu \text{mho} \quad \beta = 0.258 \quad (7.15) \]

This leads to the following switching predictions for the device.

\[ t_{ni} = \frac{1}{3.16 g_m} C \quad t_{so} = \frac{1}{2.77 g_m} C \quad (7.16) \]

From these results, a switching speed improvement of approximately 3 should be obtained over a MOS device with an identical $C/g_m$ ratio.

7.8 Summary

The goal of this chapter was to develop a figure of merit for the switching capabilities of the three-terminal N-shaped conductance. The proposed methods lead to performance figures which can be directly compared to the figure of merit used for MOS transistors.
8. A THREE-TERMINAL N-SHAPED CONDUCTANCE DEVICE AND A THIRD-ORDER CIRCUIT MODEL

8.1 Introduction

In the previous chapter, a first-order model was studied to predict potential switching speed improvements with a three-terminal N-shaped device. This simplified circuit gave figures for comparison purposes, but it may not be sufficient for predicting the true dynamic circuit response. In this chapter, the driven response of the third-order circuit in Figure 8.1 is investigated. This circuit is chosen because it is a model which naturally arises from recently proposed logic designs [24]. It is shown that this model is not a trivial extension of the second-order circuit of Chapter 3. The theoretical development is parallel to the approach in Chapter 3 and a skeleton derivation is presented.

Fig. 8.1. Third-order circuit model.
8.2 The Normalized Circuit Model

In this chapter, the device transconductance is modeled as linear and the simplified circuit of Figure 8.2 is studied.

The following normalized state equations for this model are

\[
\begin{align*}
\dot{V}_x &= -\beta_0 V_x - \gamma V_1 + \gamma V_2 \\
\dot{V}_1 &= \alpha_0 V_x - \alpha_0 R_1 f(V_1) - \alpha R_1 I_s \\
\dot{V}_2 &= -V_x + V_{Bias} - V_2 \\
\end{align*}
\]  

(8.1)

where

\[
\gamma = \frac{R_1^2 C_2}{L}, \quad \beta = \frac{R_2}{R_1}, \quad \alpha = \frac{C_2}{C_1}, \quad t' = \frac{t}{R_1 C_2}
\]

\[
f(V_1) = \sum_{i=1}^{n} \alpha_i V_i'
\]

(8.2)

\[
I_s = I_0 \cos \omega t + I_0 \sin \omega t
\]
8.3 Application of a Harmonic Balance Technique

The approximation of a nearly sinusoidal response to a driving sinusoid is made and the Harmonic Balance Method (HBM) is applied.

\[
\begin{align*}
V_1 &= A \cos \omega t + B \sin \omega t + C \\
V_2 &= D \cos \omega t + E \sin \omega t + F \\
V_x &= G \cos \omega t + H \sin \omega t + J
\end{align*}
\]  

(8.3)

8.3.1 Results of the HBM

Since there are three state variables, the HBM leads to the set of nine coupled first-order differential equations in Equation (8.4).

\[
\begin{align*}
\dot{A} &= -\beta \gamma H + wG + \gamma E - \gamma B \\
\dot{B} &= -wH - \beta \gamma G + \gamma D - \gamma A \\
\dot{C} &= -\beta \gamma J + \gamma F - \gamma C \\
\dot{D} &= -H - E + wD \\
\dot{E} &= -G - wE - D \\
\dot{F} &= -J - F + V_{\text{bias}} \\
\dot{I}_1 &= \alpha H + wA - \alpha R_1 f_{\text{sin}} - \alpha R_1 I_2 \\
\dot{I}_2 &= \alpha G - wB - \alpha R_1 f_{\text{cos}} - \alpha R_1 I_1 \\
\dot{C} &= \alpha J - \alpha R_1 f_{\text{const}}
\end{align*}
\]  

(8.4)

where \( f_{\text{cos}}, f_{\text{sin}}, \) and \( f_{\text{const}} \) are the coefficients of cosine, sine, and constants present after retaining only the fundamental frequency and constant terms of the response.

8.3.2 Equilibrium limit cycle solutions

By setting the time derivatives equal to zero, a set of nonlinear simultaneous equations give the equilibrium solutions. The method of setting \( B=0 \) is used again here and the system is reduced to three nonlinear equations in \( A, C, \) and \( I_2. \)
\begin{align*}
I_1 &= -f_{\cos} \left( \frac{bc+d}{ac+e} \right) A \\
I_2 &= \left( \frac{be-ad}{ac+e} \right) A \\
R_1(1+\beta)f_{\text{const}} + C &= V_{\text{bias}}
\end{align*}

Or using the magnitude and phase of driving current gives Equation (8.6).

\begin{align*}
|I_s| &= \left[ \left( A \left( \frac{bc+d}{ac+e} \right) + f_{\cos} \right)^2 + A^2 \left( \frac{be-ad}{ac+e} \right)^2 \right]^{1/2} \\
R_1(1+\beta)f_{\text{const}} + C &= V_{\text{bias}} \\
\tan \theta &= \frac{A \left( \frac{be-ad}{ac+e} \right)}{-f_{\cos} - A \left( \frac{bc+d}{ac+e} \right)}
\end{align*}

where

\begin{align*}
a &= -\left( \frac{\beta \gamma (1+w^2)+\gamma}{w(1+w^2-\gamma)} \right) , \\
b &= -\left[ \frac{(\alpha \gamma - w^2)(1+w^2)+\gamma w^2}{\alpha wR_1(1+w^2-\gamma)} \right] \\
c &= \gamma R_1 \frac{\beta(1+w^2)+1}{1+w^2} , \\
d &= -\frac{\gamma w}{\alpha} \frac{\beta(1+w^2)+1}{1+w^2} , \\
e &= -wR_1 \left( \frac{1+w^2-\gamma}{1+w^2} \right)
\end{align*}

and

\begin{align*}
f_{\cos} &= A \left. \frac{df}{dV} \right|_{V=C} + \sum_{i=3, \text{odds}}^n A_i \left. \frac{df}{dV} \right|_{V=C} + \frac{2}{i+1} \prod_{j=2, \text{evens}}^{i-1} \frac{1}{j^2} \\
f_{\text{const}} &= f(C) + \sum_{i=2, \text{evens}}^n A_i \left. \frac{df}{dV} \right|_{V=C} \prod_{j=2, \text{evens}}^i \frac{1}{j^2}
\end{align*}
8.3.3 Stability of equilibrium limit cycles

By linearizing the system given by Equation (8.4) about equilibrium solutions, the local stability of the individual limit cycles can be determined. The linearized ninth-order system is given by Equation (8.9).

\[
\begin{align*}
\dot{x} &= \begin{bmatrix}
-w & -\beta y & 0 & 0 & \gamma & 0 & 0 & -\gamma & 0 & 0 \\
-\beta y & -w & 0 & 0 & \gamma & 0 & 0 & -\gamma & 0 & 0 \\
0 & 0 & -\beta y & -w & 0 & 0 & 0 & 0 & -\gamma & 0 \\
-1 & 0 & 0 & -1 & w & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix} x
\end{align*}
\]

where, as defined in Chapter 3,

\[
\begin{align*}
u &= \left. \frac{df_{\text{Sui}}}{dB} \right|_{A=A_0} C=C_0, \\
\nu_1 &= \left. \frac{df_{\text{Cos}}}{dA} \right|_{A=A_0} C=C_0, \\
\nu_2 &= \left. \frac{df_{\text{Cos}}}{dC} \right|_{A=A_0} C=C_0, \\
y_1 &= \left. \frac{df_{\text{Cont}}}{dA} \right|_{A=A_0} C=C_0, \\
y_2 &= \left. \frac{df_{\text{Cont}}}{dC} \right|_{A=A_0} C=C_0.
\end{align*}
\]

8.4 The Autonomous Circuit - Zero Driving Current

A special case of the third-order circuit is with the independent current source of Figure 8.2 set to zero. In Chapter 2, it was shown that the dynamics of the autonomous second-order circuit could be satisfactorily predicted based on the stability plot. With the third-order circuit, this approach is not sufficient. Consider the load line placement in Figure 8.3. In the second-order circuit of Figure 8.4a with \(R/Z_0\) greater than one, the outer equilibria were asymptotically stable and the inner equilibria was a saddle point. For all initial conditions, the circuit will reach a steady state condition at one of the stable equilibrium points. All equilibrium limit cycles can be shown to be unstable by the results of Chapter 3.
Linear circuit intuition would imply that adding a passive, linear capacitance as shown in Figure 8.4b should not change the second-order stability result. In the nonlinear circuit, this is true only for small perturbations about the stable equilibrium point. For a large perturbation, the system goes into a stable steady state oscillation. Thus, there is simultaneous existence of two locally stable equilibrium point solutions and a locally stable limit cycle solution.
8.4.1 An autonomous example

To demonstrate this proposed operation, a simulation is given. Let the drain to source conductance characteristic of the example device with grounded gate be described by

\[ I_{DS} = 0.0000667V_{DS}^3 - 0.0002V_{DS} \]  \hspace{1cm} (8.11)

Now choose a second-order circuit design with component values; as shown in Figure 8.5a. The autonomous oscillation results of Chapter 3 predicts no stable limit cycles for this selection of parameters. Thus, all initial conditions will lead to a final position at one of the outer equilibrium points.

Adding a capacitor to this circuit as shown in Figure 8.5b changes the dynamic behavior. The outer equilibria are still locally stable, but for a large perturbation the circuit breaks into a stable steady state oscillation. For this circuit, the dynamics will lead to a stable equilibrium for a capacitance less than about 1nF. PSpice simulations for a load capacitance of 4nF is given in Figure 8.6. The only difference between the two responses is the initial condition of the inductor current. This result verifies that the load capacitance on proposed switching circuit designs may lead to problems other than just decreased switching speeds.
8.4.2 Predicting a true steady state equilibrium point

If this circuit model serves as an adequate parasitic model of the basic switching circuit, it becomes a practical requirement to predict the existence of stable limit cycles since they could lead to faulty operation. The objective of this short section is to propose a method for determining an acceptable capacitance ratio that allows the circuit to settle to a stable equilibrium point.

Consider Equation (8.5) for the autonomous case. The equilibrium values of $A$, $C$, and $\omega$ can be calculated as a function of the capacitance ratio. Now substituting these functions into Equation (8.9), the characteristic equation of the linearized oscillating system can be found. Applying the Routh criterion, the stability of equilibrium limit cycles can be determined as a function of capacitance ratio. In theory, this is a good approach but practically it is difficult. Given the high order of the characteristic equation and the possibly large number of terms in the nonlinear model, a better approach is to use a computer algorithm which tests different capacitance ratios based on the Routh criterion and converges to the limiting values.

8.5 An Illustrative Example of the Non-Autonomous System

Consider the three-terminal N-shaped conductance modeled by the expression of Equation (8.12) used in the circuit of Figure 8.1 with system parameters given by (8.13).
For the given parameter values, a set of fixed frequency oscillation amplitude curves similar to those of Chapter 3 can be generated.

In Chapter 3, an AM amplifier example was given based on the stable oscillation curves. The proposed approach was to find a fixed frequency curve where Equation (8.14) can be minimized and a stable limit cycle exists.

\[
\alpha = 1.37 \ , \ \beta = 0.000171 \ , \ \gamma = 2318 \ , \ R_i = 238600
\]  
(8.13)

\[
f(V_{DS}, V_{GS}) = 0.0000667V_{DS}^3 - 0.0002V_{DS} + 0.0003322V_{GS}
\]  
(8.12)

Figure 8.7 shows an appropriate choice of fixed frequency curve for the given system and the AM amplifier design. From this curve, zero-signal modulation voltage applied to the gate should be \(660\text{mV}\) at a normalized frequency \(\omega=15\). The input and output voltages for zero information signal is given in Figure 8.8 for reference purposes. The top trace is the input and the lower trace is the output signal.

\[
(gain)^{-1} = \frac{dV_s}{dA}\bigg|_{A=A_0}
\]  
(8.14)

**Fig. 8.7.** Fixed frequency curve for AM amplifier example.
An information signal amplitude of 6.6mV is chosen for this simulation giving a modulation index of 1%. Figure 8.9 shows the input and output signals from the PSpice simulation. The new modulation index of the output signal is approximately 7%. This simulation verifies the conjectures based on the HBM results are true.
8.6 Summary

The goal of this chapter was to demonstrate a method for predicting stable limit cycles in a practical third-order configuration of the gate-controlled N-shaped conductance device. A major result of this analysis is the nonintuitive simultaneous existence of locally stable equilibria and locally stable limit cycles.
9. A THREE-TERMINAL N-SHAPED CONDUCTANCE AND CHAOS

9.1 Introduction

Since the discovery of Chua's circuit in 1983 [57], chaos has been a hot topic in the electronics research literature [58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68]. Until this discovery, deterministic chaos was widely considered a bizarre phenomenon existing in numerical simulations. The dynamics of this new circuit verified that relatively simple physical systems could be found which exhibit chaos. Many researchers have since analyzed this circuit to demonstrate several chaotic attractors [58, 59, 61, 63]. In [59, 60], Chua's circuit is extended to Chua's oscillator which exhibits an even larger collection of chaotic attractors. In fact, [59, 60] generalize Chua's oscillator to encompass a large class of third-order circuits containing an odd-symmetric piecewise-linear conductance. In this chapter, these results are applied and extended to investigate the advantages of using a three-terminal N-shaped conductance device.

9.1.1 Chua's circuit

Chua's circuit is shown in Figure 9.1, and the current-voltage characteristic of the nonlinear resistor (Chua's diode) is given in Figure 9.2. An important characteristic of Chua's diode is its symmetry. Notice for a load line drawn through the origin, there exists either one or three equilibrium points. In both cases, the origin is an equilibrium point. For the case of three equilibria, the circuit has two outer equilibrium points with identical linearized small signal dynamics. All other Chua circuit components are linear, but they are often allowed to take negative values in the research literature [58, 59, 60]. It is important to note that Chua's circuit is a physical nonlinear system which exhibits chaos. It is not an analog computer implementation of a set of mathematical equations which exhibit chaos [58].
9.1.2 Chua's oscillator

Chua's oscillator is created by adding a series resistor to the inductance. Not only does it account for the stray inductor resistance, it plays an important role in the circuit dynamics and leads to a larger collection of chaotic attractors [61]. Also, the shape of the nonlinearity is generalized in the Chua oscillator [61]. The nonlinearity is still defined by an odd-symmetric piecewise-linear curve, but the local conductance is allowed to be of either polarity in the inner and outer sections. Most chaotic electronics researchers, including Chua's group at Berkele, now use the Chua oscillator for their study [60].

9.1.3 Proposed applications of chaos

Along with the research into practical chaos came the fundamental question: How is it useful? One interesting possibility is to use chaotic modulators for secure communications [58, 69, 70]. For this application to be viable, a practical modulator circuit must be designed. The Chua oscillator has been heavily researched, but many of its
chaotic configurations require both a Chua diode and active linear components. From a modeling standpoint, this is unimportant; but practically, this result is undesirable. Therefore, a practical chaotic modulator circuit would be a significant contribution to the secure communications effort.

Currently, a Colpitts oscillator configuration is being studied as a potential chaos generator [71, 72, 73]. A very important detail not discussed in these works is that the linear components of the example designs are passive. An interesting question to ponder is whether or not this is a result of negative feedback. Feedback has been suggested as a method for controlling or stopping chaos in [67, 68], but not investigated for synthesizing chaos with three-terminal devices. In this chapter, it will be verified that adding negative feedback can lead to more practical circuit designs.

### 9.1.4 Three-terminal N-shaped conductance and practical chaos design

Given the characteristics of the three-terminal N-shaped conductance, it is logical to consider it a candidate for chaotic modulation applications. For constant gate to source voltage, the nonlinearity is similar to a Chua diode with an offset point of symmetry. The addition of the third terminal allows for feedback designs. In this chapter, a simple feedback circuit configuration is investigated to determine if the three-terminal device has practical advantages over the two-terminal device.

### 9.2 Chua’s Oscillator and Linearly Equivalent Circuits

As mentioned, Chua’s oscillator was shown to be equivalent to a large class of third-order circuits with a single odd-symmetric, piecewise-linear, conductive element in [60]. In [59, 60, 62], several of these circuit configurations are documented. The basic result of these works is that equivalent dynamic results can be obtained in two linearly equivalent circuits by matching eigenvalues at their inner and outer equilibrium points. So by studying only one configuration, the dynamics of many other topologies can be qualitatively predicted via a mapping.

A significant extension to this mapping approach was presented in [73]. In his work, Kennedy gives a set of circuit parameters which causes the Colpitts oscillator to be chaotic. By considering the linearized eigenvalues of both the equilibrium point and a virtual equilibrium point of the Colpitts oscillator, he successfully mapped it to a Chua oscillator containing an asymmetric piecewise-linear conductance and obtained equivalent chaotic dynamics.
Since a wealth of parameters and chaotic attractors have been gathered for the Chua oscillator, new third-order chaotic systems are most efficiently designed by using the equivalent mapping approach. This idea is similar to linear filter synthesis. Popular filter responses such as Butterworth and Bessel are cataloged by their normalized eigenvalues, and filters are synthesized by mapping these eigenvalues into physical circuits [74]. On this historical basis, the chaotic feedback circuits in this study are designed via the chaotic mapping approach.

9.3 A Linearly Conjugate Mapping Example

In this section, the conjugate mapping technique is demonstrated. The work of this section is a similar development to [62] and presented here for the readers convenience. The circuit of Figure 9.3 with a piecewise linear N-shaped conductance is a member of the Chua oscillator family having three-segment, piecewise-linear conductances [60]. Neglecting the inductor resistance, this circuit was Chua's second chaos candidate in his original synthesis approach [59]. Matching the eigenvalues of this system to the eigenvalues of the Chua oscillator should give linearly equivalent dynamics in the new circuit.

![Fig. 9.3. Circuit for linearly conjugate mapping example.](image)

The state equations of the new configuration, linearized about the inner and outer equilibria, are given by Equation (9.1).

\[
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_1 \\
\dot{v}_2
\end{bmatrix} = \begin{bmatrix}
\frac{R_2}{L} & -\frac{1}{L} & \frac{1}{L} \\
0 & -\frac{g_i}{C_i} & 0 \\
-\frac{1}{C_2} & 0 & -\frac{1}{R_2 C_2}
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_2
\end{bmatrix}
\]  

(9.1)
where

\[ g_i = \left. \frac{df(V)}{dV} \right|_{V_i} \]

\[ i = 1: V_i = V_{inner} \]

\[ i = 2: V_i = V_{outer} \]

(9.2)

Now applying a time variable change, state variable change, a parameter substitution

\[ t' = \frac{t}{R_1 C_1}, \quad i_L = \frac{V_x}{R_i}, \quad R_2 = R_2 - R_1 \]

(9.3)

and defining the following dimensionless parameters,

\[ \alpha = \frac{C_2}{C_1}, \quad \gamma = \frac{C_2}{L} R_1^2, \quad \beta = \frac{R_2}{R_i} - 1, \quad a_1 = g_1 R_i, \quad a_2 = g_2 R_i \]

(9.4)

the non-dimensionalized matrix representation of Equation (9.5) is obtained.

\[
\begin{bmatrix}
    v_x' \\
    v_i' \\
    v_2'
\end{bmatrix} =
\begin{bmatrix}
    -\beta \gamma & -\gamma & \gamma \\
    \alpha & -\alpha \gamma & 0 \\
    -1 & 0 & -1
\end{bmatrix}
\begin{bmatrix}
    v_x \\
    v_i \\
    v_2
\end{bmatrix}
\]

(9.5)

The characteristic equation of this non-dimensionalized system is

\[
\lambda^3 + [a_1 \alpha + \beta \gamma + 1] \lambda^2 + [a_1 \alpha (1 + \beta \gamma) + \beta \gamma + \gamma + \alpha \gamma] \lambda + [a_1 \alpha \gamma (1 + \beta) + \alpha \gamma] = 0
\]

(9.6)

Using the notation in [60], the prescribed eigenvalues from the Chua oscillator at the inner and outer equilibrium points are \((\mu_1, \mu_2, \mu_3)\) and \((\nu_1, \nu_2, \nu_3)\). Since the prescribed sets of eigenvalues define two unique characteristic equations [60], it is sufficient to match characteristic equation coefficients of the Chua oscillator and the normalized system. The prescribed characteristic equations become

\[
\lambda^3 - p_1 \lambda^2 + p_2 \lambda - p_3 = 0 \quad \lambda^3 - q_1 \lambda^2 + q_2 \lambda - q_3 = 0
\]

(9.7)
where

\[
\begin{align*}
  p_1 &= \mu_1 + \mu_2 + \mu_3 & q_1 &= v_1 + v_2 + v_3 \\
  p_2 &= \mu_1 \mu_2 + \mu_1 \mu_3 + \mu_2 \mu_3 & q_2 &= v_1 v_2 + v_1 v_3 + v_2 v_3 \\
  p_3 &= \mu_1 \mu_2 \mu_3 & q_3 &= v_1 v_2 v_3
\end{align*}
\] (9.8)

Full details of the basic mapping approach are not presented here, but it is important to note that a problem arises for this example. If the prescribed eigenvalues are not correctly normalized, the mapping of coefficients leads to six simultaneous equations in only five unknowns. This problem is corrected by solving for the time normalizing value \( \tau_0 \) which reduces the non-dimensionalized system to five independent nonlinear equations.

\[
\tau_0 = \frac{p_2 + \left(\frac{p_2 - q_2}{p_1 - q_1}\right) - p_1 + \left(\frac{p_2 - q_2}{p_1 - q_1}\right)}{-p_3 - \left(\frac{p_3 - q_3}{p_1 - q_1}\right) - p_1 + \left(\frac{p_3 - q_3}{p_1 - q_1}\right)}
\] (9.9)

With \( \tau_0 \) known, the prescribed coefficients can be normalized and the component values of the new circuit calculated.

As a numerical example, the chaotic Chua circuit eigenvalues of Table 5 in [60] are chosen.

\[
\begin{align*}
  \mu_1 &= 6860 & v_1 &= -4840 \\
  \mu_2 &= -226 + j4650 & v_2 &= 160 + j4650 \\
  \mu_3 &= -226 - j4650 & v_3 &= 160 - j4650
\end{align*}
\] (9.10)

Applying the mapping technique, the circuit parameters of Figure 9.3 become

\[
\begin{align*}
  L &= -0.1H & C_1 &= 346pF & C_2 &= -53pF \\
  g_1 &= -0.2\text{mmho} & g_2 &= 0.134\text{mmho} \\
  R_1 &= 247.4\text{Kohm} & R_2 &= -8.8\text{Kohm}
\end{align*}
\] (9.11)

Figure 9.4 shows the PSpice simulated dynamics of the new circuit in the state space. The simulation predicts a chaotic behavior.
Figure 9.4. Chaotic circuit results from mapping procedure.

Figure 9.5 shows the dynamics of the same circuit with a cubic nonlinear resistor matched to the calculated inner conductance value of Equation (9.11). Since the cubic model does not match the calculated conductance at the outer equilibria, this simulation demonstrates that the circuit does tolerate small changes in parameters. This robustness is highly important and becomes an integral part of the practical synthesis method.

Figure 9.5. Chaotic dynamics with cubic nonlinear resistor.

As discussed in the introduction, this circuit is not a good candidate for practical chaos designs. It requires a nonlinear conductance and three active linear components. A configuration utilizing a three-terminal N-shaped device and feedback is now investigated as a potential solution to this practical implementation problem.
9.4 A Chaotic Three-Terminal N-Shaped Conductance Design

Consider the circuit configuration in Figure 9.6. This circuit was selected since it allows a direct evaluation of the advantages of feedback. For zero gate dependence, the circuit is functionally equivalent to the configuration of Figure 9.3. Also, this configuration is the natural model which arises from practical three-terminal N-shaped devices.

![Circuit Diagram](image)

Fig. 9.6. The proposed feedback circuit for generating chaos.

### 9.4.1 The nonlinear and linearized small signal differential equation models

The state variable equations of the feedback circuit are given by Equation (9.12).

\[
\begin{align*}
\dot{I}_L &= -\frac{1}{L}[I_L R_2 - V_1 + V_2] \\
\dot{V}_1 &= \frac{1}{C_1}[I_L - f_1(V_1) - f_2(V_1, V_G)] \\
\dot{V}_2 &= \frac{1}{C_2}[-I_L - V_2 \frac{1}{R_1} + V_\infty \frac{1}{R_1}] 
\end{align*}
\tag{9.12}
\]

where

\[
V_G = -R_1 \left[ \frac{V_\infty - V_2}{R_1} - I_L \right] 
\tag{9.13}
\]
The equilibrium points are still determined by the load line method presented in Chapter 2. But now the linearized small signal model about equilibrium points is given by Equation (9.14).

\[
\begin{bmatrix}
    i_L \\
    v_1 \\
    v_2
\end{bmatrix} = \begin{bmatrix}
    -R_L/L & -1/L & 1/L \\
    -g_{m1} R_L & -g_{m2} & R_L \\
    -1/C_2 & 0 & -R_{L2}/C_2
\end{bmatrix} \begin{bmatrix}
    i_L \\
    v_1 \\
    v_2
\end{bmatrix}
\]  

(9.14)

where

\[
g_i = \frac{d f_i(V_1)}{d V_1} + \left. \frac{d f_2(V_1, V_o)}{d V_1} \right|_{V_1 = V_{in}, V_o = 0} \quad i = 1: \quad V_1 = V_{inner}
\]

\[
g_{mi} = \left. \frac{d f_2(V_1, V_o)}{d V_o} \right|_{V_1 = V_{in}, V_o = 0} \quad i = 2: \quad V_1 = V_{outer}
\]  

(9.15)

### 9.4.2 A chaos design methodology

Before proceeding with the chaos synthesis, a design approach must be developed which accounts for the full nonlinear characteristic of the device. In general, a true three-terminal device exhibits both a nonlinear conductance and nonlinear transconductance with neither being symmetric. The conjugate mapping technique proposed by Chua is for a family of circuits containing a single odd-symmetric nonlinearity. In a design utilizing Chua's approach, these differences must be addressed and a solution proposed. A successful solution is presented here.

In the previous section, it was demonstrated that the experimental chaos design could tolerate changes in circuit parameters. This result suggests that the designer pursue an ideal synthesis and investigate non-idealities from the standpoint of sensitivity; therefore, the nonsymmetry issues and the nonlinear transconductance can be decoupled from an initial synthesis and their effects investigated independently. This method brings the circuit back to a member of the Chua circuit family and the conjugate matching approach is valid. Integrating a practical realizability method into the conjugate matching approach, an "ideal" implementation can be designed. After this initial design is complete,
a sensitivity study can be performed to predict the effects of parameter mismatch and nonlinear transconductance. Nonsymmetry studies have already been done in [58] and conclusions to this issue can be drawn. This overall design effort is the practical synthesis solution pursued in this work. The rest of this section presents the initial ideal design with practical realizability constraints and the following section describes the sensitivity investigations.

9.4.3 The initial conjugate mapping with practical realizability criterions

To begin the ideal design process, the N-shaped conductance is modeled as piecewise-linear, odd-symmetric and the transconductance is constant. Implementing this simpler model, the system is non-dimensionalized. Changing the time variable, one state variable, substituting a new parameter

\[ t' = \frac{t}{R_1 C_2}, \quad i_L = \frac{v_x}{R_1}, \quad R_2 = R_T - R_i \]  

(9.16)

and defining the following dimensionless parameters

\[ \alpha = \frac{C_2}{C_1}, \quad \gamma = \frac{C_2 R_i^2}{L}, \quad \beta = \frac{R_T - R_i}{R_1}, \quad g_m R_i = b \]

\[ \alpha_1 = g_1 R_i, \quad \alpha_2 = g_2 R_i \]

(9.17)

the non-dimensionalized system of Equation (9.18) is obtained.

\[
\begin{bmatrix}
  v'_x \\
  v'_1 \\
  v'_2
\end{bmatrix} =
\begin{bmatrix}
  -\beta \gamma & -\gamma & \gamma \\
  \alpha (1 - b) & -\alpha \alpha & -\alpha b \\
  -1 & 0 & -1
\end{bmatrix}
\begin{bmatrix}
  v_x \\
  v_1 \\
  v_2
\end{bmatrix}
\]

(9.18)

The characteristic equation for the non-dimensionalized system is

\[
\lambda^3 + [a_1 \alpha + \beta \gamma + 1] \lambda^2 + \\
[\alpha_1 (1 + \beta \gamma) - b a \alpha + \gamma (1 + \beta) + a \gamma] \lambda + [a_1 \alpha \gamma (1 + \beta) + \alpha \gamma] = 0
\]

(9.19)
As in the last section, the goal is to match the coefficients of this system to those obtained from a set of prescribed eigenvalues. Maintaining the prior notation, a set of composite constants can be defined from the prescribed coefficients to aid in the mapping.

\[
\begin{align*}
    k_1 &= \frac{p_2 - q_2}{p_1 - q_1}, \\
    k_2 &= p_2 + k_1(-p_1 + k_1) - k_3, \\
    k_3 &= \frac{p_3 - q_3}{p_1 - q_1}, \\
    k_4 &= -p_3 - k_3(-p_1 + k_1) - k_3
\end{align*}
\] (9.20)

To obtain a practical circuit design, the conjugate mapping approach must be combined with a set of realizability constraints. In the previous section, the configuration forced a unique time scaling for normalizing the prescribed eigenvalues. Having increased the parameter set with the negative AC feedback, the designer no longer suffers this limitation. The non-dimensionalized circuit can be mapped directly to the prescribed coefficients ($\tau_n=1$) or any other scaling of them. By investigating the impact of $\tau_n$ on the polarity of the dimensionless parameters, it is possible to choose a value which makes the circuit a more practical implementation. To obtain an appropriate selection of $\tau_n$, it must be included in the matching equations. The following sets of equations give the relationship between the normalized prescribed quantities and the originals.

\[
\begin{align*}
    p_{1n} &= \tau_n p_1, & q_{2n} &= \tau_n q_1, \\
    p_{2n} &= \tau_n^2 p_2, & q_{2n} &= \tau_n^2 q_2, \\
    p_{3n} &= \tau_n^3 p_3, & q_{3n} &= \tau_n^3 q_3, \\
    k_{1n} &= \tau_n k_1, & k_{3n} &= \tau_n^2 k_3, \\
    k_{2n} &= \tau_n^2 k_2, & k_{4n} &= \tau_n^3 k_4
\end{align*}
\] (9.21)

Following this preliminary manipulation, six equations are obtained via the coefficient matching technique and are given by Equation (9.23). The relationships are shown both in terms of normalized and original prescribed quantities.
For a practical design, the dimensionless parameters \( \alpha \), \( \beta \), and \( \gamma \) are required to be positive and the nonlinear conductance characteristic is defined as N-shaped. From these requirements and Equation (9.23), three fundamental realizability constraints are obtained.

\[
\begin{align*}
\tau_n(p_1 - q_1) > 0 \\
k_3 > 0 \\
\tau_n k_1 < 0
\end{align*}
\]  

(9.24)

From these constraints, a realizability test can be applied to the original prescribed eigenvalues to determine if a practical design can be obtained for this feedback circuit configuration. The candidate eigenvalues must fall into one of the following two cases. The impact on the required time scaling is also shown.

Case 1:
\[
\begin{align*}
(p_1 - q_1) > 0 \\
(p_2 - q_2) < 0 \\
(p_3 - q_3) > 0 \\
k_4 > 0 \\
\tau_n > 0
\end{align*}
\]  

Case 2:
\[
\begin{align*}
(p_1 - q_1) < 0 \\
(p_2 - q_2) < 0 \\
(p_3 - q_3) < 0 \\
k_4 < 0 \\
\tau_n < 0
\end{align*}
\]  

(9.25)

Now Equation (9.23) can be solved to obtain explicit expressions for \( \gamma \), \( \beta \), and \( \alpha \).
\[ \gamma = 1 + k_{1n} + k_{3n} = 1 + \tau_n k_1 + \tau_n^2 k_3 \]  
\[ \beta = -\frac{(1 + k_{1n})}{\gamma} = -\frac{(1 + \tau_n k_1)}{\gamma} \]  
\[ \alpha = \frac{k_{3n}}{\gamma} = \frac{\tau_n^3 k_3}{\gamma} \]

Again forcing the practical condition of \( \gamma, \beta, \) and \( \alpha \) positive, ranges of allowable time normalizations are obtained.

\[ f_1(\tau_n) = \tau_n^2 + \frac{k_1}{k_3} \tau_n + \frac{1}{k_3} > 0 \quad \text{and} \quad f_2(\tau_n) = 1 + \tau_n k_1 < 0 \]  

Further investigation into Equation (9.27) is best done on a **Case 1** or Case 2 basis given the inequalities. **Only** Case 1 is discussed here, Case 2 is just a mirror image on the negative \( \tau_n \) axis. Figure 9.7 shows a typical plot of a Equation (9.27). If the quadratic equation has no real roots it can be ignored and the second condition alone determines the acceptable range of time normalization. The **realizability** criterion is \( \tau \) greater than \( \tau_{min} \) and in this case \( \tau \) must be greater than \( \tau_{hi} \).

Fig. 9.7. Appropriate range of time scaling selection.
After choosing \( \tau_n \) in an appropriate region, a practical design can be realized and the dimensionless parameters are given by Equation (9.28).

\[
\begin{align*}
\gamma &= 1 + k_{1n} + k_{3n} \\
\beta &= \frac{1 + k_{1n}}{\gamma} \\
a_1 \alpha &= -p_{1n} + k_{1n} \\
a_2 \alpha &= -q_{2n} + k_{1n} \\
\alpha &= \frac{k_{4n}}{\gamma} \\
b &= 1 - \frac{k_{2n}}{k_{4n}}
\end{align*}
\] (9.28)

From Equation (9.17), these dimensionless parameter expressions give six equations in the eight unknown circuit parameters. The designer has the freedom to choose a conductive component and one memory component independently, and he has the freedom to apply frequency and magnitude scaling as desired. One drawback of this simple circuit is that the load line cannot be arbitrarily chosen with respect to the desired local conductance at the equilibrium points.

Before leaving this section, it is worthwhile to examine the dimensionless feedback parameter \( b \) of Equation (9.28). This expression is independent of the inner and outer conductance parameters and is a function only of the prescribed eigenvalues and their time normalization. An alternative expression for \( b \) is given in Equation (9.29) where \( \tau_0 \) is the time normalizing value from the circuit with no feedback.

\[
b = 1 - \frac{\tau_0}{\tau_n}
\] (9.29)

This relationship is a nice result. It shows that if a true practical design not requiring feedback exists, it is just a special time scaling case in the proposed method.

### 9.4.4 An initial design example

To demonstrate the success of adding AC feedback, the prescribed eigenvalues from the previous example, Equation (9.10), are mapped to the new circuit configuration. Implementing the results of the mapping technique and the realizability conditions into a spreadsheet format, the design is easily accomplished. Magnitude and frequency scaling is also done in the spreadsheet. Figure 9.8 shows the spreadsheet details leading to the circuit component values of Equation (9.30).
### Feedback Configuration Eigenvalue Mapping Worksheet

**Prescribed Eigenvalues for the System Linearized at the Inner and Outer Equilibrium Points**

<table>
<thead>
<tr>
<th>Prescribed Eigenvalues</th>
<th>( u_1 )</th>
<th>( u_2 )</th>
<th>( u_3 )</th>
<th>( u_3' )</th>
<th>( v_1 )</th>
<th>( v_2 )</th>
<th>( v_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 6.86 \times 10^3 )</td>
<td>-226</td>
<td>4.65 \times 10^3</td>
<td>-226</td>
<td>-4650</td>
<td>-4640</td>
<td>-4650</td>
<td>-4660</td>
</tr>
</tbody>
</table>

**Resulting Prescribed Characteristic Equation Coefficients at the Inner and Outer Equilibria**

<table>
<thead>
<tr>
<th>( a_1 )</th>
<th>( a_2 )</th>
<th>( a_3 )</th>
<th>( a_4 )</th>
<th>( a_5 )</th>
<th>( a_6 )</th>
<th>( b_1 )</th>
<th>( b_2 )</th>
<th>( b_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.41 \times 10^3</td>
<td>1.65 \times 10^4</td>
<td>1.49 \times 10^4</td>
<td>-4520</td>
<td>200999300</td>
<td>-1 \times 10^4</td>
<td>1.09 \times 10^4</td>
<td>-1526444</td>
<td>2.53 \times 10^4</td>
</tr>
</tbody>
</table>

**Composite Constants**

<table>
<thead>
<tr>
<th>( k_1 )</th>
<th>( k_2 )</th>
<th>( k_3 )</th>
<th>( k_4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>-139.682</td>
<td>-139.682</td>
<td>3705957</td>
<td>3.18 \times 10^9</td>
</tr>
</tbody>
</table>

**Constraints on the Time Constant and Its Selection**

<table>
<thead>
<tr>
<th>( \tau_1 )</th>
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<th>( \tau_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.16 \times 10^{-3}</td>
<td>#NUM!</td>
<td>#NUM!</td>
</tr>
</tbody>
</table>

**Normalized Prescribed Eigenvalues**

<table>
<thead>
<tr>
<th>( \mu_1 )</th>
<th>( \mu_2 )</th>
<th>( \mu_3 )</th>
<th>( \mu_3' )</th>
<th>( \nu_1 )</th>
<th>( \nu_2 )</th>
<th>( \nu_3 )</th>
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</thead>
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<td>46.5</td>
<td>-2.26</td>
<td>46.5</td>
<td>-48.4</td>
<td>1.65</td>
</tr>
</tbody>
</table>

**Normalized Prescribed Characteristic Coefficients**

<table>
<thead>
<tr>
<th>( p_1 )</th>
<th>( p_2 )</th>
<th>( p_3 )</th>
<th>( p_4 )</th>
<th>( p_5 )</th>
<th>( p_6 )</th>
<th>( q_1 )</th>
<th>( q_2 )</th>
<th>( q_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.41 \times 10^4</td>
<td>1.65 \times 10^4</td>
<td>1.49 \times 10^4</td>
<td>-4520</td>
<td>200999300</td>
<td>-1 \times 10^4</td>
<td>1.09 \times 10^4</td>
<td>-1526444</td>
<td>2.53 \times 10^4</td>
</tr>
</tbody>
</table>

**Normalized Composite Constants**

<table>
<thead>
<tr>
<th>( \kappa_1 )</th>
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<th>( \kappa_3 )</th>
<th>( \kappa_4 )</th>
</tr>
</thead>
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<td>-139.682</td>
<td>-139.682</td>
<td>3705957</td>
<td>3.18 \times 10^9</td>
</tr>
</tbody>
</table>

**Normalized System Parameter Calculation**

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<tr>
<th>( \beta )</th>
<th>( \gamma )</th>
<th>( \alpha )</th>
<th>( a_1 )</th>
<th>( a_2 )</th>
<th>( a_3 )</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1.37 \times 10^4</td>
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<td>31.9193</td>
<td>1.116455</td>
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</table>

**Normalized Circuit Characteristic Equation Coefficients**

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<th>( b_3 )</th>
</tr>
</thead>
<tbody>
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<tr>
<td>45.2</td>
<td>2009.93</td>
<td>104776.8</td>
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</tbody>
</table>

**Calculation of Circuit Parameters**

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<thead>
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<th>( c_1 )</th>
<th>( c_2 )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>RF</th>
<th>( L )</th>
<th>( g_1 )</th>
<th>( g_2 )</th>
<th>( g_m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>238600</td>
<td>0.000708</td>
<td>0.000972</td>
<td>238559.2</td>
<td>40.8224</td>
<td>3359.965</td>
<td>238600</td>
<td>-0.0002</td>
<td>0.000134</td>
</tr>
</tbody>
</table>

**Magnitude Scaling Selection** 2.39E+05

**Magnitude Scaling Results**

<table>
<thead>
<tr>
<th>( c_1 )</th>
<th>( c_2 )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>RF</th>
<th>( L )</th>
<th>( g_1 )</th>
<th>( g_2 )</th>
<th>( g_m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>238600</td>
<td>0.000708</td>
<td>0.000972</td>
<td>238559.2</td>
<td>40.8224</td>
<td>3359.965</td>
<td>238600</td>
<td>-0.0002</td>
<td>0.000134</td>
</tr>
</tbody>
</table>

**Frequency Scaling Selection** 2.39E+05

**Frequency Scaling Results**

<table>
<thead>
<tr>
<th>( c_1 )</th>
<th>( c_2 )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>RF</th>
<th>( L )</th>
<th>( g_1 )</th>
<th>( g_2 )</th>
<th>( g_m )</th>
</tr>
</thead>
<tbody>
<tr>
<td>238600</td>
<td>2.97E-09</td>
<td>4.07E-09</td>
<td>238559.2</td>
<td>40.8224</td>
<td>3359.965</td>
<td>238600</td>
<td>-0.0002</td>
<td>0.000134</td>
</tr>
</tbody>
</table>

Fig. 9.8. Feedback configuration chaotic design worksheet.
From the design spreadsheet, the following circuit parameters are obtained

\[
\begin{align*}
L &= 0.1 H \\
C_1 &= 3 nF \\
C_2 &= 4 nF \\
R_1 &= 238.6 \text{kohm} \\
R_2 &= 41 \text{ohm} \\
R_p &= 3360 \text{ohm} \\
g_m &= 0.3322 \text{mmho} \\
g_i &= -0.2 \text{mmho} \\
g_o &= 0.134 \text{mmho}
\end{align*}
\]

(9.30)

Notice that the desired result of passive linear circuit components is realized. Figure 9.9 shows a dynamic trajectory of this circuit with the same cubic nonlinearity as Figure 9.5.

Fig. 9.9. Chaotic circuit dynamics from proposed feedback design.

Another desirable result in this example is the polarity of the linearized conductance at the outer equilibria. For the Chua oscillator, designs with passive linear components have been documented [60], but these designs require both the \textit{inner} and outer equilibria to have a negative linearized conductance. For recently developed three-terminal N-shaped devices, this requirement may be difficult and impractical \textit{since} it will lead to a highly sensitive design. This problem is due to the nature of the negative conductance region and the small margin in acceptable load lines. The outer conductances given by this approach are easily obtained.

\textbf{9.5 Completing the Practical Design}

With the initial design \textit{successfully} completed, the designer \textit{can} now focus on the other nonlinear characteristics of the device. Three specific non-idealities of the three-
terminal N-shaped conductance need to be addressed: non-symmetry, conductance mismatch, and a nonlinear transconductance. The effects of non-symmetry has been studied in [58] and will be pursued here in terms of parameter mismatch. In this section, the issues of conductance mismatch and nonlinear transconductance are investigated.

9.5.1 The plan

The conjugate matching results led to a determination of the inner and outer conductance values for a piecewise linear Chua diode. For a practical device, the nonlinear conductance will not be odd-symmetric, piecewise linear nor will equilibria determined by the intersection of the load line have the two calculated local conductance values. Since there is no unique approach to the mismatch study, a (convenient method is chosen. The initial system can always be magnitude scaled so the inner conductance equals \( g_{\text{min}} \) of the nonlinear conductance component. Now by an appropriate choice of bias on the load line only mismatch at the outer equilibrium points are an issue. This mismatch will not be the same at each of the outer equilibria due to non-symmetry. The conjugate matching also led to a required linear feedback gain. The nonlinear transconductance will cause mismatch during the oscillation. Since the feedback resistor can be changed, settings relative to the initial design value are investigated.

9.5.2 A stability plot approach to sensitivity

If a chaos circuit design is of any practical interest, structural stability must be one of its characteristics. In a previous section, an example showed that a simple chaos design did exhibit some degree of robustness. This result suggests that sensitivity to parameter mismatches can be studied by considering the range of structural stability as discussed in [58, 75]. Recall the characteristic equation from the small signal model of the initial feedback circuit linearized about its equilibrium points.

\[
\lambda^3 + [a_1(1 + \beta + \gamma) + 1]\lambda^2 + [a_1(1 + \beta) - b_1 \alpha + \gamma(1 + \beta) + \alpha_1 \gamma] \lambda + [a_1, a_2(1 + \beta) + \alpha_2 \gamma] = 0
\]  

(9.31)

The local dynamics of the equilibrium points are determined by the prescribed chaotic eigenvalues. Since the interest here is in the conductance and the feedback gain, consider the effects of dimensionless parameters \( a \) and \( b \) becoming variable. Over some range near the ideal values, the dynamics should be qualitatively equivalent in a robust system. It is this characteristic that is manipulated to obtain the desired results.
One way to attack this problem is to consider the Routh criterion. For a third-order system, four relationships are obtained which describe the local stability of equilibrium points as a function of system parameters. Plotting these relationships in the $a$-$b$ plane, ideal design values can be located and areas of qualitatively similar local dynamics can be defined. This part of the design approach is similar to the stability plane ideas of Chapter 2. Equation (9.32) gives the Routh stability criterion for the feedback configuration.

\[
\begin{align*}
  a &> \frac{k_{in}}{a} \\
  b &< -\frac{k_{in}}{\gamma \left( a - \frac{k_{in}}{a} \right)} \left[ a^2 - a \left( \frac{\gamma}{k_{in} \alpha} + \frac{k_{in}}{\alpha^2} \right) + \frac{k_{jn} \gamma}{\alpha} \left( 1 + \frac{1}{k_{jn}} \right) \right] \\
  a &> -\frac{\gamma}{k_{jn}} \\
  b &< -\frac{a - k_{in} + k_{jn}}{\gamma} + 1
\end{align*}
\] (9.32)

9.5.3 An Illustrative Example

The best way to demonstrate this portion of the practical design is to continue the example of the previous section. From the initial design spreadsheet of Figure 9.8, Equation (9.32) becomes

\[
\begin{align*}
  a &> -1.022 \\
  b &< \frac{0.000604}{a + 1.022} \left[ a^2 + 1657.4a + 1719.32 \right] \\
  a &> -0.9998 \\
  b &< 0.000604a + 1.7301
\end{align*}
\] (9.33)

Plotting these stability relationships, Figure 9.10 is obtained. The location of the ideal $a$ and $b$ parameters are also identified. By this stability plot method, the regions of equivalent dynamics are determined by the boundaries and become obvious. (Note only the $b$ relationships are plotted to avoid clutter, the $a$ boundaries are just vertical lines.)
Now consider using the two slightly different three-terminal N-shaped devices with the current-voltage characteristics of Figures 9.11 and 9.12 to generate chaos. The only difference in the devices is the nonlinear transconductance. All external circuit parameters except for the feedback resistor are going to be held to their initial design values. Notice, zero bias will lead to the desired load line placement. The minimum conductance of the devices is the ideal value of \(-0.2\) mmho, but mismatch exists at the outer conductance values and the transconductance of both is nonlinear.

Fig. 9.10. Stability plane for chaotic circuit design.

Fig. 9.11. Parameter mismatch study device one.
To begin, address only the outer conductance mismatch issue. The load line from the initial design leads to an outer local conductance of approximately 0.4 mmho for both devices. The new location of $a$ is plotted in Figure 9.13 and chaos is predicted. For this new outer conductance and linear feedback gain equal to the initial design value, PSpice simulation verifies the existence of chaotic behavior as predicted.

Fig. 9.12. Parameter mismatch study device two.

Fig. 9.13. Stability plot showing parameter mismatch results.
Now the nonlinear transconductance is added by looking at its vertical displacement effect in the a-b plane. At the inner equilibrium point, the local transconductance is 0.3322 mmho for both devices. It is decreasing monotonically in each direction and is at 0.3215 mmho at the outer equilibria for device one. The local transconductance at the outer equilibria of the second device is 0.258 mmho. The new points in the stability plot of Figure 9.13 suggest that only the first device can still be chaotic. PSpice simulation confirms these ideas.

It makes sense that an increase in the feedback resistor might bring the circuit using device two back into chaos. So far simulations show this is not a very fruitful effort, mostly limit cycles are produced. This result is important because this stability plane idea can predict the possibility of chaos, but cannot guarantee it.

These simulations reveal that this approach is suitable for a design which consists of an initial mapping followed by a perturbation investigation of the initial design values. This approach can be extended to all circuit parameters and fine tuned when a true device characteristic is in hand.

9.6 Injection Locking Revisited

Although chaotic signals are often compared to white noise generators, an inspection of the frequency spectrum often shows structure does exist. Reconsider the nonlinear device defined in Equation (8.12) and the feedback circuit design parameters from this chapter. The chaotic drain to source voltage of the nonlinear device is shown in the time and frequency domains in Figures 9.14 and 9.15. From the spectral plot, it is clear that a peak does occur in the frequency domain. Inspecting the feedback signal, a peak at the same frequency is found.

9.6.1 A driven chaotic system

An interesting idea is to filter the feedback signal about this peak and try to maintain chaos. In the limit, this approach leads to an ideal filter which passes only a single frequency near the peak of the spectrum. If this feedback circuit leads to chaos, then by the substitution theorem, the feedback signal can be replaced by an ideal source at the same frequency and amplitude and chaos should again be observed. As an example, the data from Figure 9.15 can be used to obtain a driving amplitude of 6 volts and frequency of 7.5KHz. Using PSpice, the chaotic signal of Figure 9.16 is obtained.
Fig. 9.14. Chaotic time domain signal.

Fig. 9.15. Frequency spectrum of chaotic signal.

Fig. 9.16. Driven chaotic behavior.
This simple extension from the chaotic autonomous feedback system to an apparently chaotic driven third-order system is very important. Since the design of the feedback system was performed to obtain practical values of circuit components, this result implies that the proposed switching circuits may have highly undesirable dynamics. To investigate this problem a little further, the harmonic balance results are looked at for an indicator of possible chaotic behavior.

9.6.2 Harmonic balance predictions

In Chapter 8, the harmonic balance approach was used to predict stable driven oscillations. The harmonic balance method has been investigated lately by several researchers as a practical method for predicting the possibility of chaos [76, 77, 78]. The results of the second-order equation of [78] is particularly interesting since the nonlinearity is similar to this example. But what does the HBM predict for this circuit with the injection amplitude selected to generate Figure 9.16? Figure 9.17 shows the harmonic balance injection locking plot a six volt amplitude driving voltage. This plot is very interesting since it looks similar to a linear notch filter, but a major difference is that the locked oscillation loses stability in the notch as denoted by the dashed line. The chaotic driven system is being driven precisely in the frequency region.

![Fig. 9.17. Frequency response plot for driving gate amplitude of 6 volts.](image)

This result appears to be different than those shown for chaos in [78]. In [78] the chaos occurs near regions where more than one stable limit cycle is possible. This is not
the case for our system at this high driving amplitude. For lower driving amplitudes, this system also shows behavior similar to [78] and it may be susceptible to chaotic behavior there also. Future efforts into this area is planned, but the results pertaining to this thesis have been obtained and further work is left for another study.

9.7 Summary

In this chapter, a chaos synthesis method proposed by Chua has been extended and combined with a set of practical realizability constraints to create chaos in a third-order circuit with linear AC feedback. Also, a method for extending these results to the device with nonlinear transconductance was presented. The primary result is that a negative feedback design with the three-terminal N-shaped device may lead to more practical chaos designs. It was also shown that this method can lead to the design of driven almost periodic and possibly chaotic systems with passive linear circuit components. This result suggests that logic designs using this device may lead to unexpected chaotic results.
10. A THREE-TERMINAL RTD AND CHAOS

10.1 Introduction

In the previous chapter, a successful method for chaos synthesis with a three-terminal N-shaped conductance device was presented. Now it is time to turn attention to currently available three-terminal Resonant Tunneling Devices (RTD) and the special problems which arise with them. Basically, there is one fundamental limitation of the RTD which has not been addressed, the device current dynamic range. In this chapter, a rule of thumb criterion is developed to predict if a set of prescribed Chua circuit eigenvalues are applicable to a given RTD characteristic.

10.2 The Transconductance Current Issue

So far it has been assumed that the dynamic range of the transconductance current for fixed drain to source voltage was unlimited. In other words, the transconductance current was allowed to be as large as the design dictated. From a circuit theoretic standpoint, this result is inconsequential since operation in any quadrant of the I-V characteristic is possible. From the characteristics in [35], this appears not to be a critical issue in the two-terminal illuminated device. For RTD’s, this situation may violate the physics of the device. The three-terminal RTD’s being fabricated at Purdue have I-V characteristics which are limited to the first and third quadrant of the I-V plane. In this study, the device is being further limited to first quadrant operation due to its practical significance.

Reconsider the chaotic design example from the last chapter and device of Figure 9.11. Simulation showed the circuit was chaotic and the prescribed design led to a transconductance current peak to peak amplitude of approximately 400μA. The conductance current peak to peak amplitude is approximately 30μA. Assume a device similar to the one of Figure 9.11 where the origin of the $I_{DS}-V_{DS}$ plane has been translated to the first quadrant is used in chaos design. For the total device current to remain
positive for all time during chaos, the valley current of the new zero gate excitation I-V curve must be greater than $400\mu A$.

This specification development is both inefficient and too specific. The results are obtained by designing the circuit around a simple model of the candidate device and running simulations. A more valuable approach is to generate an approximate relationship relating the device I-V characteristics to the prescribed chaotic eigenvalues. The goal of the following section is to develop a simple calculation method for determining whether a chaos design is suitable for a given RTD.

10.3 Dependence on the Linear Tuned Circuit

A basic chaos design rule for RTD’s can be made by using two practical approximations from the operation of N-shaped devices in the feedback circuit of Figure 9.6. First, the overall feedback mechanism of the circuit is current gain. Second, the voltage amplitude of oscillation or chaos is determined by the device nonlinearity and is reasonably easy to estimate for a given RTD characteristic. Based on this viewpoint, it is worthwhile to study the linear circuit of Figure 10.1.

![Fig. 10.1. The linear circuit model under investigation.](image)

The frequency domain expression for the input admittance is given by Equation (10.1).

$$ |Y_{in}|^2 = \frac{|I|^2}{|V|^2} = \frac{1}{L^2} \left[ \frac{1}{\left( \frac{1}{R_1 C_2} \right)^2 + w^2} \right] \left[ \frac{1}{LC_2 \left( 1 + \frac{R_2}{R_1} \right) - w^2} \right]^2 + w^2 \left( \frac{1}{R_1 C_2} + \frac{R_2}{L} \right) $$  (10.1)
Now defining the following terms, the alternative relationship of Equation (10.3) is obtained.

\[
w_0^2 = \frac{1}{LC^2} \quad w_c = \frac{1}{R_tC^2} \quad w_L = \frac{R_2}{L} \tag{10.2}
\]

\[
\frac{L}{C^2} |Y_{in}|^2 = \frac{\left(\frac{w}{w_0}\right)^2 + \left(\frac{w_c}{w_0}\right)^2}{\left[1 + \frac{R_2}{R_t} \left(\frac{w}{w_0}\right)^2\right]^2 + \left(\frac{w_c + w_L}{w_0}\right)^2} \tag{10.3}
\]

Employing the dimensionless relationships defined in Equation (9.17), Equation (10.3) becomes

\[
R_t^2 |Y_{in}|^2 = \frac{\gamma \left(\frac{w}{w_0}\right)^2 + 1}{1 + \beta - \left(\frac{w}{w_0}\right)^2 + \left(\frac{1}{\gamma} + 2\beta + \gamma \beta^2\right)} \tag{10.4}
\]

Taking the derivative of Equation (10.4) with respect to \(\omega\) and setting equal to zero, the frequency of maximum input admittance \(\omega_m\) is obtained.

\[
\left(\frac{w_m}{w_0}\right)^2 = \left[2\beta + \frac{2}{\gamma} + 1\right] - \frac{1}{\gamma} \tag{10.5}
\]

Defining a composite dimensionless function, \(G\)

\[
G = R_t |Y_{in}| \frac{w_m}{w_0} \frac{w_m}{w_0} \tag{10.6}
\]

an approximate expression for the maximum amount of transconductance current for a \textit{limit cycle oscillator} design is given by Equation (10.7)
Recall the resistor $R_1$ was determined by choosing the inner conductance value from the conjugate matching technique equal to $g_{\text{min}}$ of the candidate N-shaped device. Solving the system of Equation (9.17) for the required $R_1$ gives

$$R_1 = \frac{a_1}{g_{\text{min}} \beta + 1}$$

Defining the magnitude of the transconductance current of Equation (10.7) to be smaller than the RTD valley current under zero dynamic gate excitation and substituting Equation (10.8) into (10.7), the following design criterion is obtained:

$$\frac{(\beta + 1)bG}{-a_1} < \frac{I_v}{-g_{\text{min}} |V_1|}$$

Notice the left side of this design criterion is determined solely by the prescribed eigenvalues and the right side by the RTD nonlinearity.

Approximating the minimum conductance as the average negative conductance and the oscillation amplitude as an integer scalar of the voltage range of the negative resistance region

$$-g_{\text{min}} \equiv \frac{I_p - I_v}{V_v - V_p} \quad |V_1| \equiv n(V_v - V_p)$$

an alternative to Equation (10.9) is obtained.

$$\frac{I_p}{I_v} < 1 + \frac{-a_1}{nbG(\beta + 1)}$$

It must be emphasized that these results are based on a nearly sinusoidal limit cycle rather than for chaos. When the system bifurcates from a limit cycle to chaos, energy is spread across the spectrum rather than having it focused at a fundamental frequency and a few higher harmonics. Therefore, the envelope of the transconductance current can
actually become much smaller. So this criterion makes a good design margin for chaos applications, but it does not insure against chaos. From simulation experience, it was apparent that a derating constant could be applied to Equation (10.9) to insure against chaos. This constant might be predicted from the prescribed eigenvalues and is worthy of future study.

10.4 An Example

To illustrate the proposed criterion, an example is necessary. From the prescribed eigenvalues of Chapter 9, Equation (10.9) becomes

\[
\frac{I_v}{-g_{\text{min}} |V_1|} > 29
\]  

(10.12)

Suppose the three-terminal RTD to be used has an I-V characteristic as given by Figure 10.2.

This device has a \( g_{\text{min}} \) of -0.2 mho and the expected oscillation amplitude of approximately 0.3V. The minimum required device valley current for this set of prescribed eigenvalues is 1.74mA. From Figure 10.2, the valley current is only 107\( \mu \)A. This device is not a good candidate for the chaos design.

To confirm the predictions, PSpice simulations are run on the device of Figure 10.2 with no transconductance current limitation. The chaotic circuit parameters of Equation (9.30) are used. By slightly increasing the feedback gain, the circuit goes into a limit cycle.
and the required valley current expression is in agreement with the simulation results. Decreasing the feedback gain to its chaotic value, the peak to peak envelope of the transconductance current drops to about \(200\mu\text{A}\). Although the first quadrant device is still inadequate, the requirements for chaos are not as stringent as calculated from Equation (10.9), hence, the need for a derating procedure.

10.5 Summary

In this chapter, a simple design criterion was developed to choose which RTD’s are suitable candidates for synthesis of a prescribed set of Chua circuit eigenvalues. The proposed criterion provides a practical design margin for the chaos synthesis, but violating the criterion does not rule out the possibility of chaos. This result is a consequence of the frequency spreading nature of chaotic systems.
11. EXPERIMENTAL VERIFICATION

11.1 Introduction

As with any work of this nature, experimental results are worth their weight in gold. The simulations give good support, but a physical example is virtually irrefutable. In this chapter, experimental results are presented to support the proposed I-V characterization method and a practical chaotic circuit is synthesized from a three-terminal N-shaped conductance device.

11.2 An Experimental I-V Characterization

In Chapter 4, a novel method was proposed for obtaining a correct characterization of the NDC region for the N-shaped device. For this work, a two-terminal N-shaped device was created with the circuit of Figure 11.1 and its full I-V characteristic is shown in Figure 11.2. This device was designed so a full characterization could be easily performed. The raspyness of the trace is a noise problem that results from a hasty breadboard design.

![Experimental circuit with N-shaped conductance characteristic.](image)

Fig. 11.1. Experimental circuit with N-shaped conductance characteristic.
The $g_{\text{min}}$ of this device is approximately $-175 \mu \text{mho}$. To investigate the proposed characterization method, the following test circuit is designed.

![N-shaped device test configuration](image)

Fig. 11.3. N-shaped device test configuration.

The design parameters were chosen by convenience and lead to oscillation when the device is biased in the NDC region. This is easily predicted by the stability plot method of Chapter 2.

$$R = 952 \text{ Ohm}, \quad L = 200 \text{ mH}, \quad R_{L} = 21 \text{ Ohm}, \quad C = 10 \text{nF} \quad (11.1)$$

As expected, performing an I-V characterization leads to the erroneous results of Fig. 11.4. The data in the NDC region was obtained from the average values of current and voltage measured by DC meters.
For this experiment, the amplitude of the fundamental frequency of the oscillation is estimated to be one half the peak to peak voltage. Measuring the three quantities as proposed in Chapter 3, the following table of data is obtained.

Table 11.1
Experimental characterization data.

<table>
<thead>
<tr>
<th>V_{AVE} (Volts)</th>
<th>I_{AVE} (Amps)</th>
<th>AR/Z_{0} (mVolts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.69</td>
<td>0.310</td>
<td>52.8</td>
</tr>
<tr>
<td>1.75</td>
<td>0.280</td>
<td>112.5</td>
</tr>
<tr>
<td>1.87</td>
<td>0.240</td>
<td>195.5</td>
</tr>
<tr>
<td>1.98</td>
<td>0.227</td>
<td>230.0</td>
</tr>
<tr>
<td>2.09</td>
<td>0.222</td>
<td>250.0</td>
</tr>
<tr>
<td>2.19</td>
<td>0.221</td>
<td>265.5</td>
</tr>
<tr>
<td>2.28</td>
<td>0.221</td>
<td>273.0</td>
</tr>
<tr>
<td>2.39</td>
<td>0.223</td>
<td>284.0</td>
</tr>
<tr>
<td>2.48</td>
<td>0.224</td>
<td>284.0</td>
</tr>
<tr>
<td>2.58</td>
<td>0.226</td>
<td>287.0</td>
</tr>
<tr>
<td>2.67</td>
<td>0.228</td>
<td>287.0</td>
</tr>
<tr>
<td>2.79</td>
<td>0.221</td>
<td>258.0</td>
</tr>
</tbody>
</table>
Employing the method proposed in Chapter 4, a sixth-order polynomial splice is obtained (using every other data point in Table 11.1) to trace the NDC region. *Mathematica* was used to solve the linear system and gives Equation (11.2) and the splice is shown in Figure 11.5.

\[
I = (0.001) \cdot (0.0192V^6 - 0.2622V^5 + 1.385V^4 - 3.464V^3 + 3.918V^2 - 13.22V) \quad (11.2)
\]

Fig. 11.5. Result of proposed characterization method.

11.3 An Experimental Chaotic Circuit with the Three-Terminal Device

To demonstrate the success of the chaos synthesis approach of Chapter 9, an experimental circuit was designed with the parameters given by Equation (9.30) and the circuit configuration of Figure 9.6. The three-terminal device itself was designed by methods similar to the two-terminal device and the I-V characteristic is shown in Figure 11.6. The chaotic results are shown in Figure 11.7.
Fig. 11.6. Three-terminal device I-V characteristic.

Fig. 11.7. Experimental chaos results.

11.4 Summary

The results of this chapter verify the theoretical predictions of this thesis. But even more importantly, they demonstrate that the methods presented herein are indeed practically useful.
12. RESEARCH SUMMARY

12.1 Reviewing the Problem

The original problems to be addressed by this work were experimental I-V characterizations of the two-terminal N-shaped conductance, a figure of merit for switching speed with the three-terminal device, an investigation of the possibility of unwanted dynamics in a switching configuration, and a practical synthesis approach to using the three-terminal device in an autonomous chaotic modulator.

12.2 The Problem Solution

Solving these problems was not a straightforward venture. The approach taken was to develop engineering intuition and results that lent themselves directly to other applications as was occasionally shown throughout the study. To conclude this thesis, a short summary of the solution to each problem is now presented.

12.2.1 Experimental I-V characteristics

The fundamental problem in the strange I-V characteristics seen in the research literature is caused by the dynamic bias which exists under nonlinear oscillation. This phenomenon is a direct consequence of energy balance over one cycle of the oscillation. To solve the problem, a harmonic balance technique was employed to determine how the oscillation affects the bias. Developing an instrumentation technique from these results, a much better I-V characterization is obtained.

12.2.2 Switching speed figure of merit for the three-terminal device

Since the proposed advantage of the device is the NDC region, a figure of merit was obtained from the time it takes the device to transverse this region when switched. This figure captured the advantages of the NDC and gave a method to compare these new
devices to each other and to traditional transistors. Also, the study showed that the Miller capacitance effect is not an issue with this design.

12.2.3 An autonomous chaos modulator

By using the three-terminal device in a negative feedback configuration, it was shown that a practical chaos modulator could be synthesized. The advantage of this device and negative feedback is that the linear circuit parameters can be forced to be passive. This is a practical criterion which has not been easily realized with other configurations. A successful synthesis method was developed and both simulation and experimental results were presented.

12.2.4 Undesirable dynamic behavior and the switching configuration

Evidence that configurations being proposed for logic designs might have unwanted dynamics was a direct extension of the synthesis result. Forcing the linear components to be passive was the first step, but chaotic mappings were found which gave identical load line designs to those being posed for the switching applications. By looking at the spectrum of the autonomous circuit feedback voltage during chaos, frequencies and amplitudes of interest could be identified. Removing the feedback and driving with a sinusoid near these frequencies, almost periodic and beating effects were observed due to the loss of injection locking. This result is definitely an undesirable one for switching. PSpice simulations suggest chaos may also be possible, but the numerical noise in the simulator itself has left some doubt.
LIST OF REFERENCES


