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Atomic force microscope local oxidation nanolithography of graphene

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We demonstrate the local oxidation nanopatterning of graphene films by an atomic force microscope. The technique provides a method to form insulating trenches in graphene flakes and to fabricate nanodevices with sub-nanometer precision. We demonstrate fabrication of a 25-nm-wide nanoribbon and submicron size nanoring from a graphene flake. We also found that we can write either trenches or bumps on the graphene surface depending on the lithography conditions. We attribute the bumps to partial oxidation of the surface and incorporation of oxygen into the graphene lattice. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2976429]

Recently graphene has received special attention due to its remarkable electronic properties.[1–6] The most commonly used method for the fabrication of graphene nanodevices has used conventional electron-beam lithography and subsequent plasma etching.[7–11] On the other hand, alternative lithography techniques, especially those based on scanning probe microscopy, have shown great potential for patterning various materials at nanoscale.[12] Atomic force microscopy (AFM)-based local anodic oxidation (LAO) lithography has been used to fabricate micro- and nanostructures on metallic or semiconductor surfaces.[13–15] In particular, AFM has been used to cut carbon nanotubes[16] or etch holes in highly oriented pyrolytic graphite (HOPG).[17] The advantages of LAO include the ability to pattern surfaces with nanometer resolution and to examine devices during the lithography process, and easy tuning of the fabrication. LAO nanolithography is performed in the ambient environment and eliminates several fabrication steps, such as photoresist processing needed in conventional lithography. The main disadvantage of LAO—shallow oxidation of materials—should not be an issue when pattering a few layers of graphene. Moreover, atomic resolution of freshly cleaved graphite is routinely achievable in mainstream scanning probe microscopy, thus atomic control of oxidation is possible. In this letter we report direct LAO of graphene flakes. As an example, we fabricate a 25-nm-wide nanoribbon and a submicron nanoring in a single layer graphene. We also report that under certain conditions we can form bumps on the surface of graphene flakes instead of trenches. This may indicate partial oxidation and incorporation of oxygen into the graphene lattice instead of formation of volatile carbon oxide.

We have characterized LAO patterning of graphene flakes with thickness ranging from one to several atomic layers. Our graphene sheets were mechanically exfoliated from a natural graphite and transferred onto a 300-nm-thick SiO_2 on a heavily doped Si substrate. The graphene flakes are identified by their color contrast under an optical microscope followed by thickness measurements by AFM. Cr/Au (3/50 nm) electrodes were fabricated by electron-beam lithography and metal deposition before or after LAO lithography.

We use a Veeco Dimension 3100 AFM system with an environmental enclosure with controlled humidity. The system has a noise floor ~0.3 nm in the lateral directions, precluding atomic resolution of graphene. For both imaging and lithography, a conductive silicon tip was used in a noncontact (tapping) mode in which constant height is maintained using optical feedback. The sample substrate is grounded. A small negative bias voltage (amplitude of 15–30 V) is applied on the tip, creating an electric field large enough to induce electrochemical oxidation of the sample at room temperature. The bias voltage is modulated between zero and the set value with a 100 Hz square wave to help stabilize a water meniscus around the tip. We find that electrical grounding or floating of the graphene itself makes no significant difference for the LAO.

We first demonstrate that LAO can be used to electrically isolate different regions in a graphene flake. Figure 1(a) shows a test flake before patterning with a resistance of 6.3 kΩ measured between left and right electrodes. A line

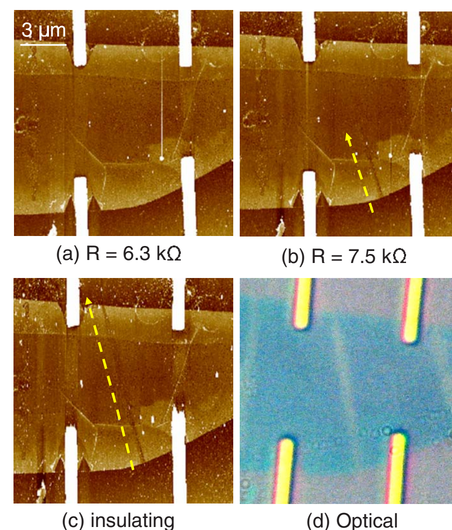

FIG. 1. (Color online) (a) AFM image of an uncut graphene flake (thickness ~5 nm). The four white bars in the picture are the metal contacts. The two-terminal resistance was 6.3 kΩ. (b) A trench was cut from the edge to the middle of the flake, along the direction indicated with the dashed arrow. The resistance increased to 7.5 kΩ. (c) The trench was cut through, electrically insulating the left and right parts of the flake. (d) Optical microscope image of the same flake with trenches.

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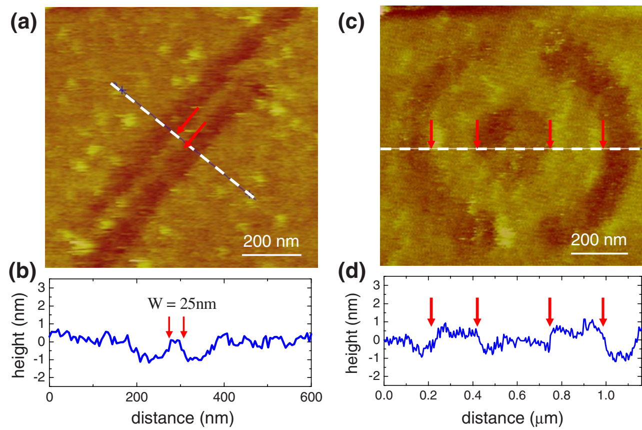

FIG. 2. (Color online) (a) AFM image of a nanoribbon fabricated on a graphene flake with thickness ~1 nm. The width and length of the ribbon are 25 and 800 nm, respectively. (b) Height profile along the dashed line in (a). (c) A nanoring (inner radius ~160 nm, outer radius ~380 nm) patterned on a graphene flake. Two long trenches, not shown in the picture, were subsequently drawn from the circumference of the ring outward to the edges of the flake to electrically isolate the ring device. (d) Height profile along the dashed line in (c).

written across half of the flake using LAO results in a small increase in that resistance to 7.5 kΩ [Fig. 1(b)]. As the line is continuously cut through the whole flake in the subsequent lithography step, the resistance across the line becomes infinite [Fig. 1(c)]. The line is barely seen in the AFM image but is clearly seen under the optical microscope [Fig. 1(d)]. The width of the line from the optical image is overestimated by a factor of 5.

Several graphene nanodevices have been fabricated using the LAO technique. In Fig. 2(a) we show a graphene nanoribbon formed between two LAO-patterned trenches. The width of an 800-nm-long ribbon is ~25 nm, the trench depth is equal to the flake thickness of ~1 nm (corresponding to one to two layers of graphene). In Fig. 2(c), a ring pattern fabricated by LAO is shown. The inner and outer radii of the ring are 160 and 380 nm, respectively. The width of the conducting region of the ring is 220 nm. We have characterized the conductance (G) of the ring (additional trenches were cut to confine the current in the flake to flow through the ring). At temperature $T<50$ K we observe reproducible fluctuations of conductance as a function of magnetic field (B) or gate voltage (V_g), shown in Fig. 3. We attribute these fluctuations to universal conductance fluctuations[7,18–20] (UCF) in such a mesoscopic device. From the UCF in $G(B)$ we estimate a phase coherence length via $B_c l_\varphi^2 \approx \phi_0$, where B_c is the correlation field and $\phi_0 = h/e$ is a flux quantum. At 4.2 K, thus calculated $l_\varphi \sim 90$ nm is much smaller than the 1.7 μm circumference of the ring, consistent with the absence of Aharonov–Bohm oscillations[7,21] in our device.

The formation of trenches as described above can be understood as due to the oxidation of graphene into volatile carbon oxides under the AFM tip.[22] On the other hand, we have found that for certain LAO conditions we can form bumps rather than trenches on graphene flakes as well as on HOPG. The conditions that result in trenches or bumps can be controlled by the combination of a set point voltage (which controls the tip-sample distance in the dynamical mode) and tip bias voltage. In general, lower bias voltages and/or lower set points (SPs) result in bumps, while higher bias voltages and/or higher set points result in trenches. In Fig. 4(a) 6 lines (from left to right) are written with the same tip voltage of −20 V while SP was cycled through 0.3, 0.2, 0.1, 0.3, 0.2, and 0.1 V, which correspond to 15%, 10%, 5%, 15%, 10% and 5% of the free-oscillation amplitude for an unloaded tip, respectively. While higher SP=0.3 and 0.2 V consistently result in formation of trenches, bumps are written for the SP=0.1 V. Alternatively, the type of writing can be controlled by the tip bias voltage. In Fig. 4(b) all the lines are written with the same SP=0.2 V while the tip bias voltage varied between −20 and −18 V for the lines marked by dashed arrows (left to right) and −16 V for the rightmost line marked with the solid arrow. This rightmost line is a bump rather than a trench. All the lines have similar morphology and are indistinguishable in a frictional mode image [Fig. 4(c)]. We speculate that at low bias voltages and low SP voltages, the AFM tip partially oxidize the graphene into *nonvolatile* graphene oxide (GO) with some oxygen incorporated into the graphene lattice. GO is known to have a larger layer thickness[23] than graphene, therefore corresponding to bumps on graphene or graphite surfaces.

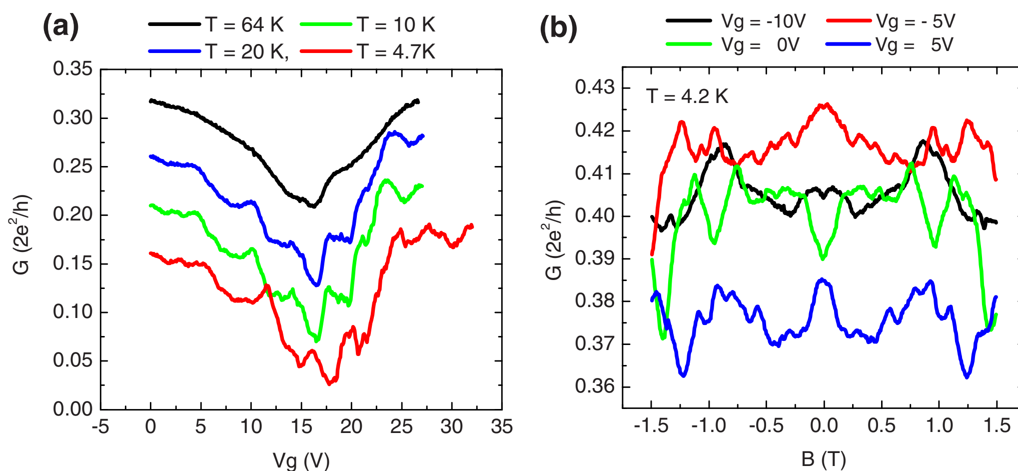

FIG. 3. (Color online) (a) Conductance fluctuations as a function of gate voltage for several temperatures in the ring device in Fig. 2(c). The three curves for $T=20$, 10, and 4.7 K were offset by −0.05, −0.1, and −0.15 (in units of $2e^2/h$), respectively. (b) Magnetoconductance of the ring at various gate voltages measured at 4.2 K.

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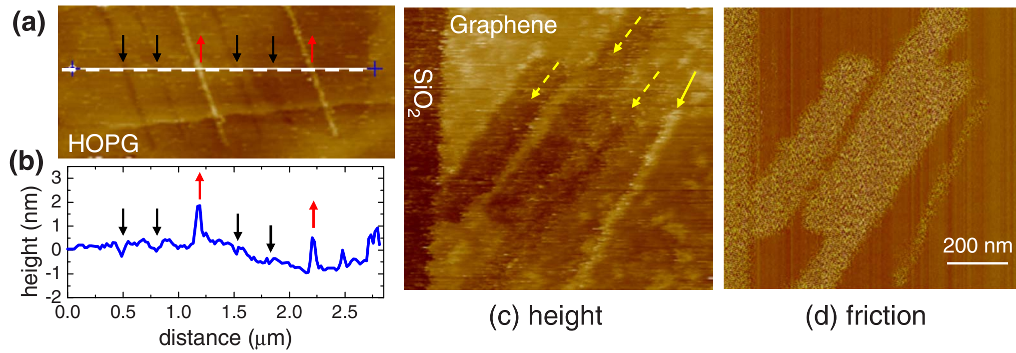

FIG. 4. (Color online) AFM images of line patterns created by the LAO technique. (a) Trenches or bumps were formed on HOPG surface. Six lines (from left to right) are written with the same tip bias voltage of −20 V while the set point was cycled through 0.3, 0.2, 0.1, 0.3, 0.2, and 0.1 V, corresponding to 15%, 10%, 5%, 15%, 10%, and 5% of the free-oscillation amplitude for an unloaded tip. (b) Height profile across the line marked in (a). Red arrows indicate bumps and black arrows indicate trenches. (c) Height image of three trenches and one bump patterned on a graphene flake (∼1 nm in thickness). The dashed arrows indicate trenches; the solid arrow indicated a bump. (d) The frictional force image at the same area as in (c).

After our study has been completed, we became aware of a recent related work,[24] where the authors also used AFM to etch trenches in graphene, but only originating from the edges of the flake. In contrast, we have demonstrated writting oxidation lines originating either from the edges or from the middle of the flake, and in both forms of trenches and bumps.

To summarize, we have demonstrated AFM-based LAO on graphene. The lithography is capable of producing small features (<25 nm) with subnanometer spacial resolution, allowing *in situ* monitoring of the device parameters (such as dimensions or electrical conduction) during the fabrication and easy tuning of the fabrication. We also found that we can write either trenches or bumps on the graphene surface depending on the lithography conditions. We attribute bumps to partial oxidation of the graphene with oxygen incorporated into the graphene lattice.

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