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Short Communication

Single-walled carbon nanotube transistors fabricated by advanced alignment techniques utilizing CVD growth and dielectrophoresis

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ABSTRACT

Single-walled carbon nanotube field effect transistors (SWNT-FETs) are fabricated by two different alignment techniques. The first technique is based on direct synthesis of an aligned SWNTs array on quartz wafer using chemical vapor deposition. The transistor with three SWNTs and atomic layer deposited (ALD) Al₂O₃ gate oxide shows a contact resistance of 280 KΩ, a maximum on-current of −7 μA, and a high I_{on}/I_{off} ratio (>10³). The second technique is based on room temperature self-assembly of SWNT bundles using dielectrophoresis. By applying AC electric fields, we have aligned nanotube bundles between drain and source contact patterns of a transistor at room temperature. Transistors based on twisted bundle of SWNTs show high contact resistance (MΩ range) and low current drive in the order of tens of nA.

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1. Introduction

Since their discovery in 1991 [1], carbon nanotubes (CNTs) have been the focus of extensive research for many potential applications, including sensing, chemistry, biology, and electronics [2–4]. Due to perfect one-dimensional crystalline structure, SWNTs exhibit unusual physical, chemical, mechanical and electrical properties. Single-walled carbon nanotube field effect transistors (SWNT-FETs) were first demonstrated in 1998 [5]. It has been shown that these transistors can achieve ballistic transport and can sustain high current densities while dissipating very low DC powers [5–6]. Despite the advantages of SWNT-FETs, these devices have not been utilized in industry due to two major hurdles in realization of large area and/or complex circuits based on these transistors. These two issues are: (1) Difficulty in the separation of semiconducting from metallic single-walled carbon nanotubes. (2) Difficulty in alignment and placement of the nanotubes to the device structure in a controlled and reproducible pattern.

Up to now, various methods for selective deposition or growth of single walled carbon nanotubes (SWNTs) on two electrodes have been developed [7–10]. In this paper, we have fabricated, characterized and compared SWNT-FETs fabricated by two advanced

aligning techniques. In the first technique, alignment of nanotubes is achieved through high temperature CVD synthesis of nanotubes on a quartz wafer. Parallel arrays of individual SWNTs with a controlled density are utilized to construct high performance SWNT-FETs. This technology allows implementation of SWNT-FETs with low contact resistance, high mobility, and high saturation current. In the second method, room temperature device fabrication is achieved based on dielectrophoresis. SWNT bundles suspended in ethanol solution display a positive dielectrophoresis which facilitate their alignment and placement through a very simple processing technology. Electrical performance of these devices is limited by their high contact resistance of SWNT bundles which is in the order of a few MΩ. Based on the observed electrical characteristics, it can be concluded that individual nanotubes in the channel achieve lower contact resistance than the nanotubes in a bundle, resulting in better overall device performance.

2. The aligned array SWNT-FETs in CVD growth

Aligned SWNT arrays are grown on miscut single-crystal quartz substrate by thermal CVD. Quartz wafer is annealed for 8 h at 900 °C in air. Single-walled carbon nanotubes (SWNTs) are synthesized by chemical vapor deposition (CVD) of methane on the substrate using iron catalyst. Source and drain contacts are formed by electron beam deposition of Pd metal. Al₂O₃ films are deposited

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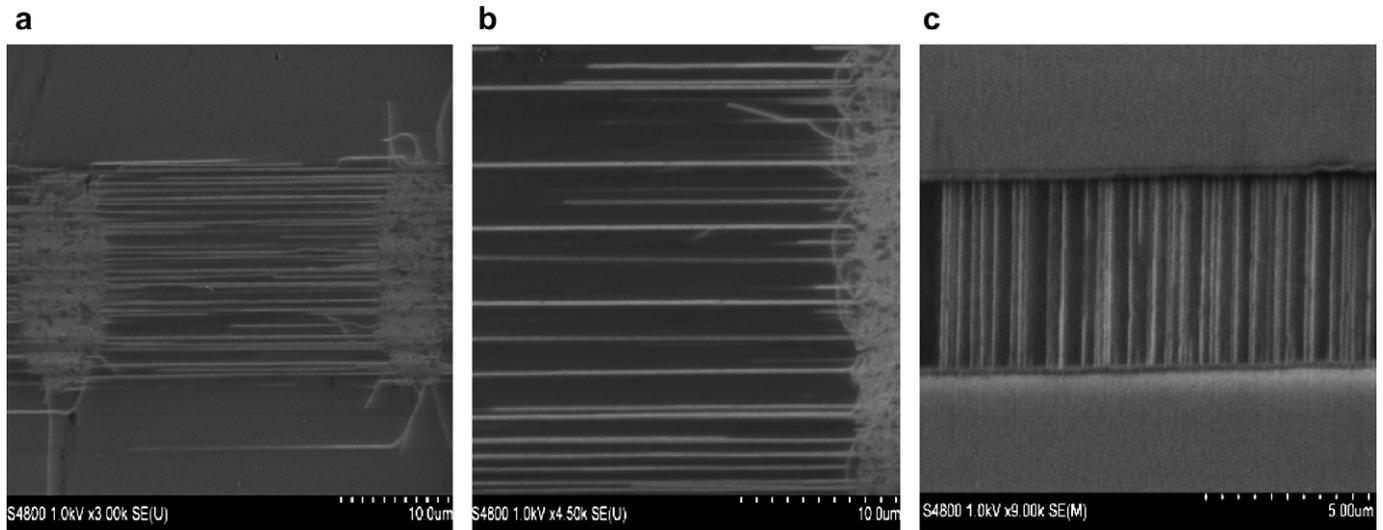


Fig. 1. Scanning electron microscope (SEM) images of aligned SWNT arrays on quartz wafer. (a) SEM images of the grown aligned arrays of SWNTs using patterned iron catalysts with spacing 10 μm . (b) The enlarged image the edge of catalyst. The SWNTs in corner of a catalyst still shows the tube-tube crossing. Pd patterns of source and drain cover in the tube-tube crossing entirely. (c) The SEM images of perfectly aligned arrays SWNT between source and drain spacing 3 μm with width of 15 μm .

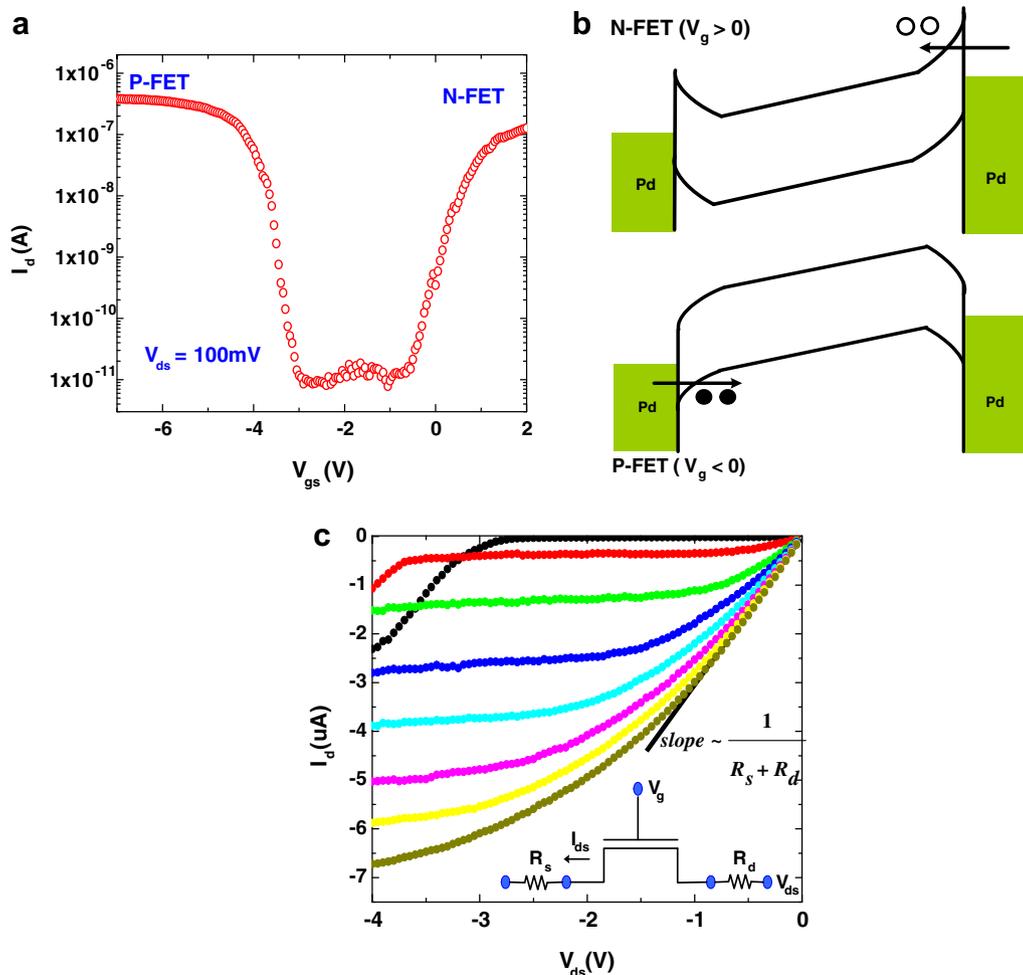


Fig. 2. Output characteristics of an aligned array SWNT-FET with a 50 nm thick ALD Al_2O_3 oxide. (a) The transfer characteristics of transistor with a width of 6 μm . (b) Energy band diagram for an ambipolar characteristic of SWNT-FETs depending on whether $V_g > 0$ or $V_g < 0$. (c) The I_d - V_{ds} curves of an aligned array SWNT-FET (inset). The equivalent circuit of SWNT-FET with source and drain resistance (contact resistance).

using ASM Micro-chemistry F-120 ALCVD™ Reactor. ALD Al_2O_3 (50 nm) layers are grown on SWNTs at 300 °C by using precursor of $\text{Al}(\text{CH}_3)_3$ (the Al precursor) and H_2O (the oxygen precursor). Cr/Au (20/400 nm) gate electrodes are finally deposited.

Nearly perfect alignment of SWNTs can be achieved with direct growth on miscut quartz as shown in Fig. 1. The degree of alignment is influenced by annealing of quartz before SWNT growth. Increasing the annealing time, which increases the degree of order in the crystal lattice near the surfaces as well as the degree of order of the steps, improves SWNT alignment [8–9]. SWNTs are parallel to the ST-miscut quartz from catalyst patterns. Fig. 2c shows SWNTs between source and drain are parallel with non tube-tube cross. The use of a well-aligned SWNT array allows devices in which the current flow is through a number of individual SWNTs. Therefore, individual SWNTs can sustain their intrinsic mobility in an aligned array of SWNTs.

Fig. 2 shows the I_V characteristics for a 1.5 μm gate length aligned array of SWNT-FETs with a 50 nm thick Al_2O_3 . Fig. 2a and c shows the electric characteristics of aligned SWNT array-FETs with a width of 6 μm having the maximum intrinsic transconductance $g_m = dI_d/V_{gs}I_{V_{ds} = 0.1 \text{ V}}$ of 0.5 μS and the maximum on-current of $-7 \mu\text{A}$. The $I_{\text{on}}/I_{\text{off}}$ for a SWNT-FET with three semiconducting SWNTs is high and equal to 4×10^4 . The I_V curves of SWNT-FETs resemble an ambipolar behavior, exhibiting an operating regime at positive and negative V_{gs} . Consider now the case where Fermi-

energy (E_F) is located around midgap. For the positive gate bias, the conduction band pushes down, and the Schottky barrier becomes narrower, resulting in an increase of electron tunneling current (N-FET). For the negative gate bias, the valence band pulls up, leading to an increase of hole tunneling current (P-FET) as shown in Fig. 2b. The slope of the I_V curves at high gate voltages and low drain voltages (linear region) is roughly the inverse of the extrinsic source and drain resistances $R_s + R_d$. From Fig. 2c, the estimated drain and source contact resistance is around 280 $\text{k}\Omega$. In this case, Pd metallization efficiently lowers the contact resistance, since individual nanotubes can be reached by Pd metallization.

3. Device fabrication using dielectrophoresis

We have used SWNTs with diameters of $\sim 1.5 \text{ nm}$ synthesized by laser ablation from Carbon Nanotechnologies Inc. Au metal patterns are deposited on a thermally grown SiO_2 with a thickness of $t_{\text{ox}} = 150 \text{ nm}$ on P + Si substrate. The gap size between the Au electrodes is 4 μm and the width of the electrodes is 5 μm . Single-walled nanotubes suspended in ethanol with a concentration of 10 ng/ml are first subjected to ultrasonic vibration for several hours in order to untangle the nanotubes. Once AC electric fields (5 MHz) between all source/drain Au metals are established, diluted ethanol with suspended nanotubes is applied on the SiO_2 surface. Dipoles of SWNT bundles are induced under an external

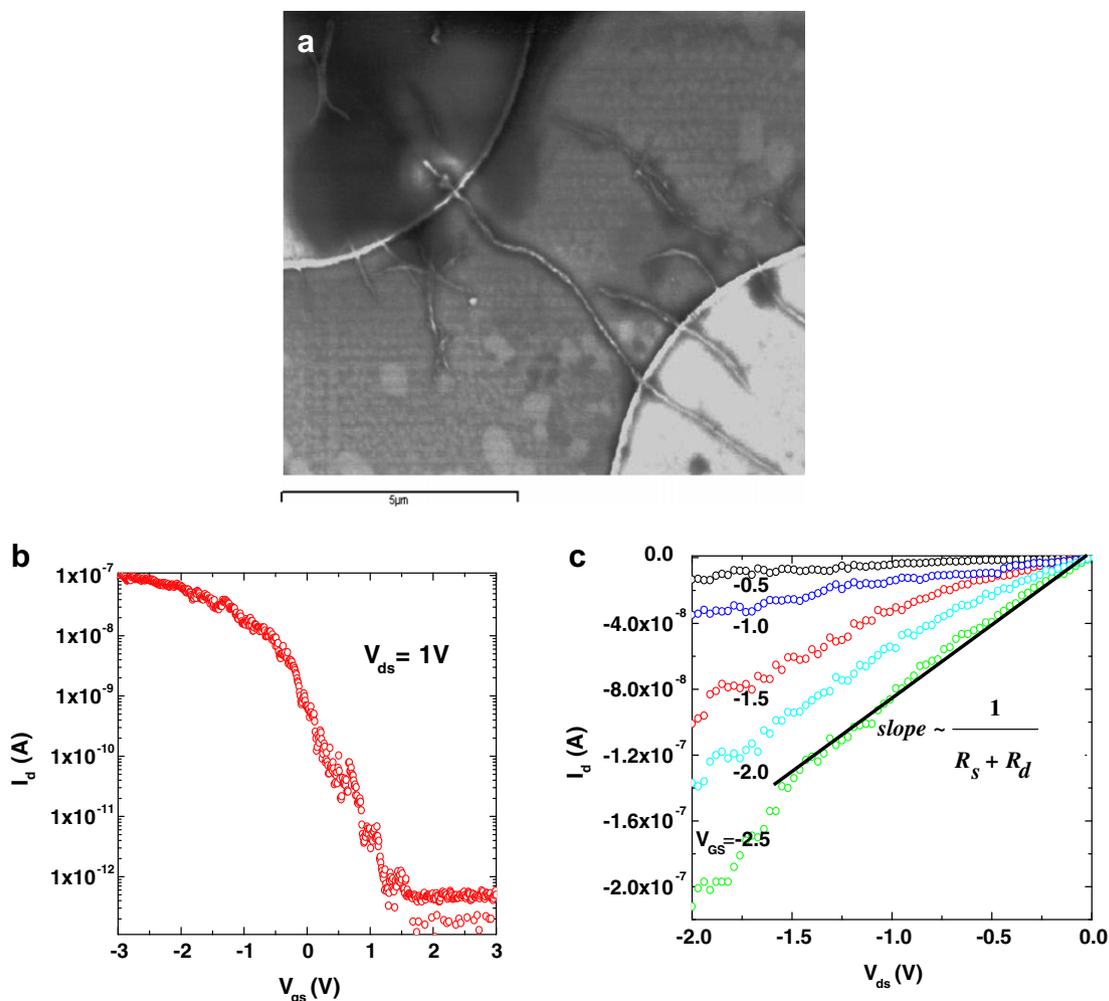


Fig. 3. (a) SEM images of an aligned pattern using dielectrophoresis in the condition of DC = 0 V, AC = 2.3VPP, frequency = 5 MHz. DC Characteristics of single-walled carbon nanotube transistors fabricated using dielectrophoresis. The device has a bundle of SWNTs with 15 nm diameter. (b) I_d - V_{gs} characteristics which also shows an ambipolar characteristics with N-FET threshold voltage above the sweeping voltage of +3 V. (c) I_d - V_{ds} characteristics of transistor.

electric field. The AC electric fields are applied until the ethanol solution completely dries at room temperature. Following the ethanol evaporation, 6 μm width of source/drain Pd metals with spacing 1.5 μm are deposited on the Au electrodes, and patterned to form contacts on nanotube.

In order to find an optimal deposition and alignment condition, the amplitudes of AC signals are changed step by step. The optimal condition of AC signal for the deposition and alignment is empirically found to be a field with an amplitude of 0.6 V/ μm (frequency of 5 MHz) as shown in Fig. 3a [10]. Under optimized condition, the aligned SWNT-FETs are highly reproducible with a yield of about 70% with one bundle of nanotube per device with an average bundle diameter of 15 nm. For further discussion, a SWNTs bundle is assumed to be an isotropic ellipsoid. The induced DEP torque acting on the bundle under an external electric field (E) can be expressed as [11]

$$T_{\text{DEP}} = \frac{\pi r^2 l}{2} \varepsilon_1 \frac{(\varepsilon_2 - \varepsilon_1)^2}{[\varepsilon_1 + (\varepsilon_2 - \varepsilon_1)L_{\parallel}][\varepsilon_2 + \varepsilon_1]} E^2 \sin 2\theta \quad (1)$$

where r , and l are the radius and length of SWNTs bundle. ε_1 and ε_2 are the permittivity of the ethanol and SWNTs bundles. $L \approx 4r^2/l^2 [\ln(1/r) - 1]$ and θ are the depolarization factor and the angle between the axis of the SWNTs bundle and the external field, respectively. Moreover, a net DEP force exerts on the bundle is

$$F_{\text{DEP}} = \frac{\pi r^2 l}{2} \varepsilon_1 \text{Re} \left(\frac{(\sigma_2^* - \sigma_1^*)}{[\varepsilon_1^* + (\varepsilon_2^* - \varepsilon_1^*)L_{\parallel}]} \right) \nabla E^2 \quad (2)$$

where l are the radius and length of SWNTs bundle. ε_1 and ε_2 are the permittivity of the ethanol and SWNTs bundles. σ_1 and σ_2 are the conductivity of the ethanol and SWNTs bundles, respectively. Since $(\varepsilon_2 - \varepsilon_1) > 0$ and $(\sigma_2 - \sigma_1) > 0$ the real part of $(\sigma_2^* - \sigma_1^*)/[\varepsilon_1^* + (\varepsilon_2^* - \varepsilon_1^*)L_{\parallel}]$ is positive. Therefore, SWNTs bundle would be expected to move toward the region of maximum electric field gradient, this is the outmost edges of round electrodes in the experiment [12], due to the net DEP force. In addition, the axis of SWNTs bundle would be expected to parallel to the electric field under steady-state condition, according to Eq. (2). The SWNTs bundle is well-aligned between two rounded electrodes by the combination of the transit and rotated forces, as shown in Fig. 3a.

Fig. 3b and c shows the typical DC characteristics for SWNT-FETs with $L = 1.5 \mu\text{m}$ fabricated using dielectrophoresis technique. Prior to IV measurements, electrical burning is performed to remove metallic SWNTs through self-heating of SWNTs at high drain currents. The extracted transconductance is found to be 52 nS for devices with one nanotube bundle. I_d - V_{ds} characteristics show current capabilities in several hundreds of nA range, which is at least one order of magnitude smaller than that of an aligned array SWNT-FET. Current saturation is not observed in these devices due to high contact resistances of source and drain estimated at around 10.1 M Ω . Strong van der Waals force causes SWNTs to tangle a twisted bundle in the solution. Due to twisted nature of these bundles, source/drain Pd metallizations do not reach individual SWNTs in the bundle. Moreover, carriers cannot freely move among adjacent SWNTs in a bundle, as the only conduction mechanism among SWNTs is tunneling current. This results in high resistance among adjacent SWNTs. Devices with $I_{\text{on}}/I_{\text{off}}$ ratio of higher than 10^3 show contact resistance values of 2.8–10.1 M Ω [13,14].

Recently there has been a report on high performance SWNT-FETs fabricated by single bundle SWNT. [15] In this work the nano-

tubes are suspended in 1,2-dichloroethane and are aligned to source/drain contact metallization using an AC electric field alignment technique similar to the dielectrophoresis technique reported here. The contact resistance of single bundle SWNTs is significantly reduced by a novel ultrasonic nanowelding technique, achieving near-ideal contact resistance of 10–20 K Ω per nanotube and an average maximum on-current of 10–15 μA per nanotube [15,16].

4. Conclusion

In this paper we report and compare IV characteristics of transistors based on aligned arrays SWNTs on quartz and single bundle of SWNTs using dielectrophoresis, where both devices have the same device geometries including gate length (1.5 μm), width of source drain contacts (6 μm), and Pd metallization. However, the position of the gate in the two devices is different. In the device composed of aligned nanotubes on quartz, the gate is above the nanotube separated by a 50 nm ALD Al_2O_3 gate oxide. In the device fabricated by dielectrophoresis, a 150 nm thermal SiO_2 separates the nanotube from the bottom gate. Both techniques achieve a high alignment of SWNTs between source/drain electrodes. The observed IV trends of SWNT-FETs are essential to contact individual nanotubes and not nanotube bundles for high performance. The transport in an aligned array of non-overlapping SWNTs provides low contact resistance, high mobility, and large on-current. On the other hand, transport between neighboring nanotubes of a twisted bundle in SWNT-FETs induces a high tunneling resistance in the range of 2.8–10.1 M Ω , which leads to high contact resistance, low transconductance, low maximum current, and non-saturating current-voltage behavior. In order to improve these problems, the ultrasonic nanowelding and untangling CNTs in the solutions helps SWNT-FET fabricated by dielectrophoresis to achieve high performance of transistor.

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References

- [1] Iijima S. Nature 1991;354:56.
- [2] Baughman RH. Science 2000;290:1310.
- [3] Cheung CL et al. Proc Natl Acad Sci USA 2000;97(8):3809.
- [4] Avouris Ph. Acc. Chem. Res. 2002;35:1026.
- [5] Tans SJ, Verschueren RM, Dekker C. Nature 1998;393:49.
- [6] Kim SK, Xuan Y, Ye PD, Mohammadi S, Back JH, Shim M. Appl. Phys. Lett. 2007;90:163108.
- [7] Nathan RF, Wang Q, Thomas W, Javey A, Shim M, Dai H. Appl. Phys. Lett. 2002;81:913.
- [8] Zhou Y, Gaur A, Hur SH, Kocabas C, Meitl M, Shim M, Rogers JA. Nano Lett. 2004;4:2031.
- [9] Kang SJ, Kocabas C, Ozel T, Shim M, Pimparkar N, Alam MA, Rotkin SV, Rogers JA. Nature Nanotechnology 2007;2:230–6.
- [10] Kim SK, Wang CJ, Shim MS, Mohammadi S. IEEE NANO 2005.
- [11] Benedict LX, Louie SG, Cohen ML. Phys. Rev. B 1995;52:8541.
- [12] Lee SW, Bashir R. Appl. Phys. Lett. 2003;83:3833.
- [13] Woo Y, Duesberg GS, Roth S. Nanotechnology 2007;18:095203.
- [14] Stahl H, Appenzeller J, Martel R, Avouris P, Lengeler B. Phys. Rev. Lett. 2000;85:5186.
- [15] Chen C, Xu D, Kong ESW, Zhang Y. IEEE Electron Device Lett. 2006;27:852.
- [16] Chen CX, Yan LJ, Kong W, Zhang YF. Nanotechnology 2006;17(March):2192–7.