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SUBTHRESHOLD LEAKAGE CONTROL BY MULTIPLE CHANNEL LENGTH CMOS (McCMOS)

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SUBTHRESHOLD LEAKAGE CONTROL
BY MULTIPLE CHANNEL LENGTH
CMOS (McCMOS)

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Subthreshold Leakage Control by Multiple Channel Length CMOS (McCMOS)*

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Abstract

In sub-micron CMOS design, non-minimum length transistors offer the possibility of achieving excellent leakage control without the disadvantages of other known leakage control techniques. Preliminary analyses indicate that one can expect leakage reduction by a factor of at least 100 (and possibly orders of magnitude higher) with only modest increases in circuit area and switched capacitance. This paper briefly reviews related leakage control techniques, describes the McCMOS technique, and presents simulation results that are indicative of the performance of the technique.

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1 Introduction

The most aggressive high performance CMOS designs today require extremely short channel transistors and low supply voltages close to 1V and lower in order to achieve maximum performance while keeping power and heat dissipation down to acceptable levels. A side effect of this progress has been the unavoidable use of low threshold transistors resulting in vastly increased leakage currents. Low power supply voltages force us to use low threshold voltages in order to maintain performances since propagation delay is roughly proportional to $\frac{V_{DD}}{V_{DD}-V_{TH}}$ for short channel devices. In addition, short channel lengths naturally lead to low threshold voltage; that are also subject to considerable variation due to variations in dopant quantities. Moreover, drain induced barrier lowering (V_{TH} reduction proportional to V_{DS}) and dopant variations become more and more pronounced as channels are shortened. We propose the use of multiple channel lengths as a means of alleviating the large leakage currents that result from short channel effects.

We have only been able to identify one previous application of multiple channel length CMOS design [1], but it was intended for multiple voltage applications not leakage control. The voltages involved were 5V and 3.3V, supply voltages for which low threshold voltages and leakage control are not

required. Researchers have documented other leakage control techniques that involve process modifications or use of bias voltages. One very effective approach is the MTCMOS (Multiple Threshold voltage CMOS) technique developed by Mutoh and others [8, 9]. In Mutoh's work, high and low threshold voltage devices are achieved by additional processing steps so as to obtain different doping levels in the channel of each transistor. The high threshold devices are placed between the power rails and the remaining lower threshold circuitry. When the high threshold devices are turned off (only during periods when the circuit is idle), leakage through the affected circuitry is reduced by orders of magnitude. Mutoh shows that the leakage of the high threshold device is on the order of $\frac{1}{1000}$ of the leakage of a same sized low threshold device. Other techniques include control of threshold voltage by means of substrate bias [6, 5], or by biasing the transistor source terminal [10] to obtain $V_{GS} < 0$ and a slight increase in threshold voltage.

2 McCMOS Technique

We propose to use increased channel lengths wherever needed to control leakage current. The effect of channel length on threshold voltage (and leakage) has been well documented [7, 2], demonstrating that V_{TH} decreases rapidly as effective channel length (L_{EFF}) is reduced. Usually this is viewed as a challenge to overcome in an effort to produce smaller devices. We propose that this behavior be exploited, where appropriate, to increase threshold voltage and lower leakage.

Figures 1, 2, and 3 present simulation results which demonstrate the savings possible when channel lengths are increased. All of the transistors indicated were simulated in HSPICE using a BSIM model for a 0.5u MOSIS process. The flat band voltage (V_{FB0}) was adjusted to simulate the effect of a reduced threshold voltage (approximately 0.25V). Three graphs; are presented. Figure 1 presents I_{DS} vs. V_{DS} given $V_{GS} = 1.5V$. This graph is used to illustrate the relative current drive capabilities for the device dimensions to be compared. Figure 2 presents the subthreshold characteristic of each device. Here we can see the impact of L_{EFF} on the subthreshold current. Figure 3 presents the I_{DS} of each device divided by the I_{DS} for the reference device ($W=3u, L=0.5u$). In the region where $V_{GS} < V_{TH}$, this graph indicates the factor of leakage savings (relative to a 3u/0.5u device). We see

that by increasing channel length alone from $0.5u$ to $1u$, we obtain a leakage savings ratio on the order of 250 while reducing current drive by about $\frac{1}{2}$. Increasing width to compensate for performance loss still allows us a 100 fold leakage improvement. The curves for a $W = 12u, L = 4u$ device show us that much greater savings are possible if we can tolerate the cost in area and capacitance. We anticipate much greater savings for smaller technologies on the order of $0.2u$ and lower for which the DIBL effect is more severe than at $0.5u$.

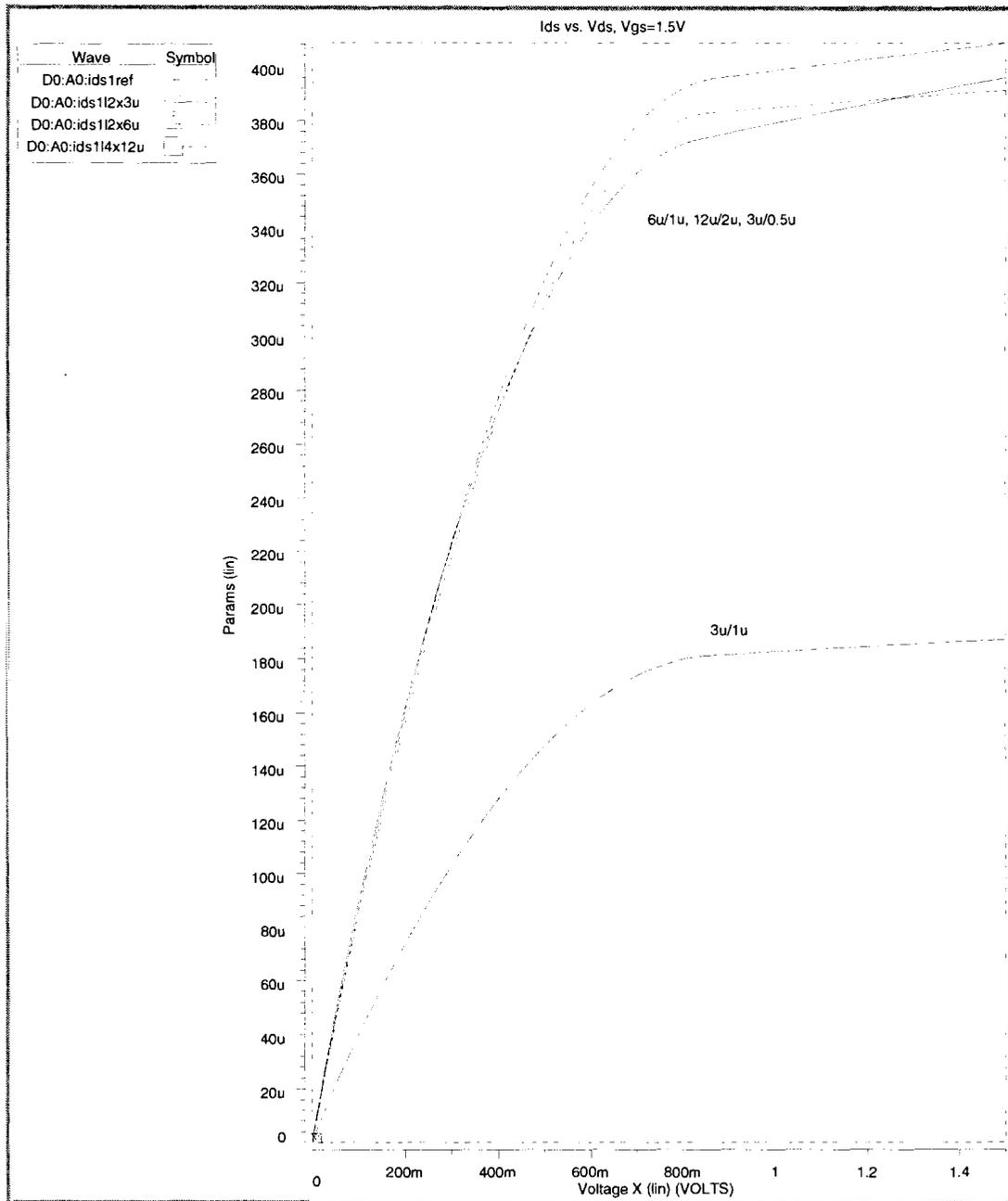


Figure 1: I-V curves for different transistor dimensions

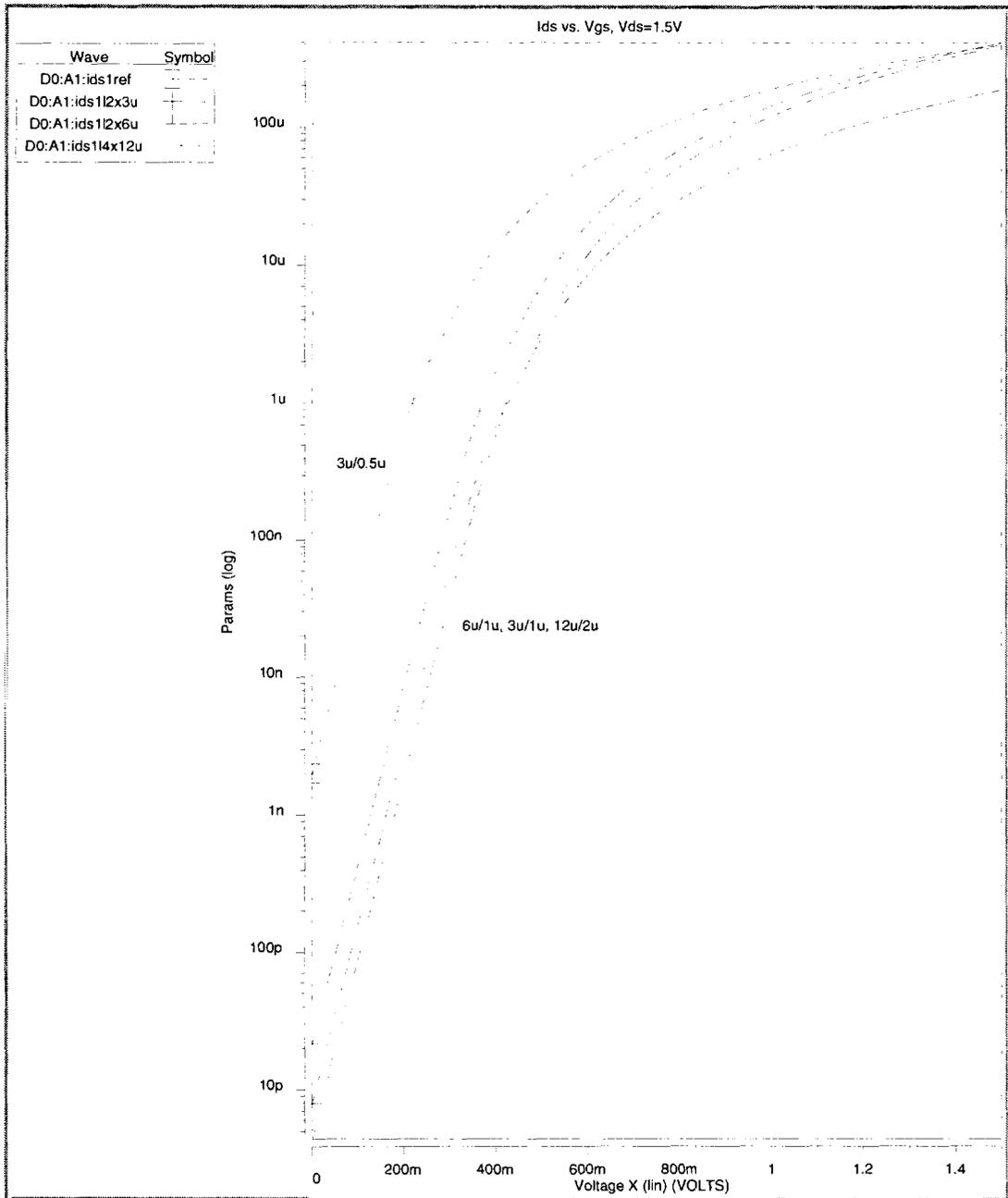


Figure 2: Subthreshold characteristic for different transistor dimensions

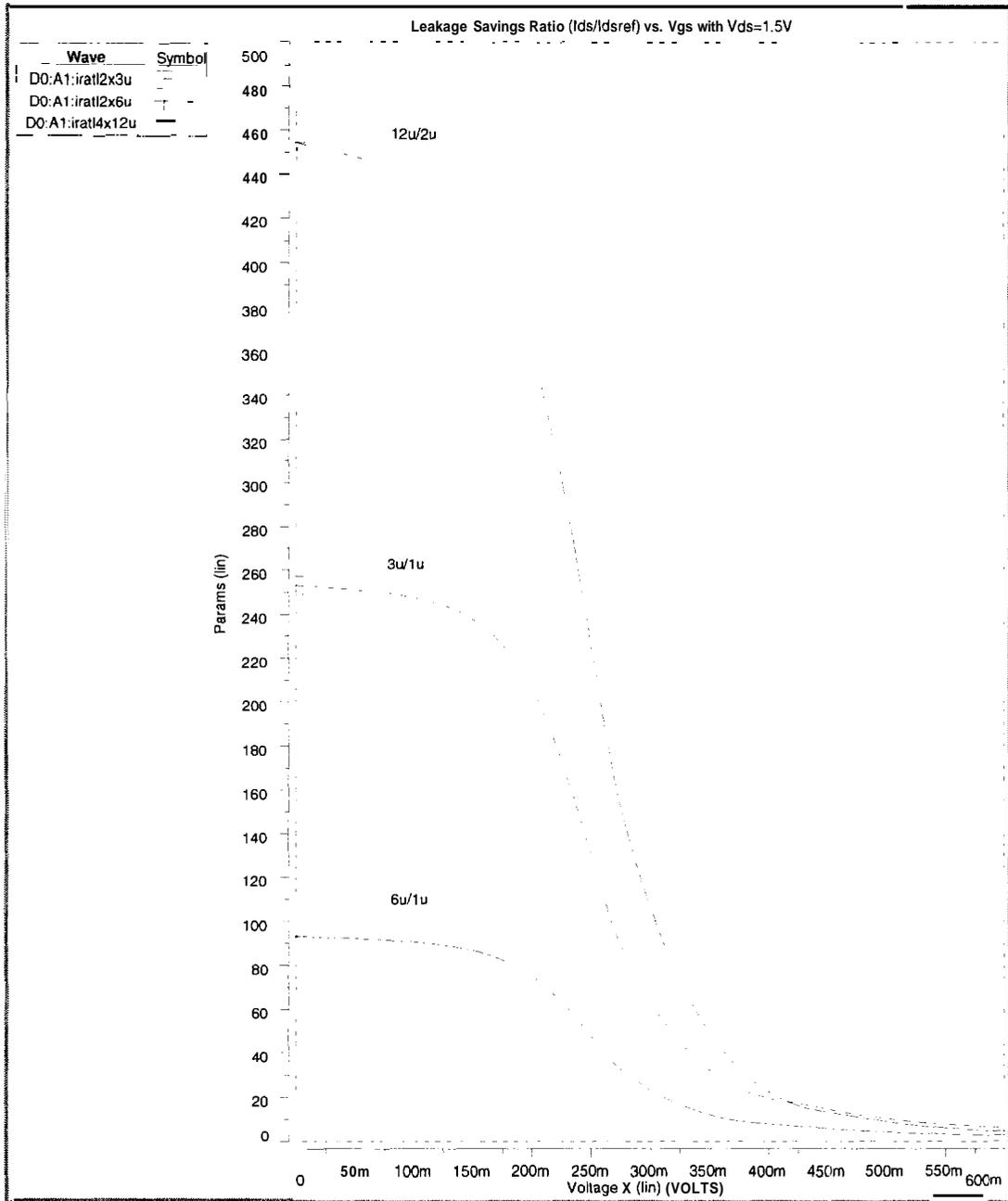


Figure 3: Leakage savings ratios relative to $3\mu/0.5\mu$ transistor

From these graphs, we propose two design principles to exploit the channel length vs. leakage relationship.

- In the non-critical path of a circuit we should increase the channel length of at least one transistor (preferably one with a high probability of being turned off) in each possible current path between V_{DD} and ground.
- In critical paths, apply the same technique but increase transistor width as necessary to maintain performance.

Clearly there are costs (area and switched capacitance) involved in this technique, but they are modest in comparison to other known techniques. Area costs should be no more than MTCMOS which requires the insertion of wide leakage control transistors. Area costs also should be mitigated by the fact that the channel area of any single transistor in the pull down or pull up path of a CMOS gate is a small fraction of the total gate area. Switching capacitance will also increase due to larger gates on some transistors. However, McCMOS is intended for operating conditions for which leakage power (in the absence of leakage control) can equal or exceed switching power. Under such conditions, leakage power savings should far exceed the increase in switching power.

The chief advantage of McCMOS over other leakage control techniques is simplicity. One merely needs to lengthen the drawn channel length of selected transistors. This can be accomplished with existing CAD tools and existing single V_{TH} processes. Other techniques require either additional processing steps or additional bias control circuitry that would not otherwise be needed for CMOS design. Another significant advantage of McCMOS is the ability to reduce leakage during both active and idle periods of circuit operation.

3 Summary

We propose McCMOS, a technique to control leakage by means of multiple transistor channel lengths. Our preliminary results show that this technique offers leakage savings comparable to other more costly techniques; without requirement for process changes or bias control circuitry. Furthermore, McCMOS makes it convenient to control leakage even when a circuit is active. It is expected that the benefits of this technique will only increase as minimum feature sizes continue to shrink.

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