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Independently addressable fields of porous anodic alumina embedded in SiO_2 on Si

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Fields of thin-film porous anodic alumina (PAA) are fabricated within a SiO_2 support and on independently addressable underlying metal pads. The underlying metallization provides a means for unique postprocessing to be performed on the PAA fields. Customized postprocessing is demonstrated with the synthesis of single-walled carbon nanotubes (SWCNTs) from an embedded catalyst in the PAA, followed by selective decoration of the SWCNTs from different PAA fields with dissimilar nanoparticles. Achieving uniquely functionalized fields of PAA on a single chip provides a scalable integration platform to be used in multiplexed chemical and biological sensing or nanoelectronic devices. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2831002]

More than half a century has passed since detailed reports were published on the anodization of Al foils to form porous anodic alumina (PAA) templates.[1] Research on the potential applications of these templates of vertical nanosized pores has accelerated recently with the increasing interest in nanoscale sensors and devices. PAA is commonly used as a template for nanowire or nanotube synthesis,[2–4] with pore (and thus nanowire) diameters from less than 10 nm to several hundreds of nanometers[5] in a naturally occurring hexagonal arrangement.[6] Nanowires synthesized within PAA are rarely functionalized *in situ*, but are released from the PAA onto a different substrate in postprocessing steps.[7] The need to release the nanowires is largely caused by the difficulty of supporting PAA thin-films on common substrates such as Si.

Most techniques that have been reported for patterning thin-film PAA on a substrate have involved protecting portions of an Al film with a patterned dielectric layer, which shields the Al from the acidic electrolyte during the electrochemical anodization process.[8,9] However, the electrolyte can often penetrate the dielectric barrier, causing the Al to begin anodizing;[9] occasionally, the pores can even protrude beneath the barrier, anodizing the Al laterally. Recently, Park *et al.*[10] developed a technique for patterning PAA within SiO_2 trenches; however, the process still requires a blanket surface metallization that leaves all PAA regions interconnected.[10] This and other similar techniques also encounter technical challenges related to incomplete PAA formation near the pattern boundaries, or even buckling due to compressive stresses between the PAA and SiO_2 sidewall.[10,11]

Herein, we describe a process for fabricating fields of PAA that can be independently functionalized within a SiO_2 support. Metal pads beneath the SiO_2, which can be isolated following anodization, provide access to a prescribed set of the PAA fields, allowing each set of fields to be uniquely functionalized (e.g., with electrodeposited nanowires of different materials[2,3,7]). Single-walled carbon nanotubes (SWCNTs) are synthesized from an embedded catalyst in the PAA,[4] and Pd is electrodeposited to decorate the SWCNTs with nanoparticles.[12,13] We demonstrate customized postprocessing by further coating the Pd nanoparticles on one section of PAA fields with Au; Pd and Au are chosen for demonstration due to their disparate sensitivities in sensing applications.[14,15] In this way, a chip is created with one section of PAA containing Pd nanoparticles on SWCNTs and a separate and independently addressable section of PAA containing Au-coated Pd nanoparticles on SWCNTs. Combining this process for embedding PAA fields in SiO_2 with the recently reported technique for obtaining thin-film PAA with ordered pores[16] is expected to enable the creation of practical structures for nanoelectronic applications that require addressable arrays of templated nanomaterials for interconnects or devices.

The procedure for fabricating electrically isolated fields of PAA is illustrated in Fig. 1. A large common electrode (with smaller branches that eventually serve as independent electrodes) is created by electron-beam evaporation of Ti (80 nm) and Pt (20 nm) onto a thermally oxidized Si substrate that is prepatterned lithographically. After lift-off, 500 nm of SiO_2 is deposited on the entire chip using plasma-enhanced chemical vapor deposition (PECVD). Following SiO_2 deposition, the common electrode and a portion of the electrode branches are lithographically exposed, and the SiO_2 is etched using 6:1 buffered oxide etch (BOE).

At this point, a final lithography step defines the fields (in this case, squares) along the branch electrodes that remain covered by the PECVD SiO_2. The SiO_2 is dry etched in a reactive ion etcher using CF_4 as the active etching gas. The reactive ion etch (RIE) process provides highly anisotropic

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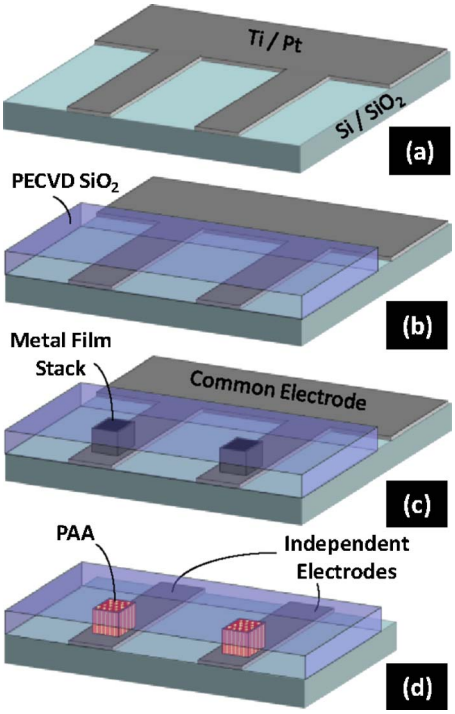

FIG. 1. (Color online) Schematics illustrating the fabrication of electrically isolated PAA fields embedded in SiO_2. (a) Lithographic patterning of Ti/Pt electrodes on SiO_2. (b) PECVD of SiO_2 followed by a patterned wet etch. (c) Lithographic definition of square fields on electrodes, dry and wet etching of SiO_2, deposition and lift-off of Ti/Al/Fe/Al film stack. (d) Anodization of the Al film stacks and subsequent cleaving of the common electrode.

removal of the SiO_2, and is followed by a brief ($\approx$30 s) wet etch in BOE. The BOE etch serves the purposes of removing remaining contaminants from the RIE and of undercutting the photoresist to minimize the effects of expansion in the Al film as it anodizes to form PAA.[10] Using the same patterned photoresist, a metal film stack of 50 nm Ti, 100 nm Al, 1.2 nm Fe, and 300 nm Al is thermally evaporated and subsequently lifted-off.

By briefly wet etching the PECVD-deposited SiO_2 prior to depositing the Al film stack, the adverse effects of volume expansion of the film during formation of the PAA are significantly reduced. The BOE, being an isotropic etchant, undercuts the photoresist to provide space for the film to expand during anodization. The field-emission scanning electron microscope (FESEM) image in Fig. 2(a) shows the boundary of the PAA and SiO_2 from a 30 s BOE etch, resulting in a gap of ~60 nm (the gap typically ranges between 50 and 100 nm). Adjusting the duration of the BOE etch controls the resulting gap between the PAA and SiO_2. Also, the elimination of compressive stress at the SiO_2/PAA interface allows the resulting PAA to be planar, without a central thickening of the PAA field, as observed in related prior work.[9–11]

An advantage of using Ti/Pt electrodes buried beneath 500 nm of SiO_2 is that the Pt surface is visible in both optical and electron microscopies, enabling alignment to the electrodes when defining patterns within which the PAA is formed. Figure 2(b) shows a FESEM image of one such PAA field that has been formed on top of an independent electrode. Square fields of various sizes were created on each electrode, ranging from 5×5 to 100×100 μm^2. All fields were anodized to form PAA by biasing the common electrode with 40 V versus a Pt gauze auxiliary electrode in

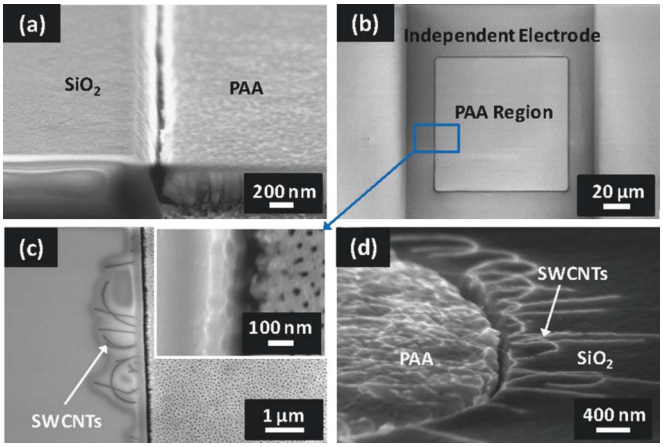

FIG. 2. (Color online) (a) Tilted cross-sectional FESEM image of a PAA field embedded in SiO_2 showing the PAA/SiO_2 boundary. (b) FESEM showing a PAA field on top of an independent electrode; note that SiO_2 covers the entire surface except where the PAA is embedded. (c) Top-view and (d) tilted cross-sectional FESEM images of the PAA/SiO_2 boundary with SWCNTs extending from the PAA onto the SiO_2 surface.

0.3*M* oxalic acid held at a constant temperature of 5 °C. Following anodization, the common electrode is removed from the chip, leaving independent electrodes beneath fields of PAA, as illustrated in Fig. 1(d). Pt was chosen as the surface metal for the electrodes due to its resistance to oxidation, allowing for a low-resistance contact between the electrode and the subsequently deposited Ti/Al/Fe/Al film stack. The quality of the contact between the Pt and the Ti (beneath the PAA) is important when using the PAA fields for processes such as templated nanowire growth because these metal layers provide a back contact to the nanowires.

The thin Fe layer that is sandwiched between the Al films serves as a catalyst for postanodization SWCNT growth.[4] After anodization, the Fe layer becomes exposed on the inner-pore walls, providing a catalytic nucleation point for SWCNTs. SWCNTs are synthesized in all fields using a microwave PECVD reactor with a hydrogen plasma and methane precursor.[4] The high-temperature (900 °C substrate), hydrogen-plasma environment works to decompose the hydrocarbons as well as to penetrate the intrinsic alumina barrier within the PAA, as reported previously.[2] The SWCNTs nucleate within the pores and proceed vertically toward the carbon supply, eventually protruding from the pores and extending along the PAA surface. The FESEM images in Figs. 2(c) and 2(d) show SWCNTs extending across the PAA/SiO_2 interface. Control over the density of the SWCNTs and the effect of the Fe on the PAA have recently been reported.[17]

To demonstrate independent functionalization of the PAA fields, SWCNTs within a given field were decorated selectively with Pd or Au/Pd nanoparticles. Selective plating was performed by contacting the electrodes connected to desired fields and electrodepositing the chosen metal. Pd was electrodeposited in a $PdCl_2$ electrolyte, as reported previously,[13] using two independent electrodes as working electrodes [see Fig. 3(a)]. Pulsed chronopotentiometry at a current density of 2 mA/cm^2 with 250, 0.5 s pulses was used to deposit the Pd, the effects of which have been detailed in previous work.[13] The result is Pd nanowires in contact with the SWCNTs within the PAA and Pd nanoparticles that decorate portions of the SWCNTs on the top PAA surface. Fol-

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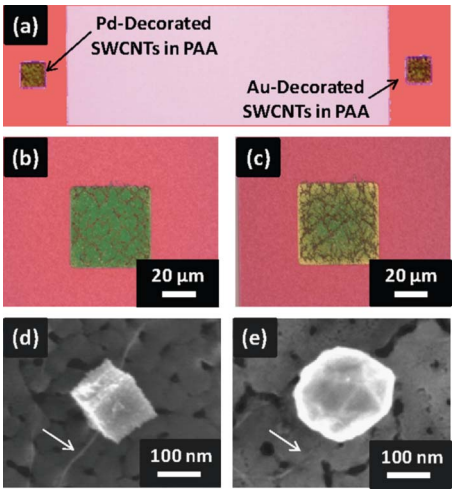

FIG. 3. (Color online) (a) Optical image of a chip showing a PAA field on one independent electrode functionalized with Pd-decorated SWCNTs, while a PAA field on the neighboring electrode has been separately functionalized by coating the Pd nanoparticles with Au. Note that the entire surface (including the electrodes) is covered by SiO_2 except for the PAA fields. (b) and (c) are optical images of a PAA field with Pd nanoparticles on SWCNTs and with Au-coated Pd nanoparticles on SWCNTs, respectively. FESEM images of (d) a Pd nanoparticle decorating a SWCNT and (e) a Au-coated Pd nanoparticle decorating a SWCNT (arrows indicate SWCNT).

lowing the Pd electrodeposition, Au was chronoamperometrically electrodeposited at a potential of 750 mV for 5 s in a chloroauric acid electrolyte to only one of the two fields, forming an overlayer on the Pd nanoparticles [see Figs. 3(c) and 3(e)]. In this way, Pd and Au-coated Pd nanoparticles were synthesized with separate and intrinsic electrical contacts through the SWCNT/nanowire/Ti/Pt electrodes on the same chip.

Figure 3 shows optical and FESEM images of a chip with the PAA fields on one independent electrode having Pd-decorated SWCNTs, while the neighboring electrode region shows Au-coated Pd nanoparticles on SWCNTs. A FESEM image of a Pd nanoparticle (which is typically cubic) (Ref. 13) decorating a SWCNT is shown in Fig. 3(d), while a Au-coated Pd nanoparticle is shown in Fig. 3(e). It is important to note that a single chip could contain a variety of independently addressable nanowires and/or nanoparticles for use as a multifunctional sensor. In the context of multiplexed biological sensing,[18] all PAA fields could initially contain Pd nanoparticle-decorated SWCNTs and, subsequently, undergo unique biofunctionalization.

In this work, fields of PAA were fabricated within a SiO_2 support and on independently addressable underlying metal electrodes. Each independent electrode provides access to a distinct set of PAA fields, enabling unique postprocessing of different fields on the same chip. Performing a brief wet etch on the SiO_2 trenches prior to depositing the Al film stack helps to minimize the adverse effects associated with volume expansion of Al to PAA, which typically causes compressive stresses on the PAA from the SiO_2 trench sidewall. Selective functionalization was demonstrated by synthesizing SWCNTs from all PAA fields on a chip and, subsequently, decorating the SWCNTs on two sets of PAA fields with Pd nanoparticles, and coating the Pd nanoparticles from only one section of fields with Au. The selective decoration of SWCNTs is only one example of how the PAA fields can be uniquely functionalized—the process flow reported herein can be readily altered to provide a user-defined number of independently addressable PAA fields, each with its own unique functionalization (e.g., nanowires of different materials, PAA with different diameter pores, etc). Achieving uniquely functionalized fields of PAA on a single chip provides a scalable platform for a variety of applications, including multiplexed chemical and biological sensing[7,18,19] or nanoelectronic devices.[2,10,12,20]

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