4-1-2008

Optimization of Gate Leakage and NBTI for Plasma-Nitrided Gate Oxides by Numerical and Analytical Models

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***Abstract*—Reduction in static-power dissipation (gate leakage) by using nitrided oxides comes at the expense of enhanced negative-bias temperature instability (NBTI). Therefore, determining the nitrogen content in gate oxides that can simultaneously optimize gate-leakage and NBTI degradation is a problem of significant technological relevance. In this paper, we experimentally and theoretically analyze wide range of gate-leakage and NBTI stress data from a variety of plasma-oxynitride gate dielectric devices to establish an optimization scheme for gate-leakage and NBTI degradation. Calculating electric fields and leakage current both numerically and using simple analytical expressions, we demonstrate a design diagram for arbitrary nitrogen concentration and effective oxide thickness that may be used for process and IC design.**

***Index Terms*—Gate leakage, negative-bias temperature instability (NBTI), optimization, plasma-oxynitride dielectric, quantum–mechanical (QM) effects, reaction–diffusion (R-D) model.**

I. Introduction

OVER THE last few decades, aggressive scaling in transistor dimensions has resulted in dramatic improvement in IC performance [1]. Before the introduction of 130-nm technology node, SiO_2 (with little or no nitrogen) was used as a gate dielectric, and such pure SiO_2 offered excellent interfacial properties with Si substrate [1]–[3]. However, as the dielectric thickness were scaled below 2 nm, higher static-power dissipation (due to increase in gate leakage [1]–[4]) and increased flatband voltage (due to boron penetration from p+ poly-Si to PMOS substrate [2]–[4]) necessitated the use of dielectrics other than pure SiO_2. Different high-κ dielectrics were proposed to replace SiO_2 [2]. Of these, oxynitride dielectrics appeared to be the near-term alternative, offering convenient processing and better reliability as compared to other high-κ counterparts [2]–[4].

Manuscript received June 26, 2007; revised January 4, 2008. This work was supported in part by Applied Materials, by Taiwan Semiconductor Manufacturing Corporation, by Renesas Technologies, and by Semiconductor Research Corporation. The review of this paper was arranged by Editor J. Suehle.

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Digital Object Identifier 10.1109/TED.2008.919545

The advantages of oxynitride gate dielectric (namely, lower gate leakage and resistance to boron penetration), however, is counterbalanced by its poorer reliability characteristics. Of particular concern is the degradation mechanism known as negative-bias temperature instability (NBTI). NBTI occurs mainly in PMOS devices under negative-voltage stress and is enhanced by inclusion of nitrogen in gate dielectrics [4]–[11]. In general, numerous studies have established the importance of the nitrogen spatial profile in dictating the boron penetration and NBTI characteristics [4], [5], [12], [13]. Such studies show that reduction of both NBTI and boron penetration requires a nitrogen profile having (comparatively) lower nitrogen near substrate–dielectric interface (for optimum NBTI) and higher nitrogen near gate–dielectric interface (for reduced boron penetration). Plasma nitridation with decreasing nitrogen concentration from poly-Si/dielectric interface to substrate/dielectric interface, therefore, became an ideal choice [5], [12], [14] for oxynitride gate dielectrics. Adjustment of nitrogen profile within the dielectric of devices having plasma-nitrided oxide (PNO) ensures improved device performance in terms of boron penetration and NBTI, even down to an effective oxide thickness (EOT) of 1.1 nm [12], [13].

Thus, among the three design considerations (gate leakage, boron penetration, and NBTI) for PNO devices, several studies reported the gate leakage versus boron penetration [2]–[4] and boron penetration versus NBTI [4], [5], [12], [13] issues. However, the remaining, and perhaps equally important, optimization of gate leakage and NBTI (the topic of this paper) has never been considered. Indeed, reduction of gate leakage under certain limit necessitates a minimal nitrogen concentration [3], [15]–[18], but whether such nitrogen concentration keeps NBTI within a desired limit (so that device lifetime meets the required criteria) has never been investigated. In this paper (an extension of our previous conference paper [9]), we perform a quantitative analysis of leakage/NBTI tradeoff (as a function of nitrogen concentration) to address the question whether cooptimization of gate leakage/NBTI is possible at any nitrogen concentration. To achieve this objective, we perform the following:

1) measure gate leakage (current density, J_G) and delay-free NBTI over broad range of nitrogen concentration;
2) model gate leakage as a function of oxide thickness and nitrogen concentration by calibrating measurements with detailed numerical simulation [19] and physically based analytical expression;

3) model NBTI degradation within a theoretically consistent framework of reaction–diffusion (R-D) model [9], [20] by taking into account the voltage, temperature, and frequency dependences of NBTI;
4) establish a compact analytical approach for predicting transverse electric field in MOS structures, useful for analyzing NBTI degradation;
5) construct a design diagram for cooptimization of J_G and NBTI for arbitrary nitrogen concentration and EOT combinations.

Based on this study, we conclude that, although there is no optimum nitrogen concentration $(\%N)$ that simultaneously reduces both gate leakage and NBTI, the reduction in J_G at NBTI limited $\%N$ can be significant and would reduce power dissipation without affecting NBTI margin.[1]

II. Experimental Detail

Sample preparation for devices used in this paper are discussed in detail in [13] and [15] and will not be repeated here. Physical thickness $(T_{\rm PHY})$ and $\%N$ for the PNO samples are determined using X-ray Photoelectron Spectroscopy (XPS) [21] with repeatability better than 3% and 2% for $T_{\rm PHY}$ and $\%N$, respectively [15]. For each sample, we measure the gate capacitance (C_G) and J_G at different gate voltage (V_G). This is followed by NBTI-degradation measurement at various stress condition (voltage and temperature) using no-delay on-the-fly $I_{\rm DLIN}$ technique [22], [23]. For a given stress voltage $(V_{G,\rm stress})$ and stress temperature $(T_{\rm stress})$, we estimate the threshold-voltage degradation (ΔV_T) using[2] $\Delta V_T(t) = |I_{\rm DLIN}(t_0) - I_{\rm DLIN}(t)|/|I_{\rm DLIN}(t_0)|^*|V_{G,\rm stress} - V_{T0}|$; where $I_{\rm DLIN}(t)$ is the drain–current measured at time t (at $V_{\rm DS} \sim 50$ mV), V_{T0} is the prestress threshold voltage, and t_0 $(= 1$ ms) is the delay between initiation of stress and the first reading of the drain–current (time-zero delay [25], [26]). As shown in [11] and [26], use of $t_0 \sim 1$ ms introduces negligible error in degradation estimation for the devices under study (having dominant interface-trap generation [11]), provided that the stress time $(t_{\rm stress})$ is greater than ~1 s.

III. Gate Leakage

A. Estimation of Device Model Parameters

Leakage analysis involving MOS structures first necessitates the determination of approximately nine model parameters that characterizes the gate dielectric. These parameters and the measurements (C_G–V_G, J_G–V_G) necessary for extracting them are summarized in Table I. We use quantum–mechanical (QM) analysis (multisubband electron/hole quantization, wavefunction penetration within the dielectric, and polydepletion features are used in this paper) [19] of experimental C_G–V_G and J_G–V_G characteristics to extract these parameters. Excellent agreement between experiment and QM simulation similar to that shown in Fig. 1 is obtained for each sample used in this paper.

TABLE I
Model Parameters Used for Characterizing MOS Structures

Symbol	Definition	Extracted From
EOT	Effective Oxide Thickness	C_G-V_G
V_{FB}	Flat-band voltage	C_G-V_G
ε_{di}	Relative dielectric constant for the dielectric (= $\varepsilon_{SiO2}T_{PHY}/EOT$; where ε_{SiO2} is the relative dielectric constant for SiO_2)	C_G-V_G
N_{sub}, N_{poly}	Substrate and poly-gate doping (assumed uniform)	C_G-V_G
m_{di}	Carrier effective mass within dielectric	J_G-V_G
$E_{g,di}$	Dielectric band-gap	J_G-V_G
ϕ_{be},ϕ_{bh}	Electron and hole barrier height at the substrate-dielectric interface	J_G-V_G

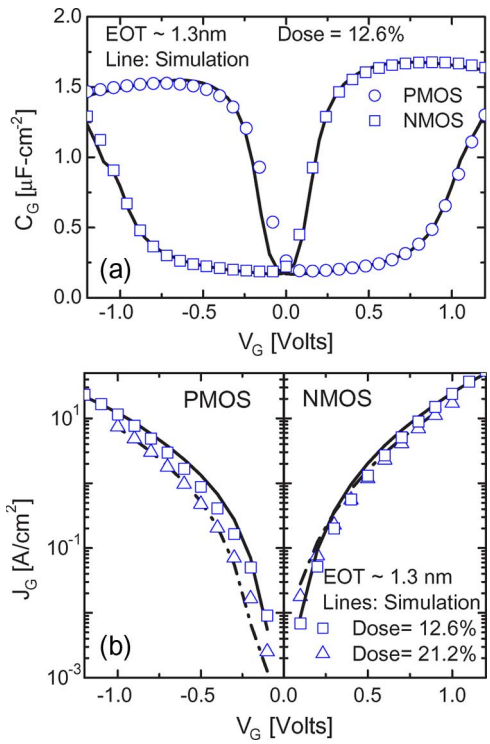

Fig. 1. Experimental (a) C_G–V_G and (b) J_G–V_G curves (in inversion region) for a few SiON devices fitted using QM simulation [19].

B. Variation of Parameters With $\%N$

The procedure of parameter extraction discussed in the previous section can now be repeated to extract the nine model parameters for oxides with various $\%N$. Devices considered in this paper have $T_{\rm PHY}$ of 1.6–1.7 nm, EOT of ~1.3 nm, and $N_{\rm sub}$ of $\sim 3 \times 10^{17}$ cm^{-3}. Nitrogen dose for PNO samples is varied from $\sim 1.25 \times 10^{15}$–$\sim 2.5 \times 10^{15}$ cm^{-2}. For all the

[1]We have ignored boron penetration in this paper, which is shown to be negligible for EOT $\leq$ 1.1 nm [12], [13].

[2]Thus, estimated ΔV_T ignores the necessary mobility and m-factor corrections [24]. Therefore, the reported lifetime, field acceleration, and safe operating condition (see Section IV) should be interpreted as a qualitative illustration for NBTI-leakage optimization.

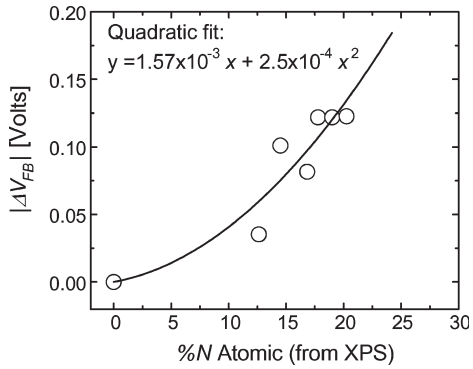

Fig. 2. Variation in $|\Delta V_{\rm FB}|$ for PMOS SiON samples, neglecting the boron-penetration effect.

NMOS samples, $N_{\rm poly}$ is $\sim 8.5 \times 10^{19}$ cm^{-3} and $V_{\rm FB}$ is ~ -1.0 V. For PMOS PNO samples, $N_{\rm poly}$ is $\sim (5.5 \pm 0.5) \times 10^{19}$ cm^{-3} and $V_{\rm FB}$ is $\sim 0.9 \pm 0.1$ V; both $N_{\rm poly}$ and $V_{\rm FB}$ are found to decrease with increasing $\%N$ (consistent with the assessment in [27]). Finally, due to boron-penetration effect in pure SiO_2 samples, higher $V_{\rm FB}$ ($\sim$1.21 V) is estimated. Our analysis shows that the boron-penetration effect also reduces $N_{\rm poly}$ for pure SiO_2 samples to $\sim 10^{19}$ cm^{-3} near polydielectric interface from its bulk value of $\sim 10^{20}$ cm^{-3}. As we are neglecting the boron-penetration effect for simplicity, we can approximate $|V_{\rm FB}|$ for the samples as

$$V_{\rm FB} = \pm \frac{k_B T}{q} \ln \frac{N_{\rm sub} N_{\rm poly}}{n_i^2} + V_{\rm FB(cor)} + \Delta V_{\rm FB}. \quad (1)$$

The first term in (1) represents the standard semiclassical approximation of flatband voltage for poly-Si gate NMOS/PMOS $(-/+)$ structures (where q and n_i are electron charge and intrinsic carrier concentration, respectively), which was previously used in [28]. Second term ($V_{\rm FB(cor)} = -0.04$ and 0.05 V for NMOS and PMOS devices, respectively) indicates the correction needed to match with $V_{\rm FB}$ obtained from QM simulation [19]. Moreover, the last term $\Delta V_{\rm FB}$ takes into account the contribution from interfacial charges at the poly-Si/oxynitride dielectric interface [27]. For NMOS samples, $\Delta V_{\rm FB}$ is $\sim$0.057 V; whereas for PMOS samples, $\Delta V_{\rm FB}$ is negative and $|\Delta V_{\rm FB}|$ increases with $\%N$ (see Fig. 2).

The variation of remaining device parameters $\varepsilon_{\rm di}$, $m_{\rm di}$, $E_{g,\rm di}$, and $\phi_{\rm be}$ are shown in Fig. 3. Here, the parameters for Si_3N_4 (57.1% N_2 dose with $\phi_{\rm be} = 2.1$ eV, $E_{g,\rm di} = 5.1$ eV, $\varepsilon_{\rm di} = 7.6$, and $m_{\rm di} = 0.23 \sim 0.28$) are obtained from [3], [16]–[18]. The error bars indicate the variation in model parameters expected due to $\pm$0.5 Å error in $T_{\rm PHY}$ measurement by XPS. These parameters show an approximately quadratic dependence on $\%N$ ($\varepsilon_{\rm di}$, $m_{\rm di}$, $E_{g,\rm di}$, $\phi_{\rm be} \propto a + b(\%N) + c(\%N)^2$; where the constants a, b, and c for each parameter are shown in Fig. 3). This quadratic trend contradicts with the linear variation typically used in the literature [3], [15]–[18] and requires some discussion. The origin of the "linear approximation" can be traced to the work of Brown *et al.* [29], where they measured $\varepsilon_{\rm di}$ for different oxynitride devices (along with devices having SiO_2 and Si_3N_4 dielectric) and later estimated $\%N$ by assuming linear variation of $\varepsilon_{\rm di}$ from SiO_2 to Si_3N_4. Referring

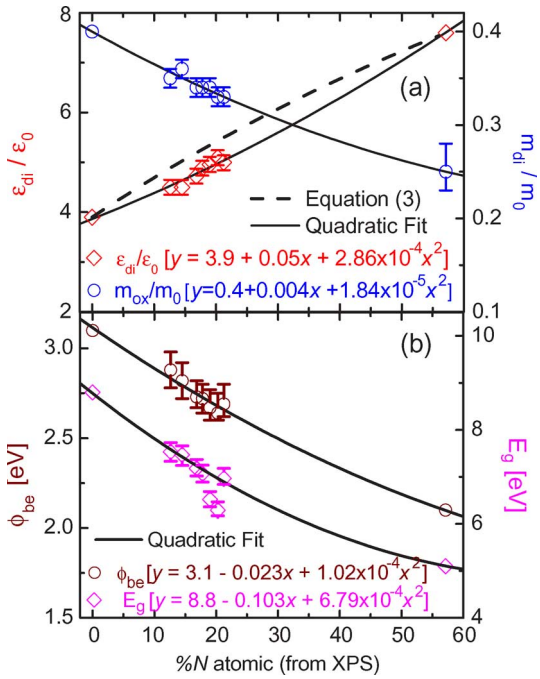

Fig. 3. Quadratic variation of (a) $\varepsilon_{\rm di}$, $m_{\rm di}$, (b) $E_{g,\rm di}$, $\phi_{\rm be}$ with $\%N$ (0% for SiO_2, 57.1% for Si_3N_4) for samples having EOT $\sim$ 1.3 nm. Here, ε_0 is free-space dielectric constant, and m_0 is mass of electron. The error bar shows the variation in model parameters expected due to $\pm$0.5 Å error in measurement of $T_{\rm PHY}$ by XPS. Dashed line in (a) plots the variation of $\varepsilon_{\rm di}$ versus $\%N$, based on (3).

(directly or indirectly) to this work by Brown *et al.*, the authors in [3], [15]–[18] used linear dependence of $\varepsilon_{\rm di}$ and other parameters without any additional proof.

For a physical interpretation of the variation of $\varepsilon_{\rm di}$, $E_{g,\rm di}$, and $\phi_{\rm be}$ with $\%N$, we consider the oxynitride as a uniform pseudobinary alloy, i.e., $SiO_aN_b = (Si_3N_4)_x(SiO_2)_{1-x}$ [30], [31] that satisfies the stoichiometry (i.e., $2a + 3b = 4$) requirement. Thus, percentage atomic concentration (uniform) of [O] and [N] can be expressed as

$$\%N = \frac{4x}{3+4x} \times 100 \quad \%O = \frac{2-3x}{3+4x} \times 100 = \frac{400 - 7(\%N)}{6}. \quad (2)$$

Using (2) and following similar steps as reported in [31], we obtain

$$\varepsilon_{\rm di} = \varepsilon_{SiO_2} \frac{4 - 7n_a}{4 + 2n_a} + \varepsilon_{Si_3N_4} \frac{9n_a}{4 + 2n_a} \quad (3)$$

where $n_a = \%N/100$ is the atomic fraction of [N] within the oxynitride. Dashed line in Fig. 3(a) plots of $\varepsilon_{\rm di}$ versus uniform $\%N$ based on (3). Observed nonlinearity of this plot contradicts the linear variation used in [3], [15]–[18] even for uniformly dosed nitrided dielectric. Now, the plasma-nitrided samples studied in this paper have [N] peak near polygate [13], [15], [21]. The XPS measurement of $\%N$ for these samples, therefore, overestimates $\%N$ in the film [21]. Such overestimation explains the observed discrepancy between the dashed line in Fig. 3(a) (based on (3) for uniformly dosed sample) and our experimental values (fitted solid line in Fig. 3(a) for $\varepsilon_{\rm di}$ versus $\%N$). Similar overestimation of $\%N$, by assuming $\%N$ equals peak [N] value, also gave identical shape for $\varepsilon_{\rm di}$ versus $\%N$

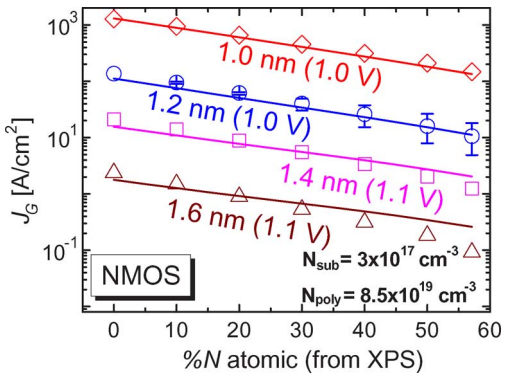

Fig. 4. J_G at V_G versus $\%N$ for NMOS devices at different EOT (symbols: QM simulation; lines: analytical approach). The error bar at EOT $= 1.2$ nm indicates J_G variation expected due to ± 0.5 Å error in $T_{\rm PHY}$, which is negligible up to 30% of N_2 dose.

in [32]. Moreover, as $E_{g,\rm di}$ (hence, $\phi_{\rm be}$) $\propto 1/\varepsilon_{\rm di}$, quadratic relation for $\varepsilon_{\rm di}$ versus $\%N$ [from Fig. 3(a)] also results similar relation for $E_{g,\rm di}$ (hence, $\phi_{\rm be}$) versus $\%N$ [in Fig. 3(b)]. Thus, consideration of oxynitride as a pseudobinary alloy, along with overestimation of $\%N$ for PNO samples using XPS setup, explains the observed "quadratic dependence" of parameters in Fig. 3. If overestimation of $\%N$ were a bit smaller (i.e., for a more uniform profile compared to PNO), one could also have observed an approximately "linear dependence" of parameters with $\%N$. Hence, we identify variation (linear or quadratic) of $\varepsilon_{\rm di}$, $m_{\rm di}$, $E_{g,\rm di}$, and $\phi_{\rm be}$ to be sample-specific, which also depends on the measurement setup being used.

C. Gate-Leakage Variation

Using the explicit dependences of device parameters on $\%N$ (from previous section), we can predict the gate-leakage variation (at a particular V_G) for both NMOS and PMOS devices at different EOT. Assuming that change in EOT does not affect characteristics of the PNO film (i.e., PNO with any N_2 dose has similar properties irrespective of EOT),[3] we have done QM simulation [19] to obtain gate-leakage variation (e.g., Fig. 4 shows J_G at $V_{\rm DD,ITRS}$ [1] for different EOT) as a function of $\%N$ and EOT for NMOS transistors. We also observe that, for similar absolute gate voltage ($|V_G|$), PMOS gate leakage is lower than that of NMOS for N_2 dose less than ~20%–25%, consistent with the findings in [15]. The error bar in Fig. 4 at EOT $= 1.2$ nm indicates J_G variation expected due to ± 0.5 Å error in $T_{\rm PHY}$, which is observed to be negligible up to 30% N_2 dose. Furthermore, Fig. 4 does not indicate a minima in gate leakage as $\%N$ is varied, which is in contradiction to the predictions in [15], [16], and [18]. As stated in [16] and also verified by us, existence of minima is a direct consequence of the value of the device parameters ($\varepsilon_{\rm di}$, $m_{\rm di}$, $E_{g,\rm di}$, and $\phi_{\rm be}$) used for Si_3N_4, hence, should not be considered as a property for oxynitride samples.

[3]This is a very crude assumption and reflects a lack of knowledge of detailed $\%N$ profile within the film. With more information regarding nitrogen profile for all PNO samples (for example, [5]) becomes available, our results can be refined. Therefore, we believe that, due to such assumptions involved in this analysis, our approach should be used as a guideline and not as an absolute reference for design optimization.

In sum, the gate-leakage study performed in this section indicates a well-known reduction in leakage with increase in $\%N$ for devices having similar EOT, with no existence of minima in the variation. To make this gate-leakage study more realistic, one should refine it using appropriate nitrogen-profile information (for example, [5]), thus taking into account the EOT dependence on the parametric variation shown in Fig. 3.

IV. NBTI Degradation

We now consider the second aspect of our optimization problem, namely, the NBTI degradation, which has become an important reliability concern for technology nodes using EOT below 2 nm [7], [10], [20], [33]–[36]. NBTI describes the temperature-accelerated degradation in PMOS devices when it is stressed with negative gate voltage. The origin of NBTI degradation has been discussed extensively since the late 1990s, and for devices with SiO_2 and plasma-oxynitride gate dielectric, the following has been reported.

1) NBTI degradation results mainly from depassivation of Si–H bonds at the Si/dielectric interface (leading $N_{\rm IT}$ generation) and resultant diffusion of hydrogen species into gate dielectric and poly-Si. R-D model is used to interpret such NBTI degradation [9]–[11], [20], [23], [33], [34], [37], [38].
2) At long stress time ($t > 1$ s), interface-trap generation ($\Delta N_{\rm IT}$) is governed by the classical (Arrhenius activated) diffusion of molecular hydrogen (H_2) [9]–[11], [20], [23], [33], [37], [38] and can be estimated as [9], [20], [23], [38]

$$\Delta N_{\rm IT} \sim \left(\frac{k_f N_0}{k_r}\right)^{2/3} (D_{H2}t)^n. \tag{4}$$

In (4), $k_f \sim E_c \exp(\gamma E_{\rm ox}) \exp(-E_F/k_B T_{\rm stress})$ is Si–H bond breaking rate (governed by hole-assisted field-enhanced dissociation of Si–H [9], [20]), $k_r \sim \exp(-E_R/k_B T_{\rm stress})$ represents Si–H bond annealing rate (due to back-diffusion of hydrogen species toward Si/dielectric interface), N_0 is Si–H bond density available before stress, $D_{H2} \sim \exp(-E_D/k_B T_{\rm stress})$ is diffusion coefficient for H_2, and n is the power-law time exponent for NBTI degradation (having values ~1/6 [9], [10], [20], [23], [37], [38], supported by H_2 diffusion in R-D framework [20], [33], [38]). In NBTI for PMOS at inversion, electric field due to mobile carriers (E_c) can be estimated by excluding the depletion-charge contribution ($E_{\rm dep}$) from total electric field ($E_{\rm ox}$), whereas in NBTI for NMOS at accumulation E_c equals $E_{\rm ox}$. Among other parameters, E_F, E_R, and E_D are the activation energies for field-independent part of k_f, k_r, and D_{H2}, respectively, and field-acceleration factor (γ) is expressed as

$$\gamma = \gamma_T + a/k_B T_{\rm stress} \tag{5}$$

where γ_T is a factor coming from hole-tunneling toward interface traps and a is effective dipole moment [9], [20].

In sum, $\Delta V_T (\sim q\Delta N_{\rm IT}/C_{\rm di})$ can be expressed as

$$\Delta V_T = A^* {\rm EOT}^* (E_c)^{2/3} \exp\left(\frac{2\gamma E_{\rm ox}}{3}\right) \exp\left(\frac{-nE_{\rm D1}}{k_B T_{\rm stress}}\right) t^n \quad (6)$$

where $C_{\rm di}$ is the dielectric capacitance and $nE_{\rm D1} = nE_D + 2/3(E_F - E_R)$. Thus, overall activation energy for ΔV_T can be written as

$$E_A \equiv nE_D + 2/3(E_F - E_R - aE_{\rm ox}) = nE_{\rm D1} - (2/3)aE_{\rm ox}. \quad (7)$$

3) NBTI degradation is independent of frequency for ac NBTI degradation, which is shown both theoretically [39], [40] and experimentally for wide frequency range [41], [42].

In addition, there are other types of devices where hole trapping (detrapping) to (from) preexisting defects also plays significant role in NBTI degradation [11], [25], [43]. These devices, mostly having thick dielectric with high N_2 near interface [11], also show frequency dependence in measured ac NBTI degradation [25], [43]. As we focus our analysis on PNO samples having less N_2 near interface, we ignore such hole trapping/detrapping in our analysis. In principle, the presented optimization scheme can be more generalized for any oxynitride devices by treating hole trapping/detrapping using appropriate models (e.g., [11], [20], [25], [43]).

A. Calculation of Electric Fields

As evident from (6), estimation of electric fields ($E_{\rm ox}$ and E_c) are critical in NBTI-degradation analysis for various EOT and $\%N$. Experimentally, one could integrate measured C_G–V_G from $V_{\rm FB}$ to V_G to determine total charge within the substrate ($Q_{\rm sub}$) and, hence, calculate $E_{\rm ox}(\text{at } V_G) = Q_{\rm sub}/\varepsilon_{\rm SiO_2}$, which equals E_c for NMOS in accumulation; while for PMOS in inversion, E_c could be calculated using $C_G(V_G - V_T)/\varepsilon_{\rm SiO_2}$. However, this direct method is difficult to apply in oxides with EOT less than 2.0 nm that have high gate leakage, where one must either use specialized test structures for measuring C_G–V_G [44] or use a reconstruction algorithm to correct the leakage-contaminated C_G–V_G [45] data. Moreover, high gate leakage for oxynitrides with EOT lower than ~1.2-nm loads the C–V analyzer and makes the C_G measurement more difficult.

For such thin oxides, therefore, an analytical approach is better suited in predicting $E_{\rm ox}$ and E_c for a particular technology node using known values of EOT, $N_{\rm sub}$, $N_{\rm poly}$, and $\%N$. A flowchart for such calculation (for inverted PMOS substrate with negative V_G) is shown in Fig. 5, where valence-band tip at the substrate/dielectric interface is used as energy reference, and charge centroids are determined from the same interface. Our approach is similar to the algorithm proposed in [46]. The results using such fast algorithm is in excellent agreement with more detailed QM C–V simulation [19] (Fig. 6).[4]

[4]Both analytical and QM simulation also predicts negligible change in $E_{\rm ox}$ under change in temperature at a particular V_G. Therefore, electric field calculated at a particular temperature can be used for reliability predictions at any other temperature.

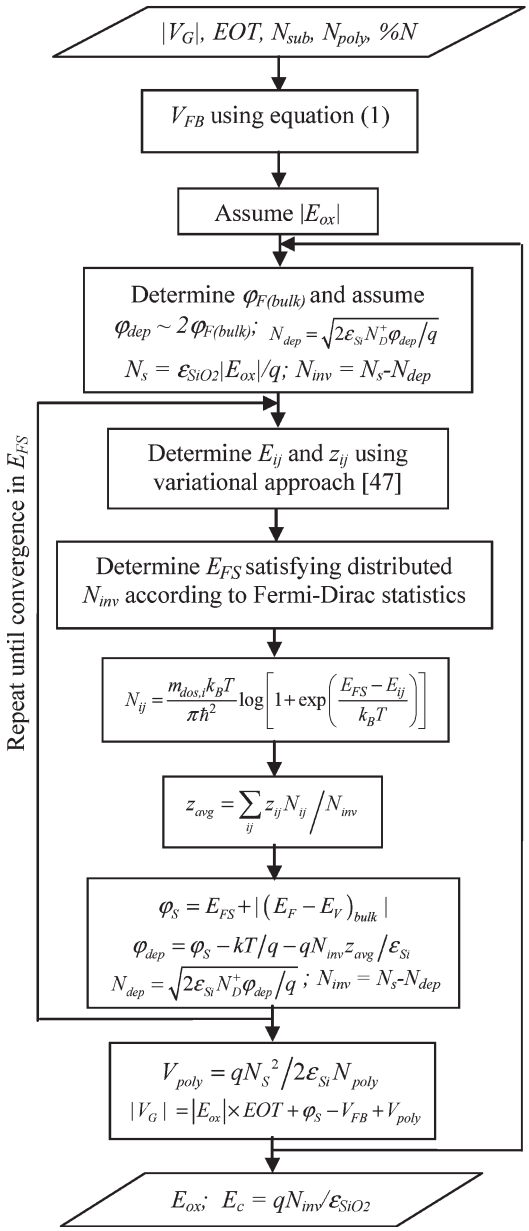

Fig. 5. Flowchart for electric fields calculation (from $|V_G|$) in PMOS inversion. Reverse calculation (electric field to $|V_G|$) is also possible. A similar calculation can also be done for NMOS devices. The notations used here are given as follows (QM notations are discussed extensively in [19], [46], and [47]): $\varepsilon_{\rm Si}$ is the dielectric constant for Si; $\varphi_{F(\rm bulk)}$ is the Fermi-level position in the bulk of the substrate (with respect to the midgap); φ_S is the surface potential; $\varphi_{\rm dep}$ is the depletion charge contribution to φ_S; $|(E_F - E_V)_{\rm bulk}|$ is the difference between the valence band and the Fermi level in the substrate bulk; $V_{\rm poly}$ is the voltage drop in poly-Si; N_D^+, N_s, $N_{\rm inv}$, and $N_{\rm dep}$ are the concentrations of the ionized donor, substrate charge, inversion charge, and depletion charge, respectively; E_{FS} is the substrate Fermi level; E_{ij} is the eigen-energy for the jth subband in the ith valley within the potential well formed near the substrate/dielectric interface (for PMOS device in inversion, only the subbands of the heavy hole valleys are considered); N_{ij} and z_{ij} are the charge concentration and charge centroid in eigen-state E_{ij}; $m_{{\rm dos},i}$ is the density-of-state effective mass for the ith valley; and $z_{\rm avg}$ is the average inversion layer thickness.

B. NBTI Model Parameters

Determination of device information and electric field enables us to use (5)–(7) in estimating NBTI model parameters (A, γ, γ_T, a, $E_{\rm D1}$, n) for pure SiO_2 and PNO samples by

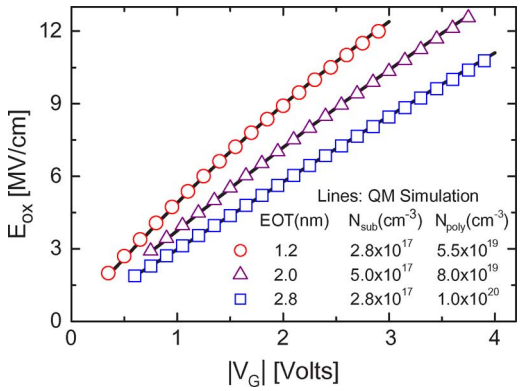

Fig. 6. Electric field versus gate-voltage relation obtained using analytical approach of Fig. 5 (symbols) are in agreement with that obtained from QM simulation (lines).

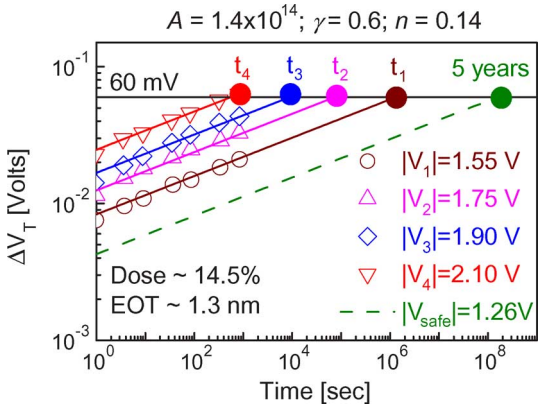

Fig. 7. Voltage-dependent NBTI stress data (taken at 125 °C) fitted using (6) enables one to estimate A, γ, and n for a device ($E_{\rm D1} \sim 0.9$ eV assumed, see Section IV-C). Lifetimes (t_1, t_2, t_3, t_4) at different stress voltages (V_1, V_2, V_3, V_4) and safe operating voltage ($V_{\rm safe}$) can also be determined, as discussed in Section IV-D.

fitting ΔV_T measured at various $V_{G,\rm stress}$, $T_{\rm stress}$. For example, using (6) one can use voltage-dependent stress data (at fixed $T_{\rm stress}$) to obtain A, γ, n (Fig. 7), or temperature-dependent stress data (at fixed $V_{G,\rm stress}$) to obtain n, E_A at $V_{G,\rm stress}$ [23], [34] [therefore, $E_{\rm D1}$ using (7)]. Determination of the remaining two parameters (γ_T, a) are done by analyzing both voltage- and temperature-dependent data and using either (5) and/or (7) [9], [20]. An estimation of γ at different $T_{\rm stress}$ and a plot of γ versus $1/k_B T_{\rm stress}$ [Fig. 8(a)] gives γ_T as intercept at $T_{\rm stress} \rightarrow \infty$ and a as slope [see (5)]. Alternately, determining E_A at different electric field [Fig. 8(b)][5] and using (7) enables the estimation of a. Later, using previously obtained γ and (5), γ_T can be estimated.

C. Variation in NBTI Model Parameters With %N

Among four independent NBTI parameters (A, γ, n, and $E_{\rm D1}$), $n \sim 0.14$ is found to be constant (independent of $\%N$) for the devices studied. The parameters A and γ, however, show

[5]Although negligible variation of E_A versus $\%N$ in Fig. 8(b) (at 1.9 V) contradicts with the E_A versus $\%N$ variation reported in [8] and [36], we identify this as a signature of negligible hole trapping in the PNO samples studied here, which have lower N_2 concentration near substrate interface [11], [20] as compared to the samples in [8] and [36].

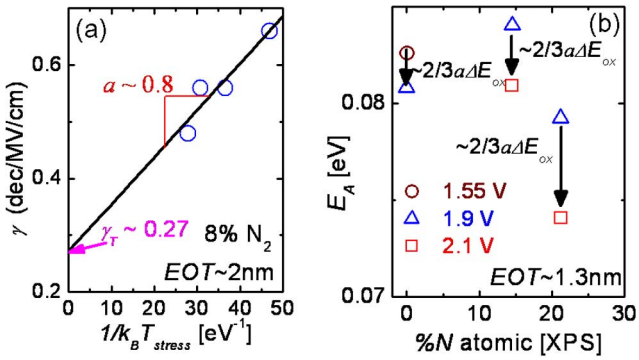

Fig. 8. Estimation of γ_T, a using voltage- and temperature-dependent stress data. (a) Plot of γ versus $1/k_B T_{\rm stress}$ directly estimates γ_T as intercept at $T_{\rm stress} \rightarrow \infty$, and a as slope. (b) Determining E_A at different electric field enables estimation of a, hence, γ_T using (5).

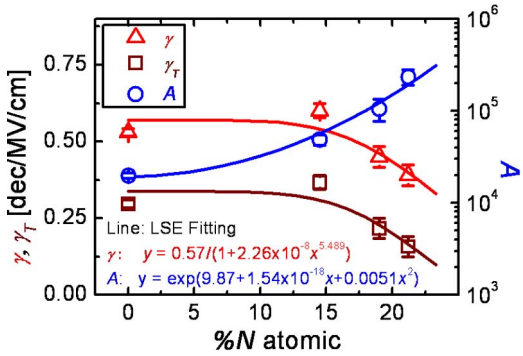

Fig. 9. Variation of NBTI model parameters (A, γ, and γ_T) with $\%N$ ($a \sim 0.8$ qÅ used). The error margins in calculations are negligible. The fitted variation will be technology-specific.

systematic variation with $\%N$ (Fig. 9). The source of variation in γ can be traced to variation in a and γ_T [see (5)]. We find that the variation of a with $\%N$ is small (within the error margin of both methods of estimations in Fig. 8). Therefore, we use $a = 0.8$ qÅ [Fig. 8(a)] for all devices, and we estimate γ_T using (5) for different $\%N$ (Fig. 9); in other words, the $\%N$ dependence of γ is actually reflected in the $\%N$ dependence of γ_T. Finally, we use $E_{\rm D1} \sim 0.9$ eV, which is calculated [see (7)] using average value of E_A ($= 0.08$ eV) for devices tested at $E_{\rm ox} = 7 \sim 10$ MV/cm and 27 °C–125 °C, which is considered as E_A for all PNO samples at an average $E_{\rm ox}$ of 8.5 MV/cm. Note that constancy of n with $\%N$ reflects dominance of interface-trap generation and diffusion of hydrogen species within poly-Si [37] as the main cause of NBTI degradation for such devices. But, constancy $E_{\rm D1}$ with $\%N$ does not reflect any fundamental requirement, except that any variation is possibly embedded within the error-margin of the data. Thus, NBTI degradation with $\%N$ variation is attributed to the following two factors: A and γ_T.

D. Safe Operating Condition

The variation of NBTI performance for different oxynitride devices is monitored by safe operating $V_G(V_{\rm safe})$, which is defined as $V_{G,\rm stress}$ at which device can operate up to its lifetime ($t_{\rm life}$) without crossing a certain failure criteria ($\Delta V_{T(\rm max)}$), for example, 60 mV of ΔV_T (Fig. 7 shows the determination of $V_{\rm safe}$ and $t_{\rm life}$ for one sample). The parameters

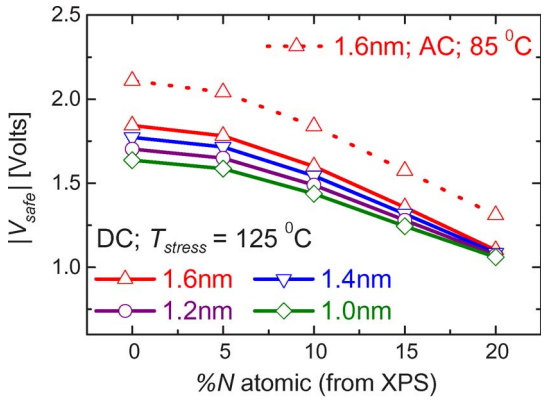

Fig. 10. $V_{\rm safe}$ versus $\%N$ at different EOT($T = 125$ °C; failure criteria: $\Delta V_T = 60$ mV, $t_{\rm life} = 5$ years for CMOS dc operation). Dotted line for EOT = 1.6 nm indicates the improvement in ac condition and with $T_{\rm stress} = 85$ °C.

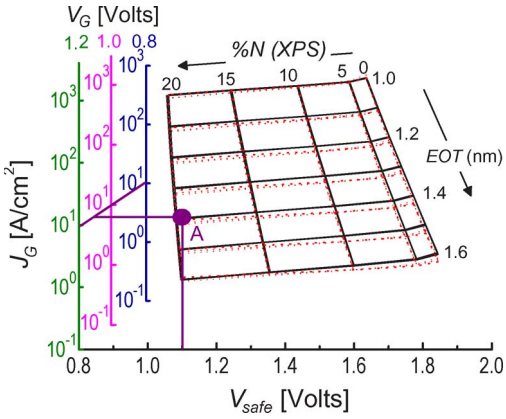

Fig. 11. Design diagram for SiON devices, obtained using Fig. 4 (J_G at $V_G = 0.8$, 1.0, and 1.2 V are considered) and Fig. 10. Solid black lines use J_G calculated by QM simulation and dotted red lines use J_G calculated from (8)–(11). Note the universality (i.e., curves at different V_G falling on top of each other) of the figure when J_G calculated by QM simulation. Operating point A ($V_{\rm safe} = 1.1$ V and $J_G = 10$ A/cm^2) suggests, for example, the use of EOT $\sim$ 1.4 nm and $\sim$20% N_2 dose.

$A(N)$, $\gamma_T(N)$ (derived by fitting the NBTI data), $V_{\rm FB}(N)$ (obtained from C–V analysis), and other (approximately constant) PMOS parameters ($N_{\rm poly} \sim 6 \times 10^{19}$ cm^{-3}, $N_{\rm sub} \sim 3 \times 10^{17}$ cm^{-3}, $a \sim 0.8$ qÅ, and $E_{\rm D1} \sim 0.9$ eV) are used to calculate $V_{\rm safe}(N, {\rm EOT})$ for any combinations of $\%N$ and EOT (Fig. 10)[6] by means of (5)–(7). Here, we use the analytical approach presented in Fig. 5 for calculating electric fields. NBTI performance for dc operation is calculated for failure criteria of $\Delta V_{T({\rm max})} = 60$ mV, $t_{\rm life} = 5$ years (equivalent to $t_{\rm life} = 10$ years in CMOS operation, assuming 50% activity of PMOS transistors). Use of NBTI-aware circuit design [48] will also help in further reduction in required lifetime. A lifetime improvement of $2^{1/2n}$ times (based on R-D model simulation for ac degradation having 50% duty cycle) is used for illustrating ac effects in NBTI degradation, although there are reports for $2^{1/n}$ times improvement (corresponding to ac NBTI degradation being $\sim$50% of dc degradation [41], [42]). Thus, we predict an improvement in $V_{\rm safe}(N, {\rm EOT})$ with inclusion of ac effects and also with reduction in temperature.

V. Optimization of Gate Leakage and NBTI

So far, we have discussed the variation of gate-leakage (obtained using QM simulation, see Fig. 4) and NBTI degradation (resultant change in $V_{\rm safe}$, Fig. 10; which uses results from Figs. 2, 5, and 9) for plasma-oxynitride devices with $\%N$ and EOT. Merging the plots of $J_G(N, {\rm EOT})$ at different V_G and $V_{\rm safe}(N, {\rm EOT})$, we obtain a design diagram for plasma-oxynitride technology having low $\%N$. Fig. 11 shows the design diagram that can be used for $V_{\rm safe} = V_G = 0.8 \sim 1.2$ V.[7] Note that the curves obtained at different V_G fall on top of each other (solid black lines in Fig. 11). This makes Fig. 11 applicable for optimization in the range of $V_{\rm safe} = 0.8$–1.2 V. The range of $V_{\rm safe}$ can be easily extended by considering $J_G(N, {\rm EOT})$ at more V_G in the design diagram (hence, adding more y-axis with appropriate current scales). Moreover, change in operating temperature and inclusion of ac effects (thus, changing $V_{\rm safe}$) can shift the diagram along x-axis (as gate leakage has negligible change with temperature). Resultant design diagram can then be used to calculate any pair of the variables ($V_{\rm safe}$, J_G, $\%N$, and EOT) when the other pair is given. For example, if an IC design requires $V_{\rm operating} = 1.1$ V and $J_G = 10$ A/cm^2, one needs to draw a vertical line from x-axis at 1.1 V and a horizontal line from y-axis at 1.1 V and 10 A/cm^2. The two lines intersect at point A (see Fig. 11). Thus, design diagram suggests the use of EOT $\sim$ 1.4 nm and $\%N \cong 20\%$.

If the optimization anticipated by the conservative design diagram is unacceptable, the optimization at higher $\%N$ and lower EOT will be possible by reconstructing a new diagram with reduced operating temperature, including ac effects, and increasing the leakage constraint. Finally, since PMOS leakage exceeds NMOS leakage for N_2 dose exceeding 20%–25% (see Section III-C), one should consider PMOS leakage/PMOS NBTI rather than the NMOS leakage/PMOS NBTI (discussed in this paper) for optimization above 20%–25% N_2 dose.

VI. Conclusion

We have analyzed an extensive set of leakage and degradation data to construct a cooptimization scheme of J_G and NBTI for arbitrary $\%N$ and EOT combinations. In such process, we highlight the importance of gate leakage versus NBTI study for PNO devices, which has not been considered so far in literature. A design diagram is proposed based on such cooptimization, which enables one to establish the dc (ac)-NBTI limited upper limit of $\%N$ for core CMOS technologies. Using the procedure described as a guideline and incorporating detailed nitrogen-profile information, with effect of boron penetration, should enable one to reliably (up to a

[6]Although Fig. 10 suggests similar $V_{\rm safe}$ for different EOT at N_2 dose $\sim$20%, it should not be taken as absolute number. As PNO samples have nitrogen profile with $[N]$ peaking near poly [14], [21], devices having same $\%N$ (measured by XPS [21]), but higher EOT, will comparatively have lower $[N]$ near substrate interface—hence, less NBTI degradation [11], [20]. Thus, $V_{\rm safe}$ for higher EOT devices is expected to be higher than the values shown in Fig. 10. Such correction again requires one to have accurate knowledge of N_2 profile within the PNO film. Once such information is available, the optimization process can be readily updated.

[7]An analytical construction of design diagram is discussed in the Appendix.

desired NBTI lifetime) operate the device with optimum static-power dissipation. We anticipate that such analysis would have broad impact for optimization of $\%N$ content in sub-2-nm gate dielectrics.

APPENDIX
ANALYTICAL CONSTRUCTION OF DESIGN DIAGRAM

In the main body of this paper, we have provided a physically rigorous procedure to optimize gate current and NBTI degradation based on a set of comprehensive measurements. However, the simulation tools we used may not be readily available to many research groups. Therefore, we develop analytical expressions for calculating electric fields, leakage current, and safe operating voltage (which is an indicator of NBTI degradation), which would enable one to rapidly construct the design diagram in Fig. 11 with reasonably good accuracy.

A. Model for Electric Fields

Noting the universal quadratic relationship between $E_{\rm ox}$ and $|V_G|$ in Fig. 6 irrespective of the values for EOT, $N_{\rm sub}$, $N_{\rm poly}$, and $\%N$ (for larger EOT samples, quadratic behavior appears at larger $|V_G|$ as compared to smaller EOT samples), we can estimate $E_{\rm ox}$ using

$$E_{\rm ox} = P_1|V_{G,\rm eff}|^2 + P_2|V_{G,\rm eff}| + P_3 \tag{8}$$

where $|V_{G,\rm eff}| = |V_G| - |\Delta V_{\rm FB}|$ and the coefficients are given by (9a) and (9b) for NMOS and PMOS devices, respectively, i.e.,

$$\begin{aligned}
P_1 =& (-0.97 + 0.7\text{EOT} - 0.15\text{EOT}^2)\\
&\times \left(1 + 0.014N_{\rm poly} - 3.22\times10^{-3}N_{\rm poly}^2\right)\\
&\times \left(1 - 1.77\times10^{-3}N_{\rm sub} - 5.08\times10^{-4}N_{\rm sub}^2\right)\\
P_2 =& (8.56 - 3.66\text{EOT} + 0.62\text{EOT}^2)\\
&\times \left(0.67 + 0.084N_{\rm poly} - 3.78\times10^{-3}N_{\rm poly}^2\right)\\
&\times \left(1 - 6.73\times10^{-4}N_{\rm sub} - 1.51\times10^{-4}N_{\rm sub}^2\right)\\
P_3 =& (0.93 - 0.87\text{EOT} + 0.24\text{EOT}^2)\\
&\times \left(1.98 - 0.27N_{\rm poly} + 0.016N_{\rm poly}^2\right)\\
&\times \left(0.94 + 0.01N_{\rm sub} - 2.7\times10^{-3}N_{\rm sub}^2\right)
\end{aligned} \tag{9a}$$

$$\begin{aligned}
P_1 =& (-0.93 + 0.68\text{EOT} - 0.15\text{EOT}^2)\\
&\times \left(1.06 + 0.013N_{\rm poly} - 2.7\times10^{-3}N_{\rm poly}^2\right)\\
&\times \left(1 + 2.6\times10^{-3}N_{\rm sub} - 4.43\times10^{-4}N_{\rm sub}^2\right)\\
P_2 =& (8.4 - 3.65\text{EOT} + 0.644\text{EOT}^2)\\
&\times \left(0.69 + 0.08N_{\rm poly} - 3.64\times10^{-3}N_{\rm poly}^2\right)\\
&\times \left(1 - 6.5\times10^{-4}N_{\rm sub} - 1.47\times10^{-4}N_{\rm sub}^2\right)\\
P_3 =& (0.78 - 0.73\text{EOT} + 0.2\text{EOT}^2)\\
&\times \left(2 - 0.29N_{\rm poly} + 0.018N_{\rm poly}^2\right)\\
&\times \left(0.9 + 0.027N_{\rm sub} - 2.33\times10^{-3}N_{\rm sub}^2\right)
\end{aligned} \tag{9b}$$

EOT, $N_{\rm sub}$, and $N_{\rm poly}$ in (9) needs to be expressed in units of nanometer, 10^{17} cm^{-3}, and 10^{19} cm^{-3}, respectively. After calculating $E_{\rm ox}$ using (8), $E_c = E_{\rm ox} - E_{\rm dep} = E_{\rm ox} - \sqrt{2q\varepsilon_{\rm Si}N_D^+\varphi_{\rm dep}}/\varepsilon_{\rm SiO_2}$ can be calculated by using $\varphi_{\rm dep} \sim 2\varphi_{F(\rm bulk)} + 6kT/q$ [49]. Such estimations of $E_{\rm ox}$ and E_c are in excellent agreement (not shown) with the results from both QM simulation and analytical formalism of Section IV-A.

B. Model for Gate-Leakage Current

Next, we develop a physically based analytical approach to estimate NMOS gate-leakage variation in inversion by using $J_G \sim N_{\rm inv} f \overline{T}$ [50]. We use $N_{\rm inv} \sim E_{\rm ox}$ (considering $N_{\rm dep} \ll N_{\rm inv}$), electron-impact frequency (f) proportional to $E_{\rm ox}^{0.6}$ [50], and estimate mean tunneling probability $\overline{T} \sim \exp(2\alpha T_{\rm PHY})$ by replacing the triangular energy barrier for electron tunneling using an effective square barrier of height $\varphi_{\rm be} - E_{\rm ox}T_{\rm PHY}/2$ [15]; hence, $\alpha \equiv \sqrt{2m_{\rm ox}q(\phi_{\rm be} - E_{\rm ox}T_{\rm PHY}/2)}/\hbar$. Based on these, we fit J_G versus $E_{\rm ox}$ (calculated by QM simulation) using

$$J_G = AE_{\rm ox}^{1.6}\exp\left(-B\sqrt{1 - CE_{\rm ox}}\right). \tag{10}$$

Fitting of J_G versus $E_{\rm ox}$ at different $T_{\rm PHY}$, $\varphi_{\rm be}$, and $m_{\rm ox}$ enables us to determine the coefficients A, B, and C such that

$$A = 2\times10^9 \tag{11a}$$

$$\begin{aligned}
B =& \left(2.73 + 17.8T_{\rm PHY} - 2.13T_{\rm PHY}^2\right)\\
&\times (0.72 + 0.7m_{\rm ox})(0.6 + 0.13\phi_{\rm be})
\end{aligned} \tag{11b}$$

$$\begin{aligned}
C =& \left(-3.56\times10^{-3} + 3.71\times10^{-2}T_{\rm PHY} - 7.1\times10^{-3}T_{\rm PHY}^2\right)\\
&\times (1.82 - 0.266\phi_{\rm be}).
\end{aligned} \tag{11c}$$

Thus, we observe an increase of B with increase in $T_{\rm PHY}$, $\varphi_{\rm be}$, and $m_{\rm ox}$, and an increase of C with increase in $T_{\rm PHY}$ and/or decrease in $\varphi_{\rm be}$; which is consistent with the semiclassical intuition presented earlier. Using the quadratic dependence of $\varepsilon_{\rm di}$, $\varphi_{\rm be}$, and $m_{\rm ox}$ from Fig. 3 and $E_{\rm ox}$ calculated using (8), we obtain leakage-current variation with $\%N$ using (10) and (11). The obtained variation is remarkably consistent with QM simulation results (Fig. 4).

C. Calculation of $V_{\rm safe}$

Next, we calculate $V_{\rm safe}$ by first determining safe operating electric field $(E_{\rm safe})$ for specific $\%N$ and EOT. This is easily done by inverting (6), such that[8]

$$\begin{aligned}
E_{\rm safe} = \frac{3}{2\gamma}\ln\Bigg[\Delta V_{T(\max)}\Big/\Big\{& A^*\text{EOT}^*\exp(-0.126/k_BT_{\rm stress})\\
&\times(E_{\rm safe} - E_{\rm dep})^{2/3}t_{\rm life}^{0.14}\Big\}\Bigg]
\end{aligned} \tag{12}$$

where (as used in Fig. 11) $\Delta V_{T(\max)} = 60$ mV, $t_{\rm life} = 5$ years, $E_{\rm D1} = 0.9$ eV, $n = 0.14$, $E_{\rm dep} = \sqrt{2q\varepsilon_{\rm Si}N_D^+\varphi_{\rm dep}}/\varepsilon_{\rm SiO_2}$, and

[8]Equation (12) can be solved iteratively by various methods. A simple MATLAB code useful for this purpose is given by $E_{\rm safecal}$ = inline(['($E_{\rm safe} - 3/(2/\gamma)$* log($\Delta V_{T\max}$/($A$*EOT* exp($-n$*$ED1/kT$)* ($E_{\rm safe}-E_{\rm dep}$)^(2/3)*$t_{\rm life}^{\wedge}n$)))'], '$E_{\rm safe}$', '$\gamma$', '$\Delta V_{T\max}$', '$A$', 'EOT', '$n$', '$ED1$', '$kT$', '$E_{\rm dep}$', '$t_{\rm life}$'); $E_{\rm safe} = f_{\rm zero}(E_{\rm scal}, [0, 10], \text{options}, \gamma, \Delta V_{T\max}, A, \text{EOT}, n, ED1, kT, E_{\rm dep}, t_{\rm life})$.

$\varphi_{\rm dep} \sim 2\varphi_{F(\rm bulk)} + 6kT/q$ [49], and A, $\gamma(\gamma_T)$ variation are obtained from Fig. 9. $V_{\rm safe}$ is later calculated using (8).

Thus, we recalculate the design diagram (dotted red lines in Fig. 11) using analytical expressions in (8)–(12) and compare it with the procedure presented this paper. Both approaches agree with each other reasonably well (although curves at different V_G do not fall on top of each other, due to the approximations involved in the obtained analytical expressions), motivating the use of these simple equations over sophisticated QM simulation in constructing the design diagram.

ACKNOWLEDGMENT

The authors would like to thank Network for Computational Nanotechnology for computational resources. The author Ahmad E. Islam would also like to thank H. Kufluoglu, Md. S. Hasan, and D. Varghese of Purdue University for useful discussions.

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