January 2008

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Rabieirad, Laleh and Mohammadi, Saeed, "A reconfigurable MEMS-less CMOS tuner for software defined radio" (2008). *Department of Electrical and Computer Engineering Faculty Publications.* Paper 66.
http://dx.doi.org/http://dx.doi.org/10.1109/MWSYM.2008.4632948

A Reconfigurable MEMS-less CMOS Tuner for Software Defined Radio

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ABSTRACT — **Design, simulation and measurement of a reconfigurable CMOS RF tuner that can be utilized in the RF front-end of a software defined radio are presented. 0.13µm high Q CMOS varactors controlled by a 22bit shift register are placed periodically on a low loss Coplanar Waveguide (CPW) transmission line to form a 4-11GHz reconfigurable tuner. The monolithic tuner does not use any MEMS devices to achieve the reconfigurability.**

Index Terms — **Programmable RF circuit, reconfigurable architecture, shift register, tuner, varactor.**

I. Introduction

Programmable RF transceiver architectures used in software defined radios can adapt to various modulation schemes, modes of operation and frequency bands. To implement such architectures, reconfigurable matching networks or tuners are essential. A reconfigurable tuner placed at the input of a low noise amplifier improves the noise figure, gain and linearity as the operating frequency is varied. As the output programmable tuner of a power amplifier, reconfigurable tuners can improve the power gain, efficiency and linearity as the frequency band, modulation scheme or power level is varied [1-3]. Implementing reconfigurable matching networks based on microelectromechanical systems (MEMS) has been previously reported [4-6]. Although MEMS devices provide low loss and high quality factors, they cannot be easily integrated with a standard CMOS or BiCMOS process. CMOS switched capacitors have been used in [7] to realize a reconfigurable matching network operating at frequencies below 1GHz. In this paper, for the first time, a fully integrated CMOS programmable tuner that operates from 4 to 11GHz is demonstrated. The proposed device is implemented in a standard 0.13µm CMOS process with a small chip area and can be programmed to 2^{22} different impedance values without using any MEMS devices.

II. Tuner Structure

To implement the programmable tuner N=44 varactor pairs with distance of s=32µm from each other are used across a 1.5mm long low loss transmission line (Fig.1). Every two varactor pairs that are facing each other are biased using the same bias line. Symmetrical design of the structure enhances the coplanar wave propagation mode. By using a 22-bit serial in/parallel out shift register integrated along the tuner, we can achieve 2^{22} possible impedance matching points. Each bit of the shift register controls the bias line of two varactors pairs in a binary fashion. The desired combination of bias voltages is fed into the shift register through the serial in and clock inputs to provide field programmability. A 1pF parallel capacitor (C_{bypass}) at the gate terminal of the CMOS varactors ensures separation of the DC bias lines and high degree of tuner reconfigurability while maintaining good RF ground for frequencies above 4GHz. A 10KΩ resistor on each bias line limits the RF coupling and loss through the bias lines. The tuner is fabricated in a 0.13µm CMOS process with 4µm thick top metallization and occupies an area of 0.7mm×1.7mm. The die photo of the chip is shown in Fig.2.

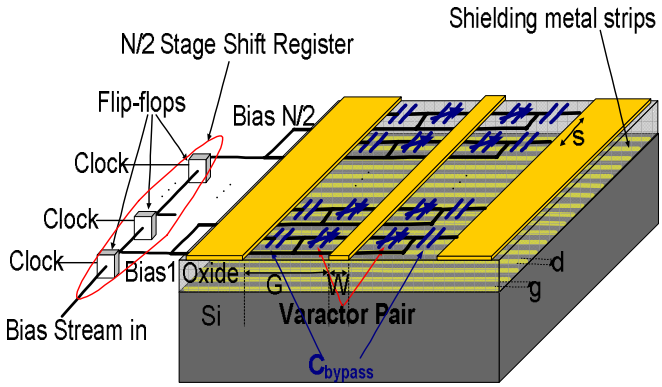

Fig. 1. Structure of the CMOS Tuner (N=44, s=32µm, W=15µm, G=35µm, shielding parameters: d=1µm, g=1µm).

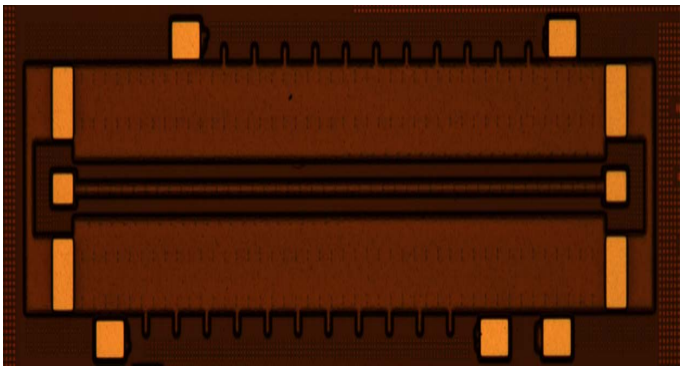

Fig. 2. Die photo of the test chip. Shift register layout is drawn around the CPW line.

III. TUNER DESIGN

The programmable CMOS tuner is formed by periodically placing high performance CMOS varactors across a low loss slow-wave Coplanar Waveguide (CPW) transmission line according to Fig. 1. To achieve a high performance tuner, both the varactors and the CPW line are optimized.

A. Varactor Design

The varactor is formed by connecting the source and drain terminals of an NMOS transistor to the signal line and the gate terminal to the bias line. There is a tradeoff between the quality factor of the varactor and its capacitance ratio C_{max}/C_{min}. Higher capacitance ratio results in more smith chart coverage but lower quality factor. We have optimized the number of fingers (n_f=26) and finger area (W×L= 1µm×240nm) of each varactors to achieve a reasonably high quality factor of 10 at 10GHz and an acceptable maximum to minimum capacitance ratio of 1.5.

B. Transmission Line Design

In addition to optimized varactors, a high performance tuner requires a very low loss transmission line such that a large area of the Smith impedance chart is covered. Standard CPW transmission lines in CMOS technology suffer from significant loss at high frequencies due to dielectric losses of low resistivity Si substrate. Such high losses translate into very small coverage of Smith chart (minimal impedance variation of the tuner). To reduce the loss and thus achieve better Smith chart coverage, an array of floating narrow metal strips is placed under the transmission line as proposed by [8]. These floating metal strips isolate the CPW structure from the Si substrate, effectively removing the dielectric losses associated with the Si substrate from the tuner structure. As a result, a significant reduction in the total loss of the transmission line (loss reduction around 0.5dB/mm at 10GHz) is achieved. This enables us to achieve a high quality factor CPW line and thus a better Smith chart coverage. Floating metal strips lower the characteristic impedance of the line by introducing additional capacitance to the CPW line. CPW geometry optimization using Ansoft High Frequency Structure Simulator (HFSS®) reveals that higher characteristic impedance of the unloaded line is necessary for better tuner smith chart coverage. Therefore the characteristic impedance of the unloaded line (without varactors) is optimized to 63Ω through adjusting the signal width W=15µm, CPW gap G=35µm, metal strip width d=1µm, and metal strip gap g=1µm. Higher CPW gaps and narrower signal width would result in higher characteristic impedance but causes significant attenuation of CPW modes.

TABLE I
LUMPED ELEMENT MODEL PARAMETERS OF THE CPW LINE.

Component values extracted from ADS for the lumped element model of the CPW line with W=15µm and G=35µm on the shielded Si substrate.	
Lt (nH/m)	531.25
Ct(pF/m)	78.125
R_t (Ω/m)	625
G_s (Ω^{-1}/m)	0.1563

IV.TUNER MODELLING

A. Circuit Model

In order to model the reconfigurable tuner, first the CPW line is represented with a lumped element equivalent circuit model. The unloaded transmission line with floating shield designed in HFSS is modeled using a cascade of short stubs in Advanced Design System (ADS®). The data from the HFSS is used to model each small section of the transmission line with lumped elements in ADS.

Since the varactors are distributed uniformly and placed close enough to each other (s=32µm), the transmission line between two adjacent varactors can be modeled by one set of lumped element model. Therefore, the tuner circuit model can be easily constructed by adding the varactor pairs to each stub. Fig.3 shows the ADS model of each small stub of the CPW line of length *s* before and after it is loaded with the varactor pairs. There is a pair of varactor at each node so the equivalent capacitance is doubled. The loss corresponding to each varactors is modeled by a series resistor. When the varactor presents the smaller capacitance C_{min}, it has less loss $R_{vlossmin}<R_{vlossmax}$ therefore the varactor in C_{min} state has higher quality factor than C_{max} state.

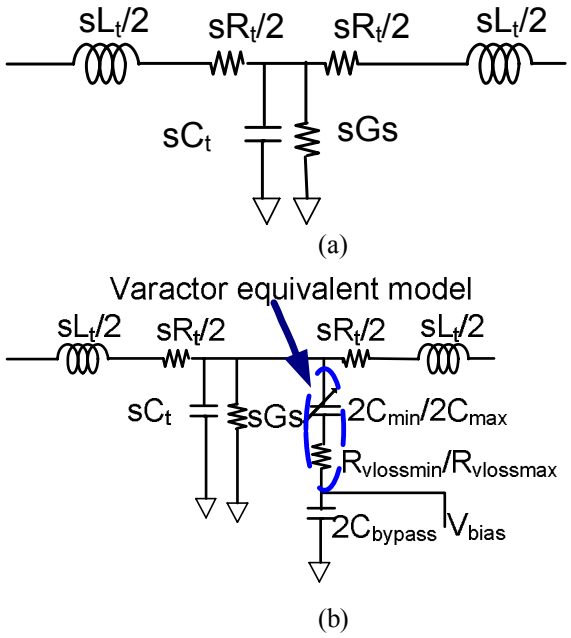

Fig. 3. Lumped element model of a short stub of transmission line. (a) unloaded stub. (b) loaded stub.

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In the design process, the values of the lumped elements (L_t, C_t, R_t and G_s) are optimized such that the simulated S-parameters from ADS model for the unloaded CPW line (Fig. 3(a)) fits the HFSS result. Table I shows the lumped element model parameters of the CPW transmission line used in the tuner extracted from ADS.

The CPW transmission line optimized for the reconfigurable tuner has been fabricated separately on the same chip. This structure is measured, simulated using HFSS and modeled by ADS. Fig.4 shows a good match of the transmission coefficient (S_{21}) and reflection coefficient (S_{11}) of the CPW line obtained from measurement, simulation and model data.

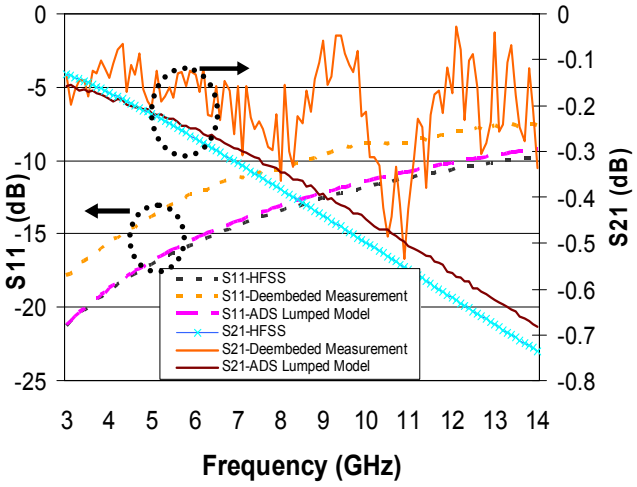


Fig. 4. S parameters of the unloaded CPW line obtained from HFSS simulation, lumped element model in ADS and measurement of the CPW line.

By cascading N=44 of the loaded stubs shown in Fig.3(b), the whole reconfigurable tuner is simulated in ADS.

B. Analytical Model

It is impractical to measure 2^{22} different configurations of the tuner. After an agreement between the simulation and measurement is established, an analytical model is needed to show the smith chart coverage. The binary bias voltage applied to the four varactors of each stub (1V or -1V), sets the S matrix of the stub to be a function of either C_{min} or C_{max}. The lumped element parameters derived from ADS are used to calculate the S parameters of each stub of length *s* and then the total S parameters of the tuner are calculated in MATLAB.

When the CPW line is loaded with varactors, its characteristic impedance changes according to the binary bias of each two varactors pairs (V_{GS}=-1V or 1V). Thus the characteristic impedance of each local CPW stub is either Z_{min} or Z_{max}. The approximate value of Z_{min} and Z_{max} can be calculated as:

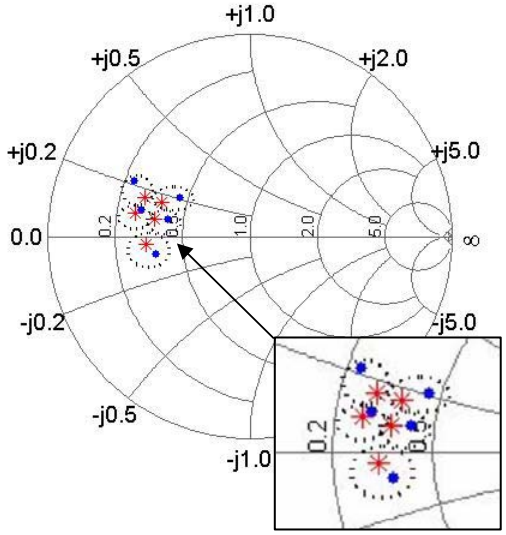
$$Z_{\min} = \sqrt{\frac{sL_t}{C_{\max} + sC_t}} \qquad (1)$$

$$Z_{\max} = \sqrt{\frac{sL_t}{C_{\min} + sC_t}} \qquad (2)$$

C_{max} is imposed on each stub that has the high bias voltage (V_{GS}= 1V), hence that stub has the local characteristic impedance of Z_{min}. Additionally, since varactors in the C_{max} state have lower quality factor than the C_{min} state, the loss of tuners with more Z_{min} stubs is higher than tuners with more stubs in the Z_{max} state.

V. MEASUREMENT

We have performed 2-port S-parameter measurement of the fabricated tuner using Agilent 8722 Network Analyzer and on-wafer probing. Calibration is done using a SOLT standard substrate and de-embedding is performed using the open-thru test structures on the chip.



● : Simulation, * : Measurement

Fig. 5. Input impedance of the tuner based on simulation and measurement of 5 different varactor bias configurations (N=44, s=32μm, C_{min}=91fF, C_{max}=132fF). Output of the shift register attached to the bias lines (1==1V and 0==-1V): 11111111111111111111, 00000000111111111111, 00000000000000000000, 11111111000000000000, 11001100110011001100. Corresponding measurement and simulation data are enclosed in the same circle.

Using a shift register in the design allows us to test the tuner in any of the 2^{22} states without needing to probe each bias node separately. Using this field programmable capability, we have entered different streams of data through the shift register and measured the 2 port S parameters. In Fig. 5, five different streams of data corresponding to 5 different points on the smith chart are shown. The simulation results from ADS are also included for comparison.

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Fig. 6 shows measured and simulated S-parameters of the tuner when all varactors are biased at either 1V or -1V. These measurements corresponds to characteristic impedance of Z_{min}=12.4Ω and Z_{max}=19Ω, respectively. The match between simulation and measurement in the Z_{max} state is better than the one achieved in Z_{min} state since the varactor model is more exact when its V_{gs} bias voltage is -1V.

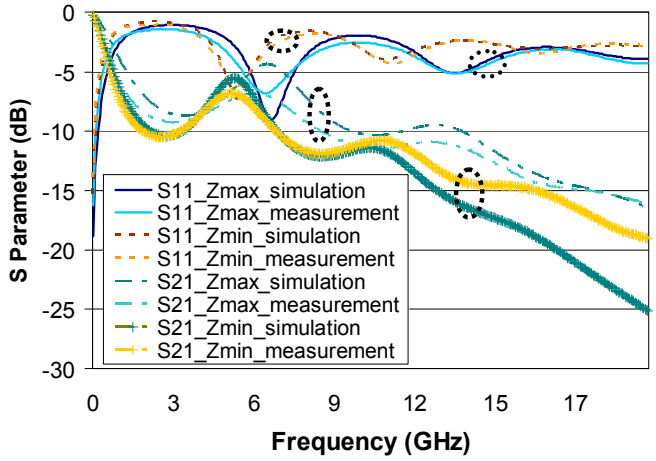

Fig. 6. S parameter of the tuner vs. frequency for two different configurations, Z_{max}: All bias voltages are -1V, Z_{min}: and all bias voltages are 1V.(N=44, C_{min}=91fF, C_{max}=132fF).

Equations (1) and (2) are used to demonstrate the Smith chart coverage of the tuner for operating frequencies of 5.8GHz and 7.8GHz as shown in Fig. 7 and Fig. 8, respectively. At frequencies below 4GHz the varactor values are too small to load the line resulting in very small coverage of the Smith chart. On the other hand, at frequencies above 11GHz, dominant tuner loss reduces the Smith chart coverage.

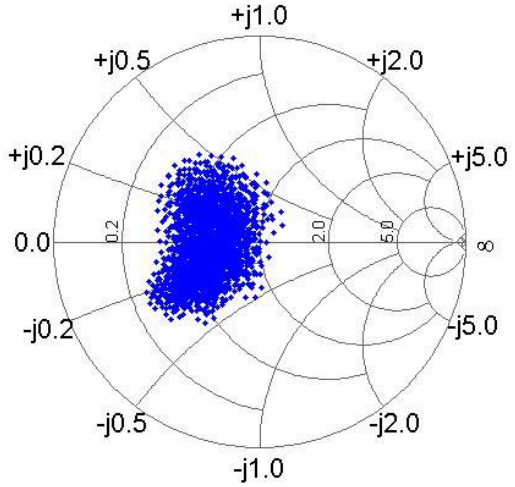

Fig. 7. Tuner Smith chart coverage at f =5.8GHz.

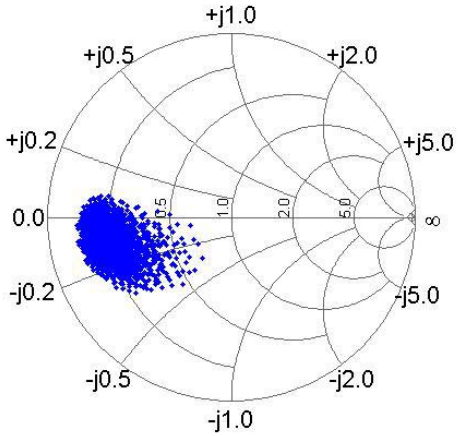

Fig. 8. Tuner Smith chart coverage at f=7.8GHz.

VI. Conclusion

In summary, a reconfigurable and programmable fully integrated CMOS RF tuner for multi-GHz software defined radio is demonstrated. Through optimizing varactors and by reducing the loss of CPW transmission line by adapting to a slow-wave structure, proper operation from 4GHz to 11GHz is achieved. Simulation and analytical models of the tuner are developed and their consistencies with the measurement results are verified.

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