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# High- $Q$ micromachined three-dimensional integrated inductors for high-frequency applications

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Three-dimensional micromachined inductors are fabricated on high-resistivity (10 k $\Omega$  cm) and low-resistivity (10  $\Omega$  cm) Si substrates using a stressed metal technology. On high-resistivity Si substrate with low- $k$  dielectric material (SU-8<sup>TM</sup>), this technology achieves a quality factor  $Q$  of 75 for a 1 nH inductor at frequencies around 4 GHz and a self-resonant frequency  $f_{sr}$  above 20 GHz. Using Si bulk micromachining to etch away the low-resistivity Si substrate with a combination of deep reactive ion etching and tetramethyl ammonium hydroxide etching methods, a 1.2 nH inductor achieves a peak quality factor  $Q$  of 140 at a frequency of 12 GHz with a self-resonant frequency  $f_{sr}$  above 40 GHz. The dependence of high-frequency performance on the inductor's variables, such as the number of turns, turn-to-turn gap, and substrate type, has been investigated. Excellent performance is achieved by removing the substrate due to the complete elimination of substrate losses and the reduction of the parasitic capacitance. This technology is simple and provides high performance integrated inductors on Si or compound-semiconductor platforms. © 2007 American Vacuum Society. [DOI: 10.1116/1.2433984]

## I. INTRODUCTION

Deep submicron complementary metal-oxide semiconductor (CMOS) and SiGe bipolar CMOS processes have recently enhanced the performance of Si-based radio frequency integrated circuits (rf ICs) up to microwave frequencies. With cutoff frequency  $f_T$  and maximum oscillation frequency  $f_{max}$  of these transistors approaching 200 GHz,<sup>1</sup> integrated inductors have become one of the bottlenecks in designing state-of-the-art radio frequency (rf) integrated circuits. Integrated inductors play an important role in the performance achieved by several rf blocks such as voltage controlled oscillators, low-noise amplifiers, filters, mixers, and power amplifiers.<sup>2-5</sup> The performance of these blocks at high frequency is determined by inductors' Ohmic and dielectric losses, resonant effects, dispersion, and parasitic radiation. The impact of these high-frequency effects on circuit performance is measured by the quality factor  $Q$  and resonant frequency  $f_{sr}$ . The quality factor of an inductor  $Q$  is defined by the ratio of the energy stored in the inductor (magnetic energy) by energy dissipated in the form of heat. Higher  $Q$  inductors help minimize rf power loss, rf noise, phase noise, and dc power consumption of rf IC circuits, while at the same time tending to increase gain and efficiency of such circuits.

Implementing rf circuit blocks on integrated circuit technology introduced integrated spiral inductors that are compatible with the IC technology.<sup>6,7</sup> The drawback is that these inductors are characterized by relatively low quality factors.<sup>8</sup> This quality factor is determined by the inductor geometry, the type of interconnect metal (Al, Au, or Cu),<sup>9</sup> the thickness of the metallization, the vertical distance between underpass/air bridge to the inductor windings,<sup>10</sup> and the dielectric loss

of the substrate. Recent work has shown that removal of the substrate below the inductor structure can increase  $Q$  by two to three times.<sup>11</sup> This substantial improvement in  $Q$  is due to the reduction of the substrate parasitic capacitance and parasitic loss due to the fringing electric fields in the substrate.

In two-dimensional (2D) spiral inductors, the coil axis is perpendicular to the substrate; thus the magnetic flux penetrates the substrate in a perpendicular fashion. If the substrate is lossy, i.e., has free charge carriers, the magnetic flux induces an eddy current (circular movement of electrons around the magnetic flux and eventual phonon scattering), resulting in heat generation in the substrate. Therefore, part of the stored energy will be wasted to heat, which means the quality factor of the inductor is degraded.

To improve the quality factor of 2D planar inductors, other research groups have developed alternative technologies, such as shielding layers,<sup>12</sup> thick metal layers,<sup>13</sup> and air bridges<sup>14,15</sup> to create microelectromechanical system (MEMS) inductors. Floating-shielded bond pads<sup>12</sup> show 15% less parasitic capacitance and over 60% higher shunt equivalent resistance compared to standard on-chip inductors. Suspended-spiral<sup>14</sup> and overhang<sup>15</sup> inductors developed to achieve high quality factors have achieved  $Q$ 's in the order of 70 at 6 GHz (1.38 nH inductor<sup>14</sup>). These technologies need more complex processing that is often incompatible with standard IC fabrication. Other technologies more compatible with IC fabrication that enable high  $Q$  inductors have been reported. High quality wafer-level packaging (WLP) inductors<sup>16-18</sup> offers novel opportunities for the realization of high-quality on-chip inductors needed in rf front ends. For WLP inductors, a thin low- $k$  dielectric layer (benzocyclobutene) reduces substrate losses and the parasitic capacitance to the patterned ground shield. Quality factors in the order of 47 at 5 GHz for a 1.8 nH inductor have been reported.<sup>16</sup>

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Compared with 2D spiral inductors, three-dimensional (3D) inductors which are elevated over the substrate have the advantage of reduced substrate loss and reduced effective dielectric constant. In 3D inductors, magnetic flux is mostly parallel with the substrate surface above the substrate, resulting in less flux penetration into the lossy substrate. Substantially lower eddy currents are generated, resulting in an increase in the quality factor of the inductor. A complete elimination of eddy currents is possible through the removal of the substrate underneath the inductor, as shown in this work.

3D inductors typically demonstrate a very high self-resonant frequency. The bulk of the 3D device resides in the air, resulting in reduced effective dielectric constant, as opposed to 2D spiral inductors with an effective dielectric constant of average of Si and air. This reduces the parasitic capacitance ( $C_{\text{par}}$ ) of the 3D device. Therefore, as seen by the following equation, significantly higher self-resonant frequencies ( $f_{\text{sr}}$ ) compared to spiral inductors are achieved.

$$f_{\text{sr}} = \sqrt{\frac{1}{LC_{\text{par}}}}. \quad (1)$$

There have been various reports on technologies developed for on-chip 3D inductors including the alumina core 3D inductor,<sup>19</sup> metal via processes utilized in the inductors,<sup>20–22</sup> and the MoCr self-assembled out-of-plane 3D inductor.<sup>23</sup> These technologies have resulted in an excellent performance for 3D inductors with maximum quality factors of 30–70 and self-resonant frequencies of 2–15 GHz. These technologies, however, either are not fully compatible with Si microfabrication technology or require nonconventional processing steps that make the integration of these inductors in microelectronic circuits very challenging. The self-assembled out-of-plane MoCr inductors reported in the literature<sup>23</sup> have been adopted for IC fabrication at frequencies smaller than 2 GHz.

In this work, high- $Q$  3D inductors targeted for rf and microwave frequencies are fabricated on Si substrate using a three fabrication step stressed metal technology that is compatible with Si and compound-semiconductor microfabrication. The presence of a low- $k$  dielectric (SU-8™) material under the inductors proved to increase the self-resonant frequency  $f_{\text{sr}}$ . The developed stressed metal technology has been combined with Si bulk micromachining technology to remove the substrate underneath the inductor and to totally eliminate dielectric losses. This resulted in a significant boost to the quality factor and self-resonance frequency of the 3D inductors.

In the following section, we describe the details of the technology used to develop 3D micromachined inductors. In Secs. III and IV, we report the high-frequency characterization and modeling of the 3D inductors. Finally, Sec. V provides a discussion of the findings of this work.

## II. FABRICATION

The technology used to develop high- $Q$  three-dimensional inductors in this work is based on a recently developed

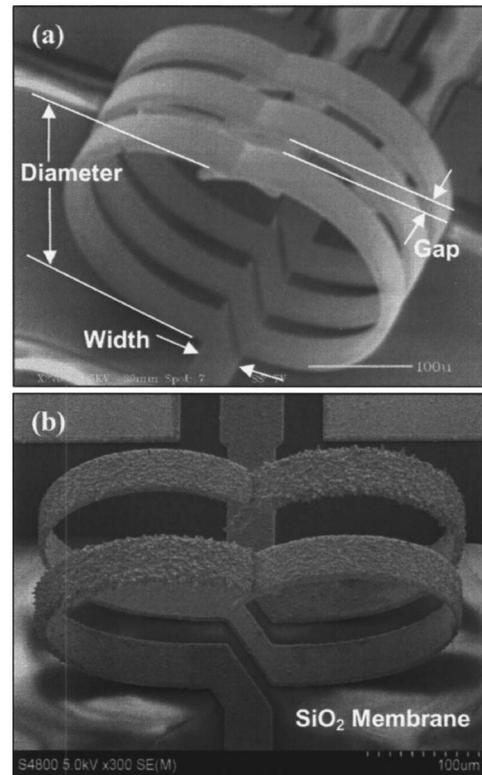


FIG. 1. (a) SEM picture of a 3D inductor. (b) SEM picture of a micromachined 3D inductor.

stressed metal technology.<sup>24,25</sup> Unlike the 3D inductor developed by Palo Alto Research Center,<sup>23</sup> which uses a sputtered MoCr metal layer to achieve high stress in the metal and to create the inductor loops, our fabrication technology is based on depositing a combination of Cr and Au thin metal layers, which are compatible with integrated circuit fabrication. Additionally, we have optimized the process for geometries (metal width, thickness, and winding diameter) to obtain inductors with optimum performance in a 1–15 GHz frequency range.

By adjusting the thickness of the deposited Cr and Au layers, one can achieve the right amount of stress (compressive in lower metal and tensile in upper metal) such that upon releasing the Cr/Au metal fingers from a sacrificial layer, the two ends of each metal finger bend upward and meet the neighboring fingers, as shown in scanning electron microscopy (SEM) pictures of the 3D inductor of Fig. 1. A final Au electroplating step is performed to improve the metal contact resistance and to augment the rigidity of the structure.

As one can see, the height of the inductor structure is more than 300 μm which is not compatible with current packaging technologies. Alternative packaging techniques such as encapsulating the structure in a Si cavity not only allows for packaging of the structure but also provides an effective shielding technique to mitigate undesired couplings in these structures. Additionally, 3D packaging technologies targeted for nonplanar devices such as MEMS and 3D passive elements can be utilized.<sup>26,27</sup>

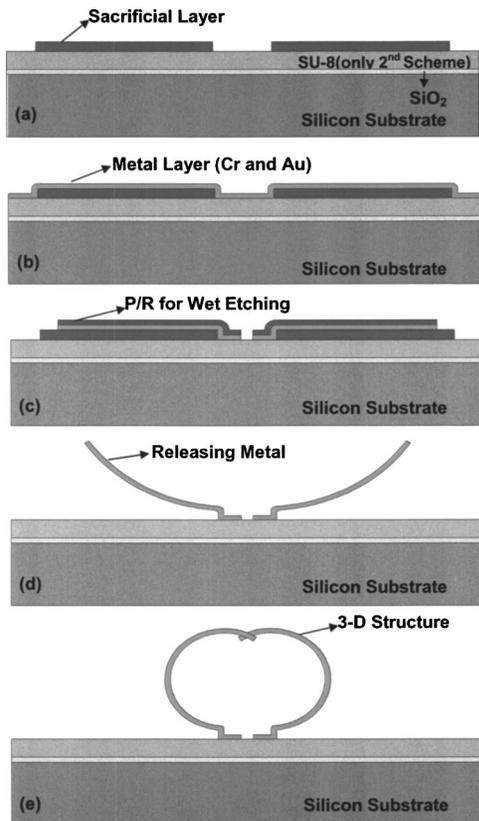


FIG. 2. Process flow for fabrication of an integrated 3D inductor.

To investigate the effects of the loss and parasitic capacitance of the substrate on the performance of the inductors and to obtain high-quality factors at frequencies higher than 1 GHz, we have developed three different variations of the technology. In the first scheme, the stressed metal combination is printed directly on a  $0.85 \mu\text{m}$   $\text{SiO}_2$  layer which is grown on the top of high- ( $10 \text{ k}\Omega \text{ cm}$ ) or low-resistivity ( $10 \Omega \text{ cm}$ ) Si substrates. The second scheme uses either a 6 or a  $20 \mu\text{m}$  SU-8<sup>TM</sup> as a low- $k$  dielectric layer (dielectric constant, 3.9) on top of a high-resistivity Si ( $10 \text{ k}\Omega \text{ cm}$ ) substrate to reduce the loss of the Si substrate and decrease the parasitic capacitance associated with the inductor fingers. A  $0.85 \mu\text{m}$   $\text{SiO}_2$  layer is also grown between the low- $k$  dielectric layer and the Si substrate for good adhesion. The third scheme uses the above 3D stressed metal technology on a low-resistivity ( $10 \Omega \text{ cm}$ ) Si substrate in combination with a backside Si bulk micromachining to completely eliminate the lossy substrate below the inductor structure. In addition to engineering the substrate loss by introducing a low- $k$  dielectric material or by backside micromachining, we have also varied the number of turns and turn-to-turn gap of the inductors to study the relevant effects. The winding metal diameter, width, and metal thickness were optimized to fixed values of 300, 45, and  $5 \mu\text{m}$ , respectively, to obtain high performance in a multigigahertz frequency range.

The steps in the first and second scheme are shown in Fig. 2. A hard-baked photoresist (AZ1518) sacrificial layer with a thickness of  $2 \mu\text{m}$  defined by a photolithographic process is

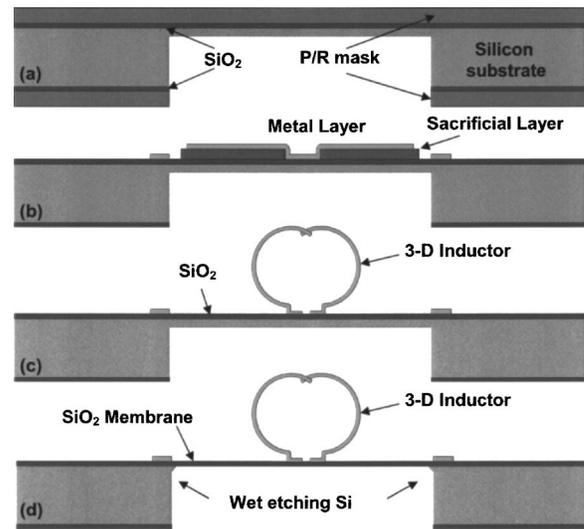


FIG. 3. Process flow for fabrication of an integrated 3D inductor on a micromachined Si substrate.

deposited [Fig. 2(a)] on top of the substrates. The substrate of the first scheme consists of  $0.85 \mu\text{m}$   $\text{SiO}_2$  and high- ( $10 \text{ k}\Omega \text{ cm}$ ) or low-resistivity ( $10 \Omega \text{ cm}$ ) Si. The substrate of the second scheme consists of  $0.85 \mu\text{m}$   $\text{SiO}_2$ , 6 or  $20 \mu\text{m}$  SU-8<sup>TM</sup> 2005 and high-resistivity ( $10 \text{ k}\Omega \text{ cm}$ ) Si. Using an e-beam evaporation process, a combination of chromium (Cr) and gold (Au) metal layers with thicknesses of 0.2 and  $0.8 \mu\text{m}$ , respectively, is formed [Fig. 2(b)]. A photoresist (AZ1518) mask for wet etching of metal finger patterns is defined. Chromium and gold layers are etched by chromium and gold etchants, respectively [Fig. 2(c)]. To release the metal fingers, the sample is put in a Baker-PRS2000 positive resist stripper solution for 1 h. During the releasing step, the top photoresist and sacrificial photoresist layer underneath metal fingers are removed, and the released metal fingers bend upward [Fig. 2(d)]. At the end of this step, both ends of metal fingers meet the neighboring fingers and form a three-dimensional inductive structure [Fig. 2(e)]. A  $4 \mu\text{m}$  Au electroplating step is performed to improve the conductivity of the three-dimensional metal windings and the stiffness of the three-dimensional structure. The process achieves a very high yield (over 90% device yield when excluding the edges of the wafer in a university clean room environment) without using any critical point drying step.

Figure 3 shows process steps of the 3D inductors fabricated on a micromachined substrate. In this scheme, using deep reactive ion etching, a partial etching of the backside of the Si substrate is performed first [Fig. 3(a)]. Then, the three-dimensional inductors are fabricated [Figs. 3(b) and 3(c)] on these partially etched areas using the Cr and Au stressed metal technology using the technology shown in Fig. 2. Finally, the remaining Si substrate underneath the 3D inductors is etched away by 20 wt % tetramethyl ammonium hydroxide at  $70 \text{ }^\circ\text{C}$  [Fig. 3(d)].

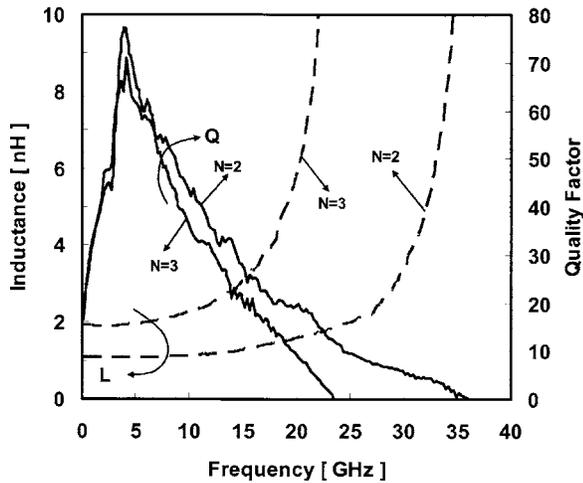


FIG. 4. Inductances ( $L_{\text{eff}}$ ) and quality factors ( $Q$ ) of two- and three-turn 3D inductors on a SU-8 20  $\mu\text{m}$  substrate.

### III. RF CHARACTERIZATION

Using the developed fabrication processes, various inductors with varying number of turns and turn-to-turn gaps are fabricated on a variety of substrates. These inductors had an effective diameter of 300  $\mu\text{m}$  (360  $\mu\text{m}$  for inductors on a micromachined Si substrate) and metal thickness of 5  $\mu\text{m}$ . The  $S$  parameters of all these inductors were measured with an Agilent 8510XF network analyzer for frequencies up to 40 GHz. As it is difficult to accurately measure high values of the quality factor, due to the very small loss values, careful calibration and repeatable deembedding of the pad parasitics have been performed by measuring the matched patterns.<sup>28</sup> Several devices of the same geometry have been measured to ensure low measurement errors. In this experiment, a short-open-load-thru calibration method was employed. The following observations are made.

#### A. Effect of the number of turns

Figure 4 shows the quality factor  $Q$  and the inductance value  $L$  extracted from  $S$  parameters for two-turn and three-turn inductors. These inductors are fabricated on a 20  $\mu\text{m}$  thick SU-8<sup>TM</sup> dielectric layer spun on the top surface of a high-resistivity Si substrate. As can be seen from the figure, a peak  $Q$  of 71 for the two-turn inductor is achieved at a 4 GHz frequency. The self-resonant frequency of the inductor is 36.5 GHz. For the three-turn inductor, a maximum quality factor  $Q_{\text{max}}$  of 78 and a self-resonant frequency of 24 GHz are observed. The maximum quality factor ( $Q_{\text{max}}$ ) slightly increases with increasing the number of turns since the effects of the metal loss and substrate coupling in these 3D inductors are not increasing as fast as the value of the inductance. In terms of the effective inductance value, an increased number of turns results in a higher effective inductance value. The self-resonant frequency decreases with the increasing number of turns because of a significant increase

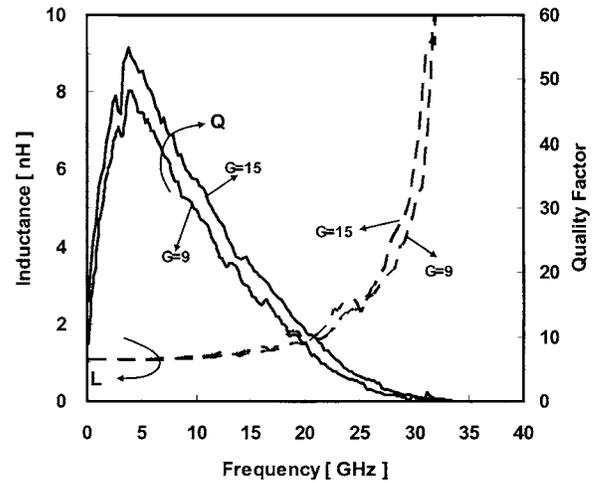


FIG. 5. Inductances ( $L_{\text{eff}}$ ) and quality factors ( $Q$ ) of two-turn 3D inductors with different turn-to-turn gaps.

in the value of the inductance (almost doubled from two to three-turns) and increased distributed turn-to-turn capacitance.

#### B. Effect of the turn-to-turn gap

We have fabricated and characterized 3D inductors with two different turn-to-turn gaps (9 and 15  $\mu\text{m}$ ) on a 0.85  $\mu\text{m}$  thick  $\text{SiO}_2$  layer deposited on a high-resistivity Si substrate. The results are shown in Fig. 5, where the inductor with the higher turn-to-turn gap (15  $\mu\text{m}$ ) has a higher quality factor  $Q$  in the entire frequency range up to the self-resonant frequency. The effective inductance value and the self-resonant frequency, however, seem to be unaffected by the turn-to-turn gap value. This indicates that the turn-to-turn gap contribution to the parasitic capacitance is minimal for gaps of 9 and 15  $\mu\text{m}$ .

#### C. Substrate effects

To investigate the effects of substrate loss and parasitic capacitance on the performance of a 3D inductor, we developed three different variations of the technology. In the first scheme, the stressed metal combination is deposited directly on a 0.85  $\mu\text{m}$  oxide layer. The substrate in this case is either a low-resistivity (10  $\Omega\text{ cm}$ ) or a high-resistivity (10  $\text{k}\Omega\text{ cm}$ ) silicon with 450  $\mu\text{m}$  thickness. In the second scheme we have tried to boost the self-resonance frequency and quality factor by using either a 6 or a 20  $\mu\text{m}$  SU-8<sup>TM</sup> as a low- $k$  dielectric layer. Incorporation of a low- $k$  dielectric layer reduces the overall loss and also reduces the value of the parasitic capacitance. In the third scheme we have suspended the 3D inductor on a thin dielectric layer by etching the Si substrate from the backside using bulk micromachining processes. A comparison between the inductance values and the quality factors of the first two technologies (high- and low-resistivity substrates with and without low- $k$  dielectric) for two-turn inductors is shown in Fig. 6. Substrate loss does not

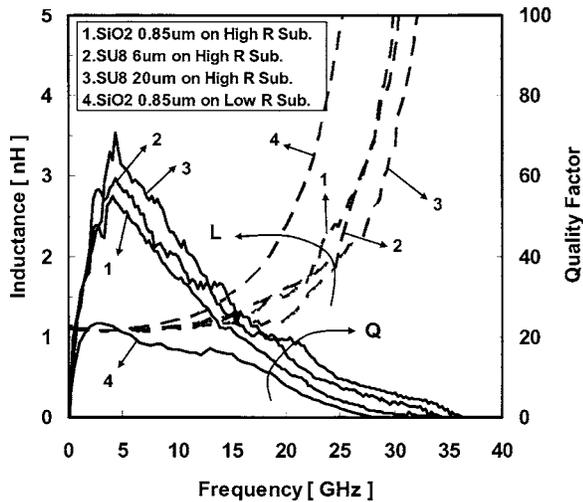


FIG. 6. Inductances ( $L_{eff}$ ) and quality factors ( $Q$ ) of two-turn 3D inductors fabricated on different substrates.

seem to affect the inductance value. This fact is independently confirmed by performing electromagnetic structural simulation using Ansoft HFSS. The quality factor and self-resonant frequency, however, are influenced strongly by substrate loss. The thicker the dielectric layer, the higher the value of the maximum quality factor  $Q_{max}$  and the higher the self-resonant frequency  $f_{sr}$ . This is due to the reduced dielectric loss and the reduced value of the effective dielectric constant. When the substrate is removed from the backside, the resulting inductors achieve a very high-quality factor, as shown for one- and two-turn inductors (see Fig. 7). Also, since the winding diameter is increased from 300 to 360  $\mu\text{m}$ , the inductance value for the same number of turns is higher compared to previous cases. A peak quality factor of 140 and a self-resonant frequency above 40 GHz were achieved for a one-turn inductor with an inductance value of 1.2 nH. The inductor had a quality factor higher than 50 for frequencies from 5 to 25 GHz.

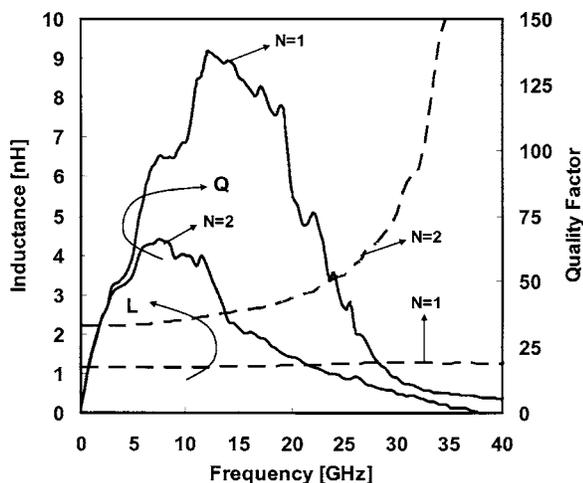


FIG. 7. Measured quality factor and inductance value of one-turn and two-turn inductors fabricated with 45  $\mu\text{m}$  width on a  $\text{SiO}_2$  diaphragm.

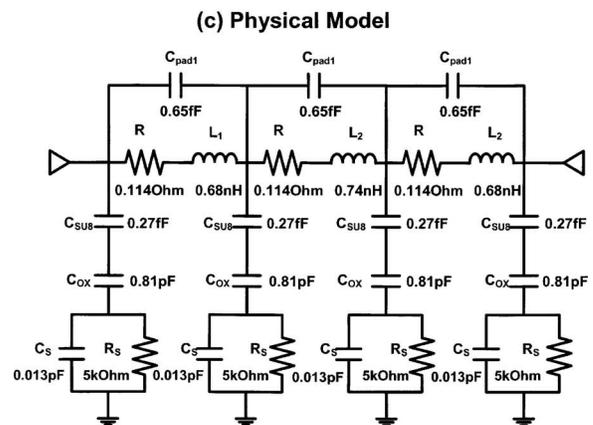
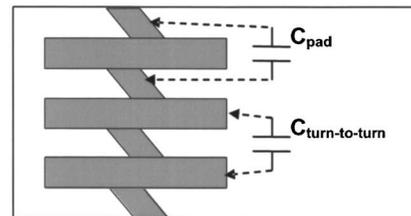
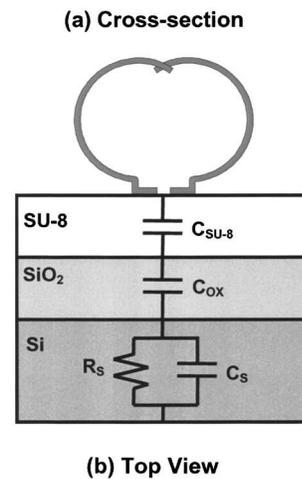


FIG. 8. Schematic view of a 3D inductor and its parasitics. (a) Cross-section view and (b) top view. (c) Physical model of the perfectly symmetrical 3D inductors developed in this work.

### IV. 3D INDUCTOR MODELING

Developing equivalent circuit models for 3D inductors not only helps us understand the physical limitation of inductors in terms of inductance value, quality factor, and self-resonance frequency, but is also useful to circuit designers in incorporating these models in SPICE-compatible circuit simulators. By their nature, 3D inductors are distributed devices. Thus the accuracy of their equivalent models is limited. In order to derive an accurate inductor model, it is critical to identify the relevant parasitics and their frequency effects. Since inductors store magnetic energy, the Ohmic resistance ( $R$ ) and parasitic capacitance ( $C$ ) adversely impact their performance. The parasitic capacitance stores unwanted electric energy, while the loss resistance dissipates energy.

The schematic view of a typical 3D inductor shown in Figs. 8(a) and 8(b) highlights the parasitics presented in the

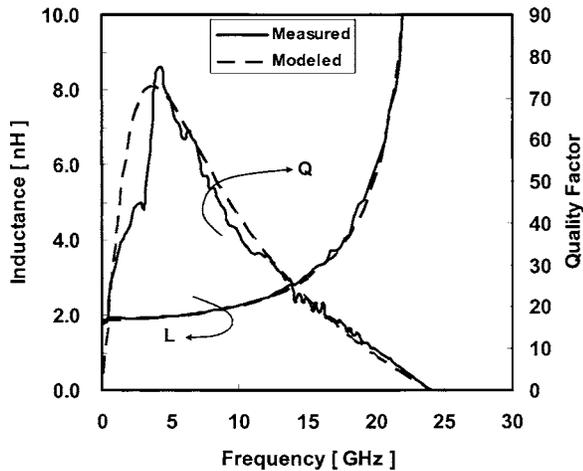


FIG. 9. Comparison between measured and modeled 3D inductors.

physical model. The circuit model of the inductor is directly related to the circuit layout or fabrication technology, the inductor geometry, and the constitutive characteristics of the substrate. As shown in Fig. 8, the inductance and resistance of the 3D inductor are represented by the inductance  $L$  and the series resistance  $R$ , respectively. The oxide and SU-8 capacitances are modeled by the series capacitances  $C_{ox}$  and  $C_{SU-8}$ . The capacitance and resistance of the silicon substrate are modeled by  $C_s$  and  $R_s$ .  $C_{pad1}$  represents the combined capacitance of the turn-to-turn capacitance in the air ( $C_{turn-to-turn}$ ) and the capacitance between the pad areas on the substrate surface ( $C_{pad}$ ). Figure 8(c) represents the physical inductor model extracted for the three-turn 3D inductor on a high-resistivity Si substrate. Note that while traditional 2D spiral inductors are not physically symmetrical, the 3D inductors are completely symmetrical, thus resulting in a simplified equivalent model.

The analysis of the inductors in this study was performed using Agilent advanced design system ADS software by extracting equivalent circuit parameters from experimental data obtained from  $S$ -parameter measurements. Based on the actual layout of the 3D inductors, parasitic values were first estimated and then fine tuned by both phase and magnitude optimization. Figure 9 shows a comparison between the measured and modeled three-turn 3D inductor. Even though the inductance value from the equivalent model completely matches that of the measurements, there is a minor mismatch between the  $Q$ -factor curves. This is attributed to small calibration and measurement errors that are inevitable in measuring high- $Q$  inductors.

## V. CONCLUSION

Various 3D integrated inductors based on a stressed metal technology and optimized for a multigigahertz frequency range are fabricated, characterized, and modeled. Using this process, the inductors fabricated on a micromachined Si substrate achieve record high self-resonant frequencies (above 40 GHz) and quality factors (as high as 140). For a 1.2 nH inductor, measured quality factors in excess of 100 are

achieved over a range of 7–18 GHz. For the same inductors, the quality factor of above 50 is achieved in the frequency range of 3–25 GHz. Three-turn inductors fabricated on a low- $k$  dielectric with a high-resistivity Si substrate exhibited a maximum quality factor of 78 and a self-resonant frequency of 24 GHz.

By experimentally studying the effect of different numbers of turns, different turn-to-turn gaps, and different substrates, the following conclusions are deduced.

1. For 3D inductors studied in this work, the inductance value increases in a quadratic manner with the number of turns.
2. Increasing the turn-to-turn gap from 9 to 15  $\mu\text{m}$  increases the quality factor but does not affect the inductor value and its self-resonant frequency. There is, however, an optimum gap value deduced from electromagnetic simulations. As the turn-to-turn gap increases, the fringing magnetic field that enters the lossy Si substrate increases, resulting in  $Q$  degradation. The optimum gap value that results in maximum  $Q$  for our 3D inductor geometries is found, by using HFSS simulation, to be 15  $\mu\text{m}$  for a high-resistivity Si substrate with 0.85  $\mu\text{m}$  of oxide.
3. Increasing the thickness of the low- $k$  dielectric material increases the quality factor at higher frequencies and improves the self-resonance frequency.
4. Increasing the resistance of the Si substrate improves the quality factor significantly but does not affect the self-resonant frequency.
5. For turn to turn gaps of 9 and 15  $\mu\text{m}$ , the effect of turn-to-turn capacitance is insignificant. The parasitic capacitance in this case is dominated by small metal footprints that the 3D inductor leaves on the substrate.
6. Excellent performance is achieved by removing the substrate due to the complete elimination of substrate losses and the reduction of the parasitic capacitance.
7. The equivalent circuit model of 3D inductors is fully symmetrical and thus easy to extract.

## ACKNOWLEDGMENT

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