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Conductance quantization and zero bias peak in a gated quantum wire

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Abstract

Conductance measurements are reported for an 0.4 μm wide GaAs/AlGaAs quantum wire with 7 cross-channel gates. The device exhibited integral conductance steps, magnetoconductance plateaus in agreement with the multiprobe formula and a conductance feature at $0.65(2e^2/h)$. Differential conductance measurements down to 50 mK revealed a zero bias conductance peak that vanished with an in-plane field of 1 T. The width of this peak was comparable to that reported in high mobility quantum point contacts (Phys. Rev. Lett. 88 (2002) 226805). At low conductances this device also exhibited single electron charging characteristic of a multiple quantum dot.

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1. Introduction

Conductance quantization is one of the fundamental discoveries of mesoscopic physics. In AlGaAs/GaAs quantum point contacts (QPC)

conductance plateaus occur at integral values of $2e^2/h$ corresponding to an integral number of electric subbands carrying the transport current [1,2]. While integral conductance quantization can be understood from a single-electron picture [3–5], the widely observed 0.7 conductance feature observed in QPCs appears to involve many-electron physics [6–13]. In this paper, we report conductance measurements on a 3 μm long quantum wire with seven cross channel gates. The device exhibited the characteristics of electronic

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waveguide conduction, including integral conductance plateaus and agreement with the multiprobe formula of Buttiker [3,4]. Evidence of an 0.7 conductance feature lead us to perform differential conductance measurements at milliKelvin temperatures. In that regime we observed a zero bias conductance peak similar to that reported in high mobility QPC's [7]. At conductances below $(0.3) \times 2e^2/h$ the device exhibited Coulomb blockade oscillations. The channel length of the quantum wire was comparable to the elastic mean free path, indicating that all aspects of quantum mesoscopic transport can exist even when the ballistic condition is only marginally satisfied. The data also suggest that the 0.7 feature is a general feature of single mode transport in 2DEG systems.

2. Experimental

Fig. 1 shows a schematic of a 7-gate device and an SEM image of the gated quantum wire region. The detailed fabrication procedures have been reported previously [14]. GaAs/Al_xGa_{1-x}As wafers with mobility of 500,000 cm²/Vs were patterned with optical lithography into 3 μm wide and 40 μm long Hall bars. The gated region of the mesa was further etched to a width of 0.4 μm. Electron-beam lithography was then used to pattern 90 nm wide cross-channel gate electrodes with a spacing of 230 nm. The two-dimensional electron gas (2DEG) was located 80 nm beneath the mesa surface. Hall measurements showed a carrier density of $n = 5.3 \times 10^{11}/\text{cm}^2$ in the 3 μm wide regions of the 2DEG. SdH measurements gave $n = 4.7 \times 10^{11}/\text{cm}^2$ in the 0.4 μm wide quantum wire region. The transport mean free path was approximately 5.5 μm, somewhat less than twice the length of the 0.4 μm quantum wire region. Four-lead conductance measurements were carried out in both a ³He evaporator cryostat and a dilution refrigerator. Standard lock-in techniques were used with a constant 19 Hz current of 0.3–2 nA amplitude. All leads to the device were pi-filtered (1 MHz rolloff frequency) at the cryostat head. For the dilution refrigerator measurements the sample was enclosed in a metallic shield attached

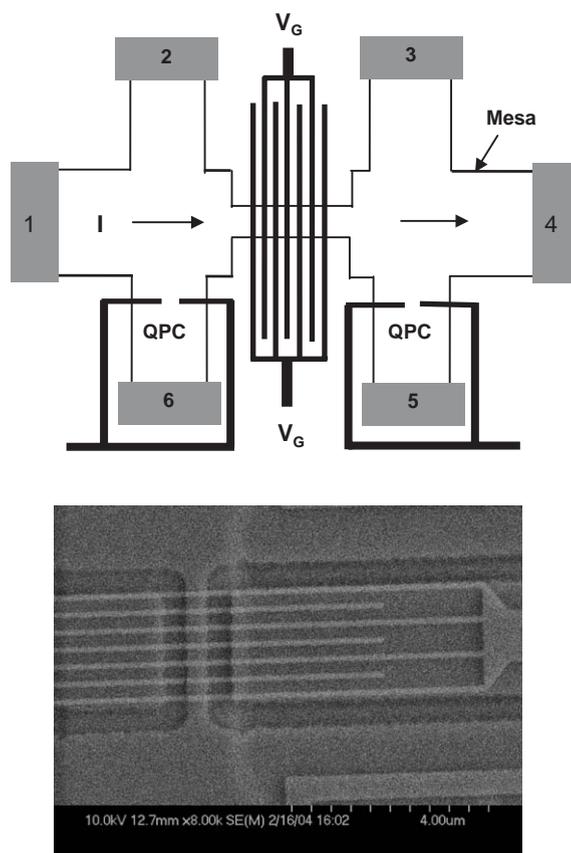


Fig. 1. (Top) Schematic of 7-gated quantum wire device. Numbered rectangles indicate ohmic contacts, dark lines represent gates. (Bottom) SEM image of gated quantum wire.

to the mixing chamber. Electrical leads passed through a copper powder/epoxy filter embedded in the low-temperature shield.

Because of periodic dilution refrigerator blockages the data were taken over three separate cooldowns. The cooldown number is indicated in each figure caption. The gate voltage location of specific conductance features often changed by substantial amounts from run to run, a situation that is common to GaAs/AlGaAs heterostructures. This behavior is often attributed to the movement of charged impurities introduced in the fabrication process. These impurities can produce built-in potentials that make the pinch-off voltage difficult to predict or control. For

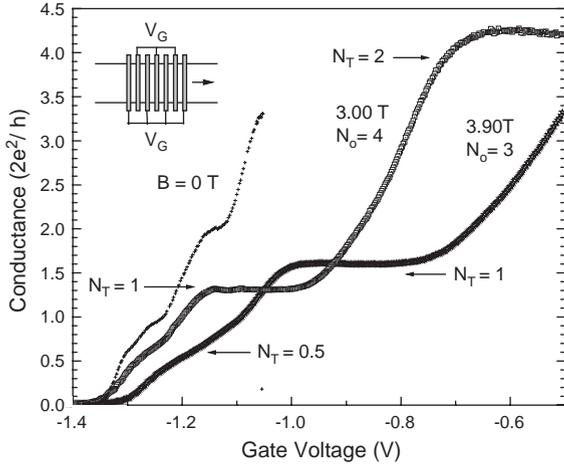


Fig. 2. Four-lead conductance versus gate voltage in the 7-gate quantum wire for $B_{\perp} = 0, 3.0, 3.9\text{ T}$ fields. Locations of the plateaus predicted by Eq. (1) are marked. $T = 0.4\text{ K}$ (Cooldown #1).

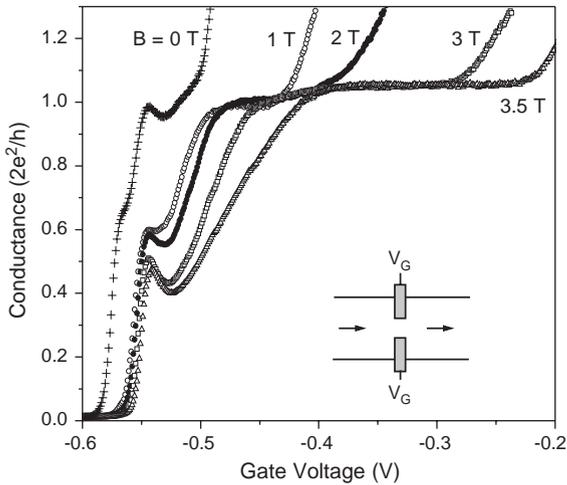


Fig. 3. Two lead conductance versus gate voltage for QPC 6 of Fig. 1. Magnetic fields $B_{\perp} = 0, 1, 2, 3, 3.5\text{ T}$ were applied (Cooldown #1).

example, Figs. 2 and 3 show considerably different pinch-off voltages for a QPC and the 7-gate quantum wire located on the same mesa of Fig. 1. Despite these differences, the plateau conductances were reproducible and indicate electronic waveguide conduction.

3. Waveguide conduction

Fig. 2 shows the conductance versus gate voltage for the 7-gate quantum wire on the same chip. In this case, the current flowed from contact 1 to 4 and a 4 lead measurement was possible. In zero magnetic field there are steps at 1 and 2 conductance quanta. The total length of the $0.4\ \mu\text{m}$ wide region is $3\ \mu\text{m}$ and the elastic mean free path was $5.5\ \mu\text{m}$, so the transport was marginally ballistic. The imposition of a quantizing perpendicular magnetic field results in very strong conductance plateaus, as shown. In the noninteracting electron approximation the 4-lead conduction through a coherent structure is expected to obey the multiprobe formula of Buttiker [3,4]. This approach provides an elegant description of quantum transport that easily incorporates transport by quantum Hall edge states. Detailed modeling is required to obtain the transmission coefficients for a particular structure but once these are known the conduction for any combination of voltage and current probes is determined. When the magnetic field induces an integral number of Landau levels in the “bulk” 2DEG, as will be the case here, the situation is particularly simple. When N_0 Landau levels are filled, an equivalent number of spin-degenerate edge channels conduct current in the bulk, $3\ \mu\text{m}$ wide mesa region, shown in Fig. 1. Conductance plateaus occur when N_T channels are transmitted through the gate region while the rest are reflected back into the bulk 2DEG. Using the multi-probe formalism, the 4-lead longitudinal resistance is given by [3,4]

$$R_{XX} = \frac{h}{2e^2} \left(\frac{1}{N_T} - \frac{1}{N_0} \right). \quad (1)$$

This result has been verified in both quantum point contacts and rectangular barriers where the channel width was much greater than the Fermi wavelength [15–18]. Our device is somewhat different from those studied previously since the gated region was narrow enough to support only a few modes of conduction. Fig. 2 shows the conductance quantization for $B = 3.0\text{ T}$ and 3.9 T corresponding to $N_0 = 3$ and 4 bulk Landau levels, respectively. The horizontal arrows mark

the longitudinal conductance predicted by Eq. (1) for $N_T = 1$ and 2 spin-degenerate edge channels. For the lower field the agreement is very close while for the larger field the discrepancy is a few percent. No attempt was made to subtract off a series resistance from these plots. These data demonstrate that the 7-gate wire exhibits the behavior one would expect for a few mode electronic waveguide.

4. 0.7 Conductance feature and zero bias peak

Since the main concern of this paper is the 0.7 conductance phenomenon, Fig. 3 shows this feature in the conductance versus gate voltage trace for the left QPC (Fig. 1). The current flowed from contact 2 to contact 6 and the geometry therefore forced us to perform a two lead measurement. A perpendicular magnetic field increases the 1D subband spacing and results in wider, flatter integral conductance plateaus, as shown. There is also a clear conductance knee near 0.65 quanta. The magnetic field caused this feature to migrate toward 0.5 and also gave the knee a more resonant shape. Earlier studies showed that breaking of the spin degeneracy with an in-plane field forced the 0.7 feature toward 0.5 quanta [6].

Fig. 2 shows that the conductance of the 7-gate quantum wire also has a knee near 0.6–0.7 quanta. There has been considerable effort to understand this feature in QPCs. Theories invoking both a density-dependent spin energy gap [8] and a dynamical, Kondo-like mechanism [7,13] have been proposed. Evidence for the spin gap comes from conductance measurements on long, very high mobility wires in which the 1D carrier density (n_{1D}) could be varied continuously [8]. There, it was found that increasing n_{1D} caused the 0.7 feature to migrate toward 0.5 quanta, indicative of a spin-split plateau. Support for the Kondo picture has come primarily from the observation of a zero bias peak in the differential conductance, dI/dV_{ds} , of quantum point contacts [7]. This peak was observed at temperatures ranging from 80 to 670 mK. An in-plane magnetic field of order 6 T suppressed the peak and at intermediate conductances a field-induced peak splitting was observed.

Depending upon the gate voltage, the maximum zero bias conductance reached nearly to the “unitary” limit of $2e^2/h$ [7]. The peak was similar to that observed for the Kondo effect in quantum dots [19–21].

Despite the ubiquity of the 0.7 feature in conductance versus gate voltage measurements, a zero bias peak has been reported in only one set of devices, to our knowledge [7]. Fig. 4 shows a family of dI/dV_{ds} curves taken on our 7-gate quantum wire during a later run at 58 mK. Gate voltages varied from -190 to -140 mV in 2 mV increments. A zero bias peak appears whose maximum conductance reaches 0.66 conductance quanta before the peak vanishes. The valley–valley width of each zero bias peak is indicated by the two arrows and is plotted versus gate voltage in Fig. 5. Over the range of gate voltages where a peak was observable the zero bias conductance is less than 0.7 and the width is essentially constant, as reported in Ref. [7]. Our valley-to-valley width of 0.3 mV is also comparable to the FWHM of 0.15 mV reported there. For increasing zero bias conductance the peak width first decreased and then the peak vanished. Data in Ref. [7] also showed an initial decrease and then a rapid increase in width as the peak conductance reached $2e^2/h$. Fig. 6 shows the same measurement but with

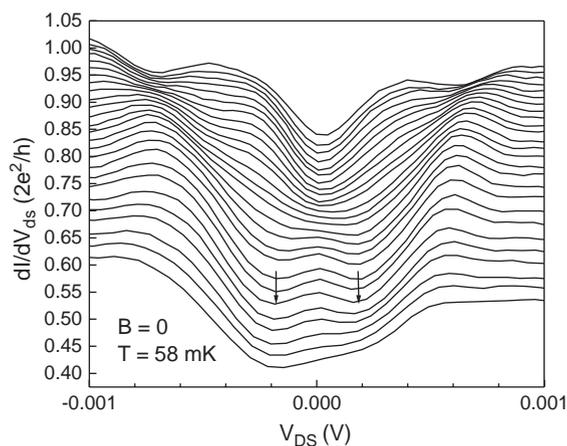


Fig. 4. dI/dV_{ds} of 7-gate quantum wire at 58 mK and $B_{||} = 0$. Gate voltages range from -190 mV to -140 mV. Arrows indicate the valleys defining the zero bias conductance peak (Cooldown #2).

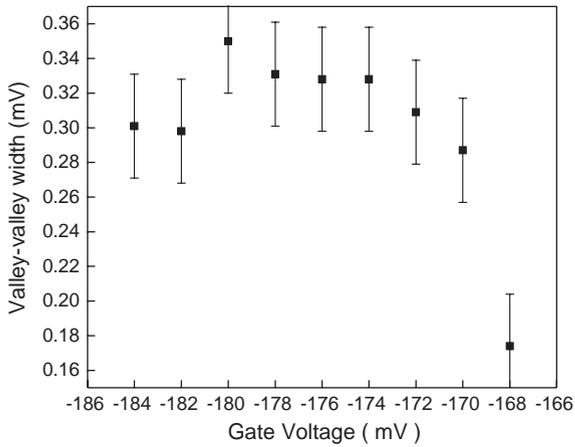


Fig. 5. Valley–valley width of zero bias conductance peak versus gate voltage (Cooldown #2).

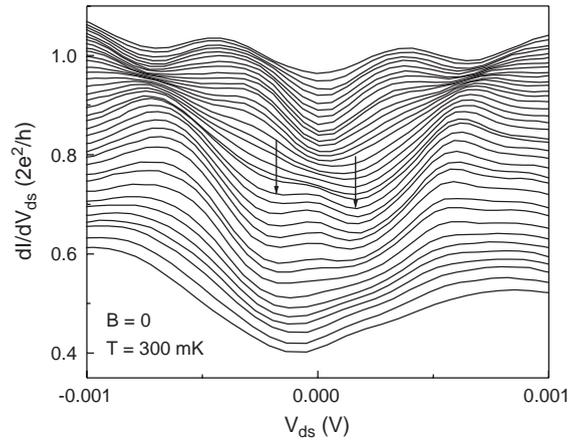


Fig. 7. dI/dV_{ds} at 300 mK, $B_{||} = 0$, for a series of gate voltages (Cooldown #2).

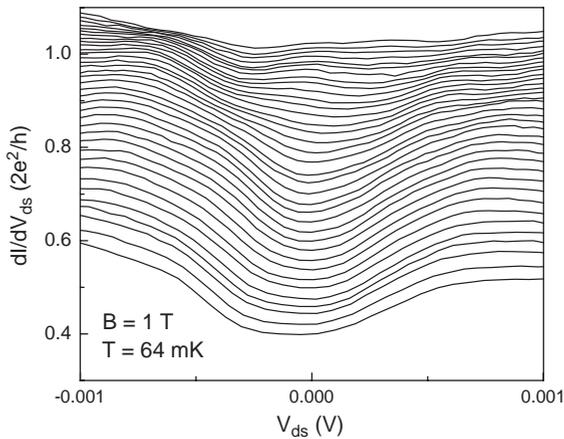


Fig. 6. dI/dV_{ds} at 58 mK and $B_{||} = 1$ T, for a series of gate voltages (Cooldown #2).

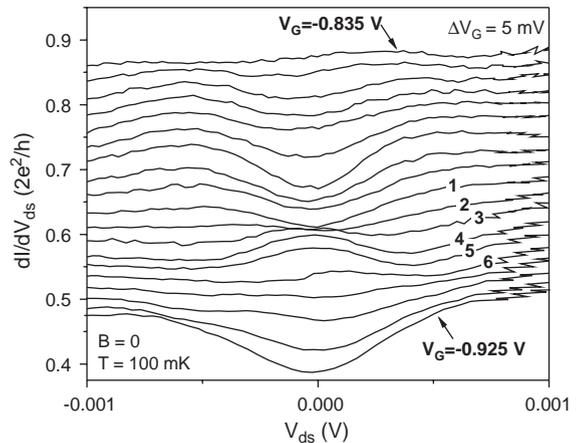


Fig. 8. dI/dV_{ds} at 100 mK, $B_{||} = 0$, with gate voltage curves in the vicinity of the zero bias peak labeled for analysis in Fig. 9 (Cooldown #3).

$B_{||} = 1$ T *in-plane* magnetic field. The zero bias peak has vanished completely. We did not observe a field-induced peak splitting for any gate voltage. Again, the data in Ref. [7] showed splitting only over a limited range of voltages so this aspect of the phenomenon may be device dependent. Finally, Fig. 7 shows the effect of raising the temperature to 300 mK. The zero bias peak remains but is less pronounced. However, the maximum conductance now reaches 0.7 before the peak vanishes. These data show that the zero bias peak for our 7-gate wire has qualitatively similar behavior to

the peak observed in high mobility QPCs [7]. This similarity is notable considering that our device had roughly 30 times the channel length of a QPC, an entirely different potential landscape, and was only quasi-ballistic.

In a subsequent cooldown the temperature dependence of the zero bias peak was measured. Fig. 8 shows a family of dI/dV_{ds} curves taken at 100 mK. The plot in Fig. 9 shows how the conductance of at zero DC bias changed with temperature for the curves marked 1–6 in Fig. 8.

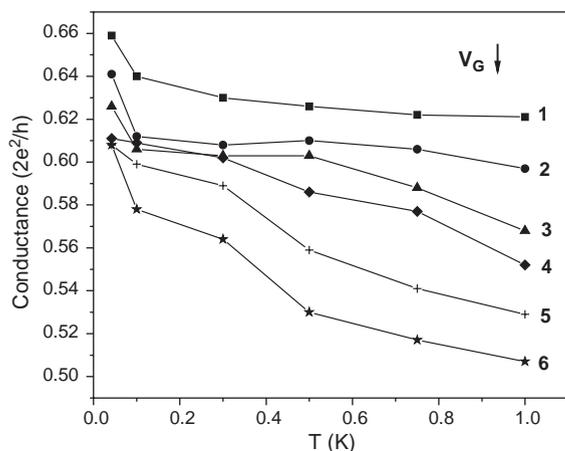


Fig. 9. Temperature dependence of the zero bias conductance for different gate voltages corresponding to sweeps in Fig. 8 (Cooldown #3).

Within the Kondo model for the zero bias peak, traces such as those shown in Fig. 9 should lie on a single universal curve when the temperature is rescaled as T/T_K , where $T_K(V_{\text{gate}})$ is the Kondo temperature for a given gate voltage. Although a consistent scaling factor could not be found for our data, the slow decrease of zero bias conductance with temperature was observed, as in Ref. [7]. Given the complexity of the potential landscape in our device, as compared to a QPC, it would be surprising if the temperature scaling would depend upon a single parameter such as the gate voltage.

We also performed measurements on three different 2-gate quantum wires. In all other respects, these were nominally identical to the 7-gate wire. None showed integral plateaus, an 0.7 feature or a zero bias conductance peak. In quantizing fields they did produce clean plateaus in agreement with Eq. (1). This result is somewhat perplexing. Integral plateaus result from single electron transport. All of the devices (2- and 7-gate) had close to the same mobility. However, the motion of even a single nearby charge can drastically influence the conduction in such systems and these effects are not predictable. It is possible that the 7-gate device accidentally had a more favorable potential landscape and showed

integral plateaus. By contrast, the 0.7 feature is commonly believed to be a *many* electron effect. There is evidence that many electron effects are *enhanced* in longer wires [11] which may be why we observed it in the 7-gate device.

Although our own data demonstrates the simultaneous appearance of an 0.7 conductance step and a zero bias peak, this does not appear to hold generally. Studies in ultraclean 0.5 and 1 μm quantum wires showed an evolution of the 0.7 feature toward 0.5 with increasing 1D carrier density, but no differential conductance peak [8]. While the 0.7 “knee” is a robust feature for a variety of structures, the amplitude of the zero bias peak may be highly device specific. For example, the maximum amplitude of the peak in Fig. 4 is roughly 3% of a conductance quantum while the peak in Ref. [7] was closer to 20%. In analogy to the wide variety of zero bias phenomena in superconductivity, the location of the peak at zero energy is universal, but the amplitude will likely depend upon the details of the conducting channel.

5. Single electron charging

The fabrication process can introduce a variety of uncontrollable factors such as 2DEG inhomogeneity, sidewall depletion in narrow mesas and charged impurities that alter the potential landscape. It is reasonable to ask if the cross-channel gates actually produced a potential modulation. In the low-conductance region the device can be considered a series combination of quantum dots and should exhibit Coulomb blockade oscillations. Fig. 10 shows conductance versus gate voltage sweeps for $T = 50$ to 500 mK. Since a change of the cross channel gate voltage affected both the dot potential and the barrier transmission we did not observe the clean separation between Coulomb blockade peaks that occurs when a “plunger” gate is used. Instead, we observed oscillations superimposed on an increasing background conductance as the barrier transmission increased with gate voltage [22]. Fig. 10 shows an oscillation period, $\Delta V_{\text{gate}} = e/C_{\text{gate}} = 16$ mV, corresponding to $C_{\text{gate}} = 1.2 \times 10^{-17}$ F. In 3-gate devices of otherwise identical dimension and mobility we

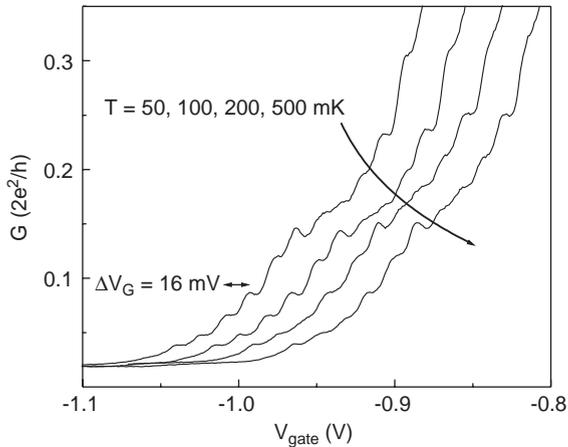


Fig. 10. Conductance versus gate voltage for $T = 50\text{--}500\text{ mK}$ showing periodic conductance oscillations. Successive curves have been shifted to the right for clarity (Cooldown #3).

found the same period within 5% so we associate the oscillation period with charge islands trapped between successive gates. In multiple quantum dots, when the interdot conductance $G_{\text{int}} \ll 2e^2/h$ the gate voltage periodicity is that of an individual dot. Once G_{int} exceeds $2e^2/h$, the system acts as a single charge island, with correspondingly smaller charging energy [23]. This behavior is consistent with Fig. 10. Assuming the 7-gates acted in series, we would expect the transition from weakly coupled individual dots to a single island to occur when the total conductance exceeds $(2e^2/h)/7$. After this point the oscillation period would decrease and, since the coupling to the charge reservoirs would exceed $2e^2/h$, Coulomb blockade oscillations would be suppressed. As shown in Fig. 10, once the total conductance reached approximately $(2e^2/h)/4$ the oscillations vanish, approximately as expected.

The geometry of our device was similar to the 3-gate quantum wire of Ref. [24]. There, an 0.7 feature was observed as well as integral conductance steps and Coulomb blockade oscillations. The oscillations persisted for interdot conductances well in excess of $2e^2/h$, probably owing to the higher mobility of the device. However, those authors did not report any differential conductance measurements so it is not clear whether their device exhibited a zero bias peak.

6. Conclusions

The conductance has been measured in a 7-gated quantum wire at temperatures down to 50 mK. This device exhibited a range of mesoscopic transport phenomena including integral conductance steps, quantized 4 lead magnetoconductance, an 0.7 feature with a zero bias conductance peak and single electron charging. The simultaneous presence of quantized waveguide conductance and the zero bias peak lends support to the Kondo-like interpretation of the 0.7 phenomenon. However, we were not able to fit the zero bias peak conductance to a universal function of T/T_K , as was done in Ref. [7].

Acknowledgements

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