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A Dual-Mode Programmable Distributed Amplifier/Mixer

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Abstract — A dual-mode field programmable RF amplifier / mixer is presented. Transistor switches, low loss CPW lines and RF transistors are combined in a 3-stage distributed topology which can operate as either a distributed amplifier or a distributed mixer. Functional reconfigurability is achieved using one bit programming without changing the signal path. The programmable module in its distributed amplifier mode provides a gain of 8dB in a 3-8 GHz bandwidth. When switched to the distributed mixer mode, it shows a measured average conversion gain of 4dB in a 1-16GHz bandwidth. This circuit is fabricated in a standard 130nm CMOS technology and occupies 4 mm×1.2 mm chip area.

Index Terms — CPW line, distributed amplifier, distributed mixer, field programmable, RF.

I. INTRODUCTION

Transceivers in multi-mode terminals have to deal with signals in different frequency bands that have various power levels and modulation schemes stemmed from multiplicity of wireless standards as well as the variations in the medium. To intercept these signals, the approach of using multiple receivers is not desirable due to high implementation cost, high power dissipation and accuracy issues. The flexibility achieved through real-time reconfigurable architectures addresses the demands for lower cost, lower power dissipation and less time to market in a compact single block with multifunction capability.

RF Reconfigurability based on multiple frequency bands has been explored to some extent [1]-[3]. In [1] a programmable common gate CMOS low noise amplifier (LNA) with an active inductor load capable of programming its center frequency is implemented. In [2], a software-driven re-programmable receiver for wireless signal interception is presented in which programmable digital filters are used to characterize the signal in different bands. An integrated dual-band tri-mode CDMA IF receiver with programmable channel-match filter is introduced in [3]. In [4] the authors have reported a field programmable fully integrated CMOS impedance tuner for applications in RF front end of software defined radios.

In addition to adaption to various frequency bands, programmable RF systems also require a wide dynamic range as well as adaptable mixing strategies. A receiver with a wide dynamic range provides a flat gain for a wide range of input power levels so that the desired message can be recognized above the noise level in a cluttered environment. The voltage

gain of high dynamic range receivers is conventionally controlled by additional circuitry such as gain control or offset control circuits [5]-[7]. On the other hand a receiver with programmable mixed signal blocks can provide the option of changing from super-heterodyne to homodyne mode. A software implemented combination of gain control loops and multi-stage mixing is proposed in [7] to handle a variety of signals in 2MHz-2GHz range. In this study for the first time we report the merging of the amplifying and mixing stages in a wideband dual-mode RF block suitable for implementation in real-time software-defined programmable receivers.

A programmable RF block that can be used as both amplifier and mixer can dynamically change the architecture of the front end of the transceiver. At each block it can be decided to either increase the signal level by using the block as an amplifier or move the signal to another frequency by choosing to use it as a mixer. The programmable RF block implemented here can be used as either a wide-band amplifier operating in 3-8GHz frequency range or as a wideband mixer operating in 1-16GHz frequency range. A distributed topology is used to implement the programmable block.

Distributed amplifiers are widely utilized in optical communication systems, broadband, military and security radio applications, satellite communications, broadband sensing as well as ultra-wideband (UWB) radios [8][9]. They can achieve flat gain and good input and output matching over a wide range of frequencies. In addition to broadband amplification, implementation of a broadband system may also require a broadband frequency conversion circuitry. For this purpose a distributed mixer can be used. Using a dual-mode amplifier/mixer, the signal can be amplified in an arbitrary number of blocks and then be converted to other frequencies using the remaining blocks. The gain of the system can be dynamically controlled by changing the number of cascaded blocks programmed as amplifiers and the mixing strategy can also be chosen based on the number of blocks programmed as mixers.

II. OVERVIEW OF COMPONENTS

A. RF Block

Active cells of a dual-mode RF circuit are used either as a gain stage or as a mixer cell. The schematic of the active cell

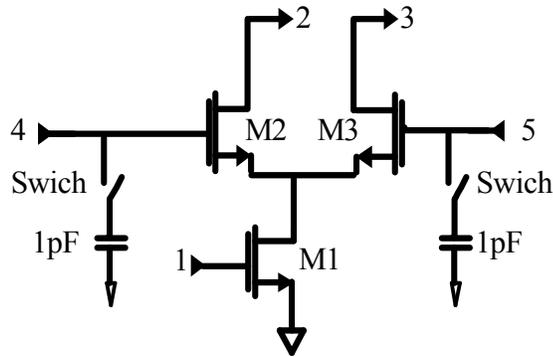


Fig. 1. Schematic of a differential RF block used as both amplifier and mixer cell. M1: $W=180\mu\text{m}$, $L=0.13\mu\text{m}$ with 25 fingers, M2 and M3: $W=200\mu\text{m}$, $L=0.13\mu\text{m}$ and 20 fingers

is shown in Fig.1. As an amplifying cell, the RF block can be viewed as two merged cascode cells. In this mode, each of the two transistors in the differential pair (M2 and M3) operate with the same signal amplitude and phase and individually create a cascode stage along with M1. In the mixer mode the two transistors operate together as a switch pair while M1 acts as a transconductance stage.

B. Transistor Switch

Switching functions are widely employed in multifunction multimode systems such as multi-input multi-output (MIMO) systems and phased array transceivers/antenna [10]-[11]. In these systems switches are typically implemented on the signal path so their finite insertion loss (S_{21} in on-state) or finite isolation (S_{21} in off-state) can deteriorate the signal. The main challenge in realizing programmable RF circuits have been the tradeoff between the insertion loss of switches in the on-state and the switch isolation in the off-state. Transistor switches are optimized for both their insertion loss and isolation based on the programmable RF function they mimic. Hence, adopting numerous switches on the signal path would result in significant performance degradation due to both switch loss and isolation. In this work RF switches are employed to couple/decouple RF transmission lines away from the signal path. Although in this proposed topology switches are not on the path of signal, their insertion loss and isolation still affect the performances of both amplifier and mixer. As a result, these switches need to be designed to yield optimum performance in both amplifier and mixer modes.

As it can be seen from Fig.1, there are two switches in each block controlled by the same signal. If the switches are on, the signals at ports 4 and 5 are AC-coupled to ground through two 1pF capacitors. Under this condition, M2 and M3 work as common-gate transistors that carry the amplified signal coming from M1 in a cascode topology. If the two switches are off the AC signal (which is the LO signal of the mixer) flows through these ports to the gate of the differential transistors (M2 and M3).

CMOS transistor switches have been widely studied [12]-[13]. These switches are compact, cost efficient and can be easily integrated when compared to RF MEMS switches. The high insertion loss, low isolation and mediocre linearity characteristic of CMOS switches often hinder their application in programmable RF systems. In this work NMOS transistors controlled by one common programming bit are utilized as switching elements. High isolation of these two switches in the off-state allows most of the LO signal power to reach the gate terminals of M₂ and M₃ of each RF block in the mixer mode. Low switch insertion loss in the on-state provides good AC ground through 1pF capacitors for the DC supply applied to ports 4 and 5 in the amplifier mode. Hence a better stability and higher amplifier gain are achieved in this mode.

Upon simulations for various transistor sizes a 20 finger RF transistor with $50\mu\text{m}$ width and 130nm length is chosen which provides high isolation above 15dB and low insertion loss below 2.5dB for frequencies up to 15GHz. Larger switch widths result in lower isolation (<15dB) and decrease the mixer conversion gain in the mixer mode as the LO signal power leaks to the ground. Smaller switch widths result in higher insertion loss (>2.5dB) which reduce the amplifier gain in the amplifier mode and may cause instability.

C. Transmission Line

All distributed designs use either real or artificial (lumped inductors and capacitors) transmission lines to support performance in a wide bandwidth [8][9]. Standard CPW transmission lines in CMOS technology suffer from significant loss at high frequencies due to dielectric losses of low resistivity Si substrate. To minimize the line attenuation due to conductor loss and penetration of EM fields into the lossy substrate, the top metal layer (and typically the thickest metal layer) in the CMOS process is employed for the CPW structure. Also to further reduce the loss an array of floating narrow metal strips are placed under the transmission line as proposed by [14]. These floating metal strips isolate the CPW structure from the Si substrate, effectively removing the dielectric losses associated with the Si substrate. This method enables us to obtain loss reduction of around 0.6dB/mm at 10GHz [4].

Ansoft High Frequency Structure Simulator (HFSS®) is used to design CPW lines that enable the circuit to have high gain in both amplifying and mixing modes. The optimized CPW lines for this application yields a signal width of $W=15\mu\text{m}$, a gap between signal and ground line of $G=35\mu\text{m}$ and metal strip width and gap of $1\mu\text{m}$.

III. FIELD PROGRAMMABLE RF CIRCUIT

The field programmable distributed circuit is shown in Fig. 2. It is a three stage distributed circuit with five CPW transmission lines used to tap the five terminals of each RF

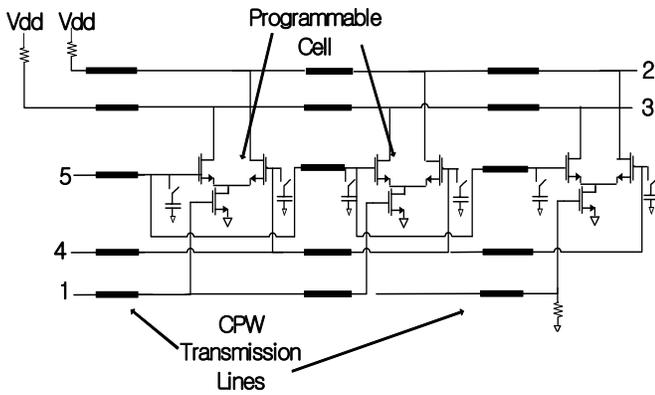


Fig. 2 Schematic of distributed programmable amplifier/mixer

block. There are 3 input ports (1, 4 and 5) and two output ports (2 and 3). The circuit is designed to operate as both a distributed amplifier and a distributed mixer implemented using shielded CPW lines. The programming is established by using embedded transistor switches in each RF block controlled by only one bit. The chip is fabricated in a standard $0.13\mu\text{m}$ CMOS technology with dimensions of $4\text{mm}\times 1.2\text{mm}$ as shown in Fig. 3.

A. Amplifier Mode

The conventional distributed amplifier consists of two transmission lines that connect the gate and drain terminals of multiple transistor stages. In the amplifier mode of the programmable distributed amplifier/mixer of Fig. 2, the RF block (shown in Fig.1) is used as two parallel cascode stages with the lower transistors merged. The input RF signal flows into the gate of the input transistor M1 and because all DC and RF signals are symmetric both differential pair transistors (M2 and M3) operate completely symmetric and amplify the signal equally with a zero phase difference. Only three transmission lines are used in the distributed amplifier (connected to ports 1, 2 and 3) while gates of the top transistors are biased at a fixed DC voltage. The two transmission lines connecting ports 4 and 5 in Fig.1 function as RF grounds through coupling capacitors in series with switches that are turned on. Therefore, the inductive effects of long transmission lines on these paths are removed.

B. Mixer Mode

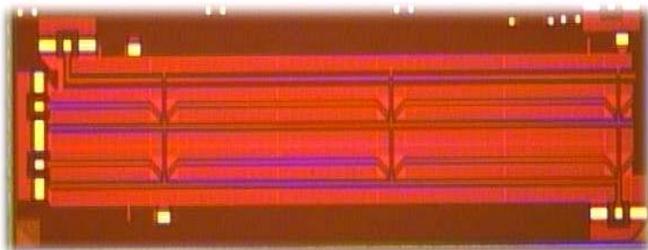


Fig. 3 Micrograph of the programmable amplifier/mixer

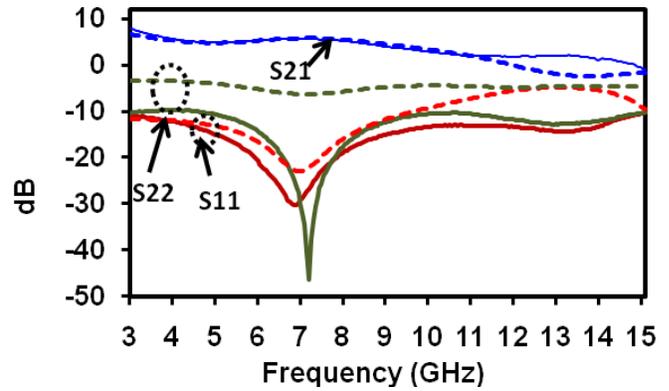


Fig. 4. Measured and simulated results in amplifier mode

The same circuit can operate as a distributed mixer. In this mode of operation, each RF block can be used as a fully differential single balanced mixer which effectively rejects the common mode noise. M1 acts as the RF transconductance stage while M2 and M3 having the same geometry and biasing conditions act as the switching pair with input signals at their gate applied with 180° phase difference.

In each cell the IF component is produced by multiplying the input RF signal by a periodic waveform at LO frequency. The RF signal flows through the transmission line 1 (Fig. 1) and reaches the gate terminal of the transconductance transistor in each cell. This signal acts as the gate-source voltage of transconductance transistors thereby generating a drain current proportional to the RF input signal. The differential pairs are driven by the large signal LO voltage applied at tap points 4 and 5. These transistors are turned on and off in each period of LO signal only allowing one of the transistors to conduct at half period. Since a large amplitude differential LO signal is applied to the switch pair transistors, their bias points and hence their transconductance is not fixed, so the IF output signal of each single balanced block is a function of both the LO voltage and RF signal. This switching mechanism modulates the current of the transconductance transistor and produces the IF signal at tap points 2 and 3 with 180° phase difference from each other. The differential pair only allows odd harmonics to be generated at the IF terminals.

The LO signal having frequencies as high as 16GHz may be attenuated if the isolation between the LO transmission lines and 1pF capacitors are not sufficient resulting in conversion gain degradation or high LO signal power requirement. In this implementation all the transmission lines for RF, LO and IF are symmetric, enforcing identical phase at each tap point and maximizing the IF power at the output.

IV. MEASUREMENT

On-wafer 2-port S-parameter measurement of the programmable circuit in the amplifying mode (switches on) is performed using an Agilent 8722 Vector Network Analyzer. Port 1 is the input port while any of the ports 2 or 3 or the

VI. ACKNOWLEDGEMENT

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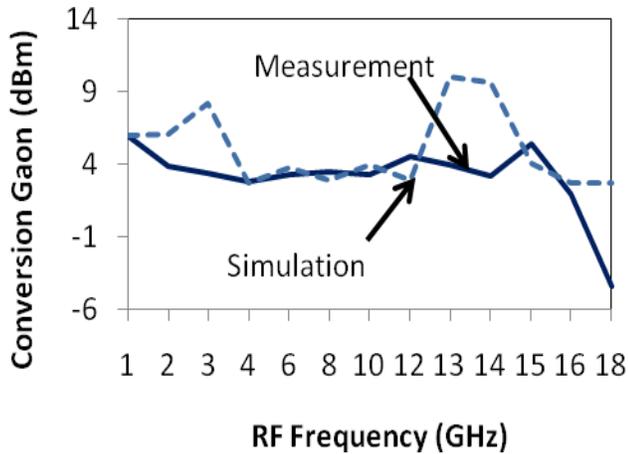


Fig. 5 Measured and Simulated conversion gain of the mixer as functions of RF frequency at $f_{IF}=300\text{MHz}$, $P_{LO}=10\text{dBm}$ and $P_{RF}=-15\text{dBm}$

sum of the two can be used as the output port. Measured and simulated S-parameters are shown in Fig.4 under $V_{DD}=4\text{V}$ and $V_G=2.2\text{V}$ with only port 2 power measured. A forward transmission gain of 8dB in the frequency range of 3-8GHz is achieved.

In the mixer mode when all transistors are switched off, both mixer conversion gain (IF power to RF power) and mixer linearity are evaluated using a 3dB coupler connected to a CW sweeping signal generators and an Agilent 8722 spectrum analyzer. The measured and simulated conversion gains of the mixer are shown in Fig. 5. A conversion gain of ~4dB in the frequency range of 1-16GHz is obtained under $V_{DD}=4\text{V}$, LO signal power of 10dBm, RF signal power of -15dBm and a fixed IF frequency of 300MHz.

The linearity of the mixer is measured using a single-tone measurement as the conversion gain is recorded for different RF input powers. The mixer shows an input-referred 1dB compression point of -5dBm.

V. CONCLUSION

A fully integrated programmable dual-mode RF amplifier / mixer based on low loss CPW transmission lines, dual-purpose active cells and integrated switches is presented. This circuit uses CMOS transistor switches programmed to connect / disconnect transmission lines to / from RF blocks to implement either cascode amplifying gain cells or single balanced mixer cells.

The circuit can be programmed to perform as both distributed amplifier and distributed mixer and is fabricated in a standard $0.13\mu\text{m}$ CMOS technology. In the distributed amplifier mode a forward transmission gain of 8dB in 3-8GHz range is achieved. In the mixer mode, a power conversion gain of around 4dB in 1-16GHz RF signal bandwidth is achieved.