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# A nanocapacitor with giant dielectric permittivity

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## Abstract

A nanocapacitor with ultra high capacitance ( $718 \pm 0.2$  pF) has been fabricated using electro-deposited Au nanowires manipulated between two Au microelectrodes by the dielectrophoresis technique. A high dc resistance value ( $\sim 100$  M $\Omega$ ) and nonlinear current–voltage characteristics indicate the formation of a dielectric interface between the nanowires. From frequency dependent conductivity, it is seen that the interface exhibits a giant dielectric permittivity ( $\epsilon \sim 1.8 \times 10^7$ ), which shows no frequency dispersion over the range from 30 Hz to 1 MHz. The enhancement of this permittivity value is attributed to the formation of a disordered interface containing gold atoms disrupted from the surface of the Au nanowires.

## 1. Introduction

During the last two decades, extensive research effort has been devoted to nanotechnology with emphasis on such topics as carbon nanotubes, nanowires, nanodiodes, single electron transistors, molecular data storage and drug delivery. Surprisingly, the area of nanodielectrics is relatively unexplored, despite the enormous scope of potential applications in power electronics and as gate electrodes in thin film transistors [1–5]. Perhaps the greatest opportunity in nanodielectrics is in nanoparticulate materials. Nanoparticles are the fundamental building blocks in the design and creation of several structural components in nanoscale devices. The novel and differentiating properties of these structures have been exploited to tailor device performance. A recent development in nanotechnology involves entities in which relatively few atoms or molecules are involved. A consequence of this finite dimension is that such entities cannot be considered in isolation; rather, the interface between them and their surroundings plays an important role in determining their properties.

With the development of nanotechnology, energy storage devices (batteries and supercapacitors) have drawn much attention for potential applications in the power sources

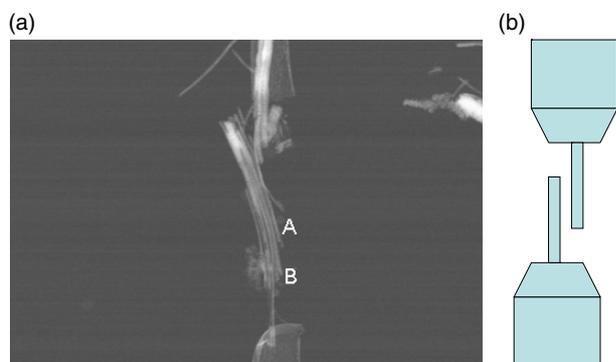
of various electronic products [6]. Recently, to provide enhanced capacitance, composite electrodes such as activated manganese oxide–carbon nanotube composites, polyaniline gold nanoclusters, etc, have been used for supercapacitor applications [7].

The dielectric properties of metallic nanoparticulate systems were first predicted almost 30 years ago [8]. It is only recently that a giant dielectric permittivity in an assembly of ultra fine silver metal particles, as a result of quantum confinement of electronic wavefunctions has been reported [9]. In the present work, we have used a completely different approach to create nanodielectric interfaces containing Au atoms between two nanoelectrodes to fabricate a nanocapacitor with an ultra high capacitance.

## 2. Experimental details

Figure 1(a) shows a SEM micrograph of our device in which a bundle of Au nanowires is manipulated between two Au microelectrodes by the dielectrophoresis technique [10]. The nanowires were grown by electrodeposition inside a porous anodic alumina membrane with a pore diameter of approximately 60 nm. Porous anodic alumina (PAA) templates, formed by a two-step anodization process, were used to template the growth of gold nanowires. Before anodization, each side of a 0.13 mm thick aluminum foil

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**Figure 1.** (a) SEM micrograph of the nanowire device. The wire A from one electrode and the wire B from the other electrode form the nanocapacitor. (b) Schematic diagram of the nanocapacitor. (This figure is in colour only in the electronic version)

(99.9995% purity, Alfa Aesar) was electropolished in a solution composed of 5 vol% sulfuric acid, 95 vol% phosphoric acid, and 20 g l<sup>-1</sup> chromic acid at 20 V at 80 °C. The first and second anodization steps were accomplished in 0.3 M oxalic acid at 40 V and 4 °C for 8 and 14 h, respectively. Following the first anodization step, the anodized PAA was removed in a solution composed of 3.5 vol% phosphoric acid, 96.5 vol% deionized water, and 45 g l<sup>-1</sup> chromic acid at room temperature for 8 h. This left behind an aluminum foil with self-ordered dimples on its surface. During the second anodization step, the pores initiated at the dimples, thereby forming a parallel array of 60 nm pores that were 25 μm in length. Gold nanowires were electrodeposited into the pores of PAA under galvanostatic conditions (2 mA cm<sup>-2</sup>) using a commercial solution (Orotemp 24, Technic Inc.). The gold nanowires were ~4 μm in length, corresponding to a growth rate of 1.9 nm s<sup>-1</sup>.

In the first step of device fabrication, Au microelectrodes and probing pads for electrical measurements were made on a Si wafer with a 500 nm thick SiO<sub>2</sub> layer by photolithography, Au deposition and photoresist lift off techniques. In the second step, the membrane was dissolved in NaOH, and after successive centrifugation and rinsing with deionized (DI) water, the nanowires were separated from the membrane. A clean solution of the nanowires, in ethyl alcohol, was prepared in a small beaker. Nanowires inside the microelectrodes were manipulated by the dielectrophoresis technique. For this, the substrate containing the microelectrodes was dipped into the nanowire solution, and using an ac signal with frequency 1 MHz and bias 15 V the nanowires were aligned in between the Au microelectrodes, as shown in figure 1. It should be noted that before electrical measurements the device was annealed at 400 °C for 30 min to make the nanowire contacts with the microelectrodes ohmic. The current–voltage characteristics were measured using a HP 4156A semiconductor parameter analyser using two probes. The C–V measurements were carried out using a Hewlett Packard 4284A C–V analyser.

### 3. Results and discussions

From figure 1(a) it is seen that a bundle of nanowires were connected at the top electrode and another bundle to the bottom

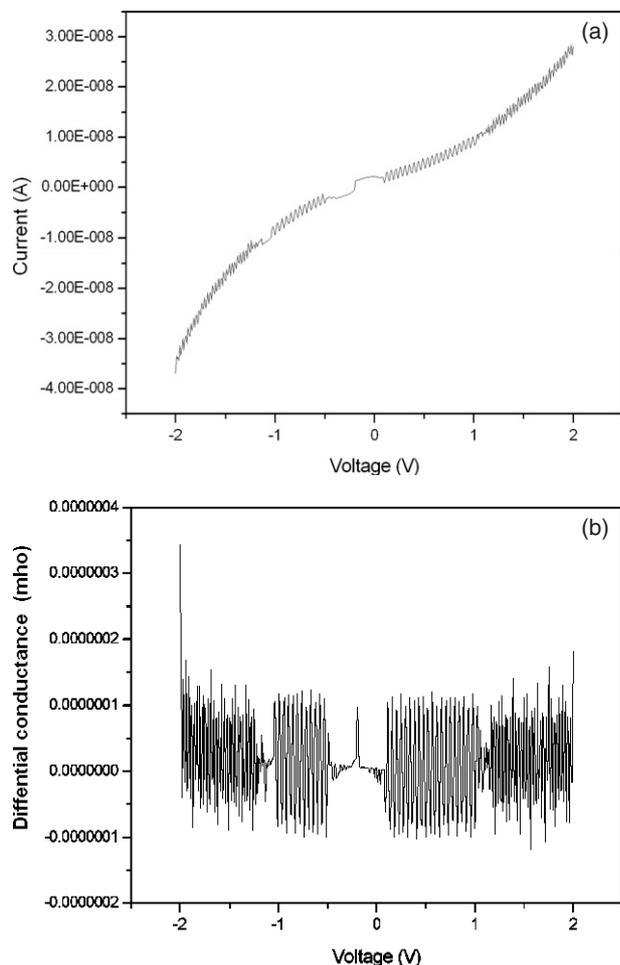
electrode. It is noted that in the dielectrophoresis technique the connection of the nanowires with the microelectrodes is ohmic in nature. This has also been verified in the present work by checking the resistance value of a separate device in which single wire was connected between the microelectrodes in a similar way. In the middle portion of the present device, shown in figure 1(a), nanowire A from the top electrode and B from the bottom electrode forms a nanocapacitor with interface thickness ~5 nm. Although, a number of nanowires are connected with the bottom electrode, they are all connected in the top position. Even if a few more participate in the formation of the nanocapacitor, the capacitance measurement will show the lowest one as they are connected in series. Therefore, we have considered the simple device structure as shown schematically in figure 1(b).

It is observed that the freshly fabricated devices show an open circuit characteristic, presumably due to poor contact between the nanowires and the Au microelectrodes or between nanowires. The insulating layer between nanowires may be due to a thin layer of Al<sub>2</sub>O<sub>3</sub> on the nanowires or a hydrocarbon layer which forms on Au upon exposure to air. Annealing the device at 400 °C decreased the device resistance significantly. The annealing mechanism is believed to be desorption of the residual hydrocarbon or adsorbed solvent, and possibly migration of the Au atoms through the insulating layer.

To characterize the device, we carried out current–voltage measurements, shown in figure 2(a), from which it is seen that the current is nonlinear with voltage, fluctuating with voltage at room temperature. The origin of this fluctuation might be due to nanocontacts of the gold atoms or clusters with the nanoelectrodes. A study of the temperature dependence of the current–voltage behaviour and also of the noise property are necessary to fully understand the origin of this fluctuation. Such work is now in progress. The corresponding differential conductance (dI/dV) calculated from the I–V characteristics, is shown in figure 2(b), exhibiting conductance fluctuations. From figure 2(a), the zero bias (dc) resistance is calculated to be ~100 MΩ. The conductivity of the material at the interface has been estimated, taking the dielectric thickness to be 5 nm and area as the length (2 μm) multiplied by a fraction of the arc (10 nm) over which the wire forms a nearly parallel plate capacitor to (~2.4 × 10<sup>-5</sup> S cm<sup>-1</sup>), which is very high compared to the conductivity of a bulk Al<sub>2</sub>O<sub>3</sub>.

The variation of capacitance, and the corresponding loss with frequency at zero bias voltage is shown in figure 3(a). From the figure, it is seen that the capacitance and the loss remain constant over the entire frequency range from 30 Hz to 1 MHz, which is due to the wide distribution of relaxation times. Considering a parallel plate capacitor with Al<sub>2</sub>O<sub>3</sub> as dielectric and dimensions the same as those taken in the conductivity calculation, the capacitance is estimated to be ~10<sup>-16</sup> F. Therefore, it is seen that the measured capacitance (718 pF) of the present device is enormously high (seven orders of magnitude) compared to the capacitor with Al<sub>2</sub>O<sub>3</sub> as dielectric. The capacitance may be calculated more precisely, using the expression for a parallel wire capacitor with a thin layer of Al<sub>2</sub>O<sub>3</sub> film (5 nm) between the nanoelectrodes, as

$$C = \pi \epsilon \epsilon_0 L / 4 \cosh^{-1}(d/R)$$

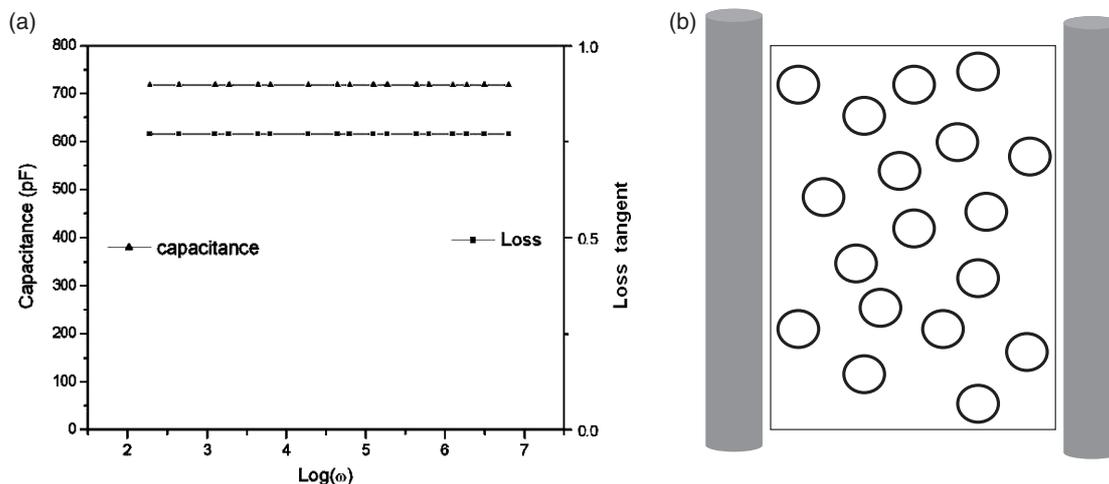


**Figure 2.** (a) Current–voltage characteristics of the nanocapacitor. (b) Conductance fluctuation ( $dI/dV$ ) calculated from the current–voltage characteristics shown in (a).

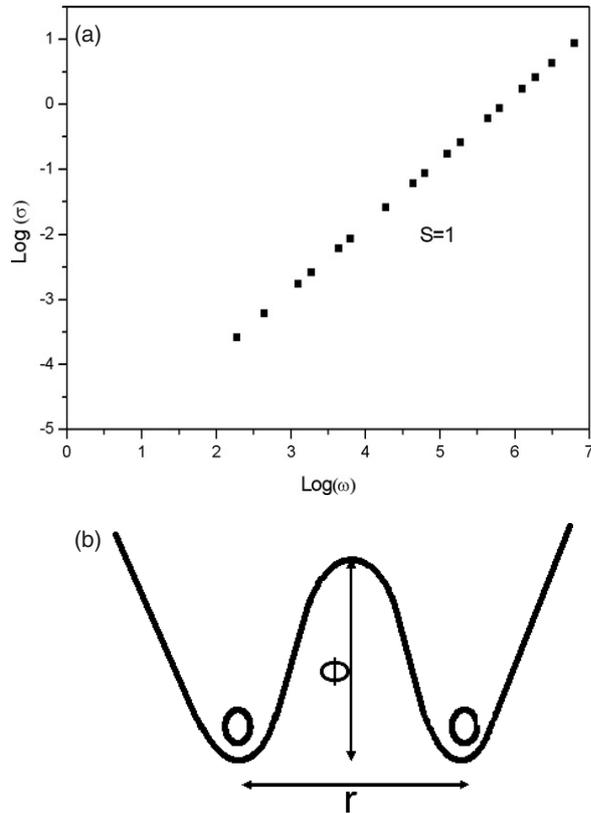
where  $\varepsilon$  is the relative permittivity of  $\text{Al}_2\text{O}_3$ ,  $\varepsilon_0$  is free space permittivity ( $8.854 \times 10^{-12} \text{ F m}^{-1}$ ) and  $L$  is the length of the wire,  $2d$  is the separation between the axes of the wires and  $2R$

is the diameter. Taking  $L$  as  $2 \mu\text{m}$ ,  $2R$  equal to  $60 \text{ nm}$  and  $2d$  as  $65 \text{ nm}$ , it is seen that the capacitance is almost the same as that obtained in the case of a parallel plate capacitor. We did not consider the stray capacitance of the nanowire contact with the microelectrode as it is ohmic. Only that with the substrate has been accounted for. Considering the permittivity of silica as 4, it is seen that the value is several fF, which is several orders of magnitude lower than the measured capacitance. The repeatability of the measurements has also been checked for other devices, for example, a capacitance of  $60 \text{ pF}$  and a loss tangent (ratio of  $\varepsilon''/\varepsilon'$ ) of 10 is obtained for another device (not shown).

We speculate here as to the nature of the dielectric interface that was formed in this experiment. It is believed from previous measurements [9] that Au nanowires formed by electrodeposition consist of an assembly of ultrafine metal particles or grains connected to each other. The size of the grains forming the wires depends on the growth rate. As a typical example [11], a grain size of  $10 \text{ nm}$  was obtained for a current of  $10 \mu\text{A}$  and  $1 \text{ nm}$  for current  $2 \text{ mA}$ . In the present device, it was observed that the wires were formed by ultra fine grains yielding a wire surface that was rough on the scale of the grain size. (e.g. figure 1 of [9]). It is also well established that the surface atoms of a nanoparticle are loosely bound, and that as the particle becomes smaller, more atoms in the nanoparticle become part of the ‘surface’, thereby depressing the melting point [12]. As the nanowires are formed by a large number of ultra fine particles, each nanowire forming the electrode for the present capacitor is considered as a metallic cylindrical core surrounded by a very thin layer of surface atoms that are loosely bound to the cylindrical core. During dielectrophoresis (manipulation of the wires inside the microelectrode) we applied a large voltage of  $15 \text{ V}$  across the electrodes. As soon as a good contact between the wires and the microelectrode was formed, the wires come very close to each other as a result of the high electric field between them. When the wires come very close to each other (of the order of few nanometers) the electrostatic force (due to the high field  $\sim 10^7 \text{ V cm}^{-1}$ ) on these atoms exceeded the elastic limit [13] (few nN). As a result, the Au atoms may be drawn out into



**Figure 3.** (a) Variation of capacitance and the corresponding loss with frequency. (b) Schematic diagram of the interface showing a disordered phase of gold atoms.



**Figure 4.** (a) Variation of total conductivity with frequency in the log scale. (b) Hopping of electrons over the energy barrier between the atomic sites.

the thin layer of residual alumina, forming a new disordered phase with a random distribution of Au atoms as depicted in figure 3(b).

Figure 4(a) represents the measured variation of conductivity with frequency. The frequency dependent conductivity in a disordered system is given by [14],

$$\sigma_{\text{tot}}(\omega) = \sigma_{\text{dc}} + A\omega^s$$

where  $\sigma_{\text{dc}}$  is the dc conductivity and  $s$  is the frequency exponent lying between 0 and 1. In disordered solids, non-Debye type relaxation behaviour has been widely discussed in the literature. Basically, there are two theoretical approaches to look at the relaxation phenomena. In the first case, a single particle hops across random barriers and/or trapping sites, whereas in the second case the hopping event involves many-particle interactions, i.e. the motion of a carrier is greatly influenced by the relaxation of its neighbourhood and the exponent  $s$  is a measure of the degree of interaction.

From the above equation it is seen that the variation of ac conductivity (excluding the dc contribution) with frequency plotted on the log scale gives a straight line, the slope of which is the frequency exponent  $s$ .  $s$  is extracted for the present device from figure 4(a), which gives a value of  $s$  equal to 1. This linear dependence of conductivity with frequency was first predicted [15] for atomic hopping in amorphous semiconductors, in which a fully or partially ionized atom hops over a random barrier separating the two sites. The

same behaviour ( $s = 1$ ) in chalcogenide (semiconducting) glasses was explained by correlated barrier hopping of electron pairs (bipolarons) between the charged centres [14]. Finally, when  $s = 1$  was found in ionically [16] conducting glasses it was concluded that the relaxation behaviour is universal, and will be manifest in systems in which the relaxation times of the polarizable centres are exponential functions of a random variable with a reasonably smooth and wide distribution. Such a variable may be a hopping distance, energy or a combination of the two. In the present device, ac conduction arises due to the motion of electrons between the Au atoms at the interface. The value of the exponent  $s$  equal to 1 indicates that the atoms are distributed randomly so that the relaxation parameter is a function of a smooth and random variable of distance ( $R$ ) and energy ( $\phi$ ), as shown in figure 4(b). It is seen that the dc conductivity is less than that obtained from ac conductivity extrapolating figure 4(a) down to zero frequency by a factor of 10. This means that the measured frequency range is well above the hydrodynamic range where the two-site approximation breaks down. The conductance fluctuation (figure 2(b)) with lower dc conductivity arises due to the formation of weakly coupled nanocontacts between the disordered phase and the electrodes through some Au atoms.

Considering a 5 nm gap between the wires, the relative dielectric permittivity has been calculated to be  $\epsilon \sim 1.8 \times 10^7$ . Recently [9], such a giant permittivity ( $10^{10}$ ) was reported in an assembly of ultra fine silver metal particles and attributed to quantum confinement of electronic wavefunctions using a metallic strand model<sup>8</sup> in which the dielectric permittivity is given by,

$$\epsilon \sim (1/2)q_s^2 l_0^2$$

where  $q_s$  is the Fermi Thomas screening parameter and  $l_0$  is the length of the metal strand. The formation of such a metal strand of Au atoms in between the nanowires also cannot explain such a high dielectric constant ( $\epsilon \sim 1.8 \times 10^7$ ) as the above equation shows only  $\epsilon \sim 10^3$  considering a strand length equal to 5 nm (gap between the nanowires) and  $q_s^2 \sim 10^{20} \text{ m}^{-2}$ .

To explain the observed ultra high capacitance value in the present nanocapacitor, and the linear variation of conductivity with frequency, we have considered a simplified picture illustrated in figure 3(b). From the frequency dependent conductivity it is understood that the interfacial dielectric layer between the nanowires is a disordered phase containing Au atoms. Considering the simplest model of a flat surface ( $2 \mu\text{m} \times 10 \text{ nm}$ ) of two nanowires forming a parallel plate capacitor, the total number of surface atoms is calculated to be  $\sim 3.4 \times 10^5$ . Although, these Au atoms are distributed randomly in the interface, the average distance between the atoms is calculated to be  $\sim 6.5 \text{ \AA}$ . Therefore, we believe that the atoms are distributed randomly at the interface between the wires in which electrons hop between the atomic sites as is indicated by the ac conductivity data. The presence of these metal atoms creates a high density of states; as a result, the permittivity of the interface increases to a very high value ( $\epsilon \sim 1.8 \times 10^7$ ) as calculated from the measured capacitance. Considering the two-site approximation, the net polarization ( $P$ ) has been estimated to  $\sim 0.23 \text{ C m}^{-2}$ . The electric field ( $E$ ) required to create this sustained polarization is obtained by the formula  $P = \epsilon_0(\epsilon - 1)E$  as  $1.3 \times 10^3 \text{ V m}^{-1}$ , where

$\epsilon_0$  is the free space permittivity. This means that, under the application of a voltage  $\sim 6.5 \mu\text{V}$  (or equivalently  $6.5 \mu\text{eV}$  as the charging energy), which is much lower than the oscillatory level (10 mV) of the ac source used to measure the capacitance, the interface will be polarized due to the motion of electrons between the atomic sites to produce this ultra high capacitance.

It is noticed for the present devices that the interface is not stable under a bias of several volts. From  $I$ - $V$  characteristics measured from  $-5$  to  $5$  V (not shown in figure 2(a)), no regular feature is observed. Rather, the current fluctuates randomly between very high and low conducting states. This is also consistent with the existence of metal atoms in the interface; in the high field region the metal atoms form connecting paths between the electrodes to allow a high current, followed by a low conducting state with the disruption of the filament due to heating effects when high current flows. This kind of filamentary growth (switching) and disruption of metal particulates in the high field region is a common feature as observed by many researchers [9, 17].

Another interesting feature is that the capacitance is higher when the loss factor is lower and vice versa. For example, device 1 shows capacitance 718 pF and loss 0.7, whereas for device 2 the corresponding quantities are 60 pF and 10. This is due to the fact that a fraction of the atoms (which do not participate in the ac conduction) in the interface form a leakage path from one electrode to the other. As a result, the loss factor increases with decreasing capacitance.

In conclusion, by using the novel properties of ultra fine particles it is possible to fabricate nanodielectrics with giant permittivity values between two metal nanoelectrodes to form a nanocapacitor with ultra high capacitance. We believe the loss factor can be controlled by tailoring the thickness and number of atoms present in the interface. The resulting

nanocapacitors could have applications in energy storage, ultrasensitive transducers in nanoelectronic circuits, and also as high K materials in transistors.

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