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High Performance Inversion-type InGaAs MOSFET with ALD High-*k* Gate Dielectric

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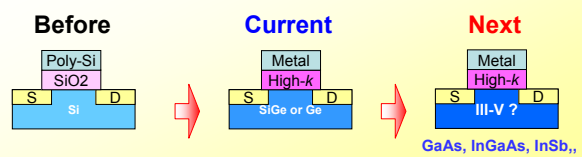
1 Introduction

The silicon based complementary metal-oxide-semiconductor (CMOS) technology now faces ever shrinking device dimensions and demands for higher performance. The latest advance in CMOS industry suggests that ALD high-k dielectrics developed for silicon may pave the way for novel channel materials in future CMOS integrated circuits. In this work, high performance inversion-type enhancement mode InGaAs MOSFET with *ex situ* ALD gate dielectric and 0.5 micron gate length is demonstrated for the first time with maximum drain current of 367mA/mm and extrinsic transconductance of 130mS/mm.

CMOS Evolution

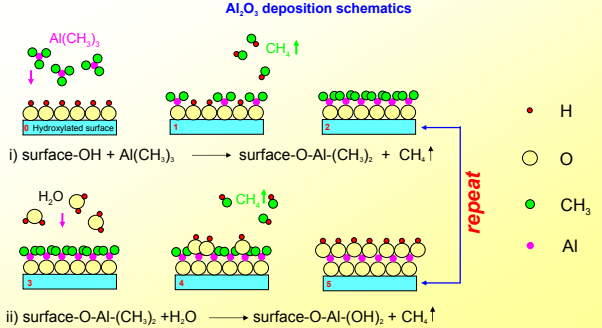


Gate Oxide: SiO_2 → high-*k* (high permittivity) (Al_2O_3, HfO_2, HfSiON, La_2O_3, $LaAlO_3$….)
Channel: Si → high mobility (SiGe, Ge, **GaAs, InGaAs, InSb**, CNT, Graphene..)

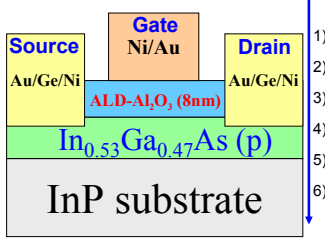
Atomic Layer Deposition (ALD) is a self-limiting, sequential surface chemistry that deposits conformal thin-films of materials onto substrates of varying compositions. ALD process generally consists of two half reaction: i) adsorption of metal-organic precursor molecules on the surface and ii) reaction of the adsorbed species with oxygen-containing species such as H_2O, O_2 and O_3.

Atomic Layer Deposition (ALD)

Al_2O_3 deposition schematics



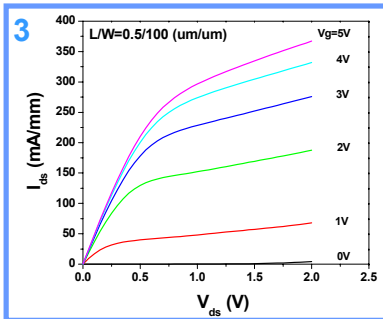
2 Device cross section



Process Flow

1) ALD Al_2O_3 deposition (passivation layer)
2) S/D patterning and Si implantation
3) S/D dopant activation (700~850 °C)
4) Re-growth of ALD 8nm-Al_2O_3 gate oxide
5) S/D contact metallization
6) Gate patterning and Ni/Au evaporation

3



Drain current versus drain voltage at different gate bias for a 0.5 μm gate length n-MOSFET with 8nm ALD Al_2O_3 gate dielectric.

•Maximum drain current: 367mA/mm

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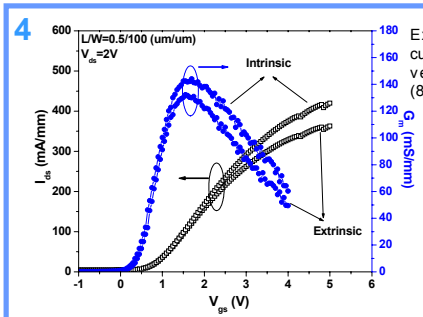

Extrinsic and intrinsic drain current and transconductance G_m versus gate bias for Al_2O_3 (8nm)/$In_{0.53}Ga_{0.47}As$ n-MOSFET.

• Extrinsic G_m: 130 mS/mm

• Intrinsic G_m: 145 mS/mm

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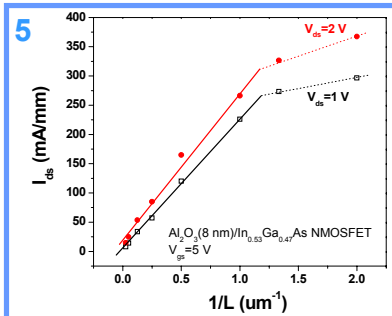
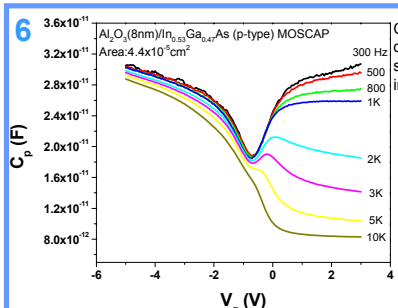


Drain current versus gate length (1/L) at different drain voltages for Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$ n-MOSFET.

• The drain current scales linearly with 1/L as expected and begins to saturate at L=0.75 μm.

6

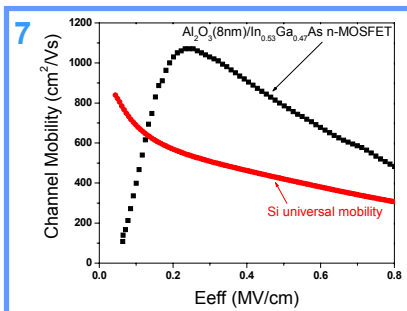


Capacitance-Voltage characteristics of an Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$ MOS structure at multiple frequency in dark.

• Full inversion observed at 300Hz

• Mid-gap D_{it}: ~2 x10^{12}/cm^2

7



$In_{0.53}Ga_{0.47}As$ n-MOSFET channel mobility versus effective normal field compared with Si universal mobility.

• Peak mobility: 1100 cm^2 /Vs

• Twice of Si universal mobility at 0.5 MV/cm.