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Inversion-type enhancement-mode InP MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO nanolaminates as high-k gate dielectrics

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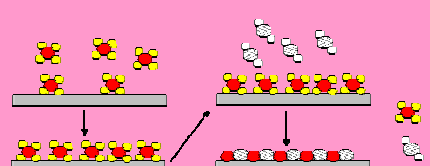
Introduction of atomic layer deposition high-k dielectric on III-V MOSFET

As the Moore's Law push device scaling to a fundamental physical limit, alternatives have been attempted to explore the "*Plenty of Room at the Bottom* ". Chip giant Intel and IBM announced the high-k dielectric with metal gate technology on their 45-nm node generation using ALD—" *The implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s*"—By Gordon Moore

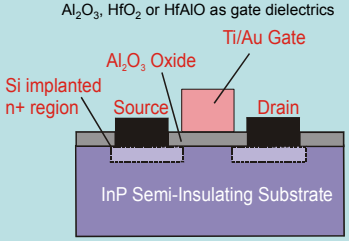
That's the somehow give people the motivation to pursue the similar concept : ALD high-k dielectric on III-V compound semiconductor MOSFETs, which have higher mobility than Silicon, probably a suitable candidate of further generations.

ALD process flow



- ALD is short for atomic layer deposition
- Is a surface-limiting process
- Grow thin film layer by layer
- Very uniform and precisely thickness control

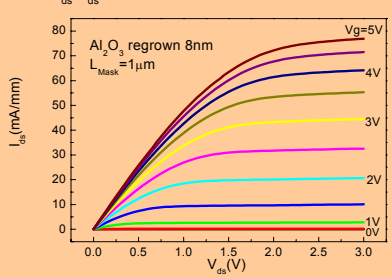
Schematic view of an E-mode n-channel InP MOSFET with ALD Al_2O_3, HfO_2 or HfAlO as gate dielectrics



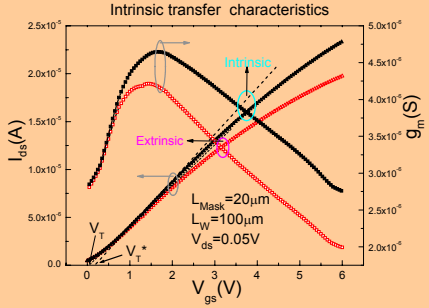
Fabrication process flow for E-mode high-k/InP MOSFETs

- Surface clean and pretreatment $(NH_4)_2S$
- Deposition of 30nm Al_2O_3 using ALD
- Ion Implantation (Si 35Kev, $1\times10^{14}/cm^2$)
- Activation using RTA 720℃ 10sec
- For regrowth oxide, etch away oxide using BHF and regrow 8nm Al_2O_3 and PDA
- S/D region patterning and metal deposition AuGe/Ni/Au and RTA
- Gate region patterning and metal deposition Ni/Au

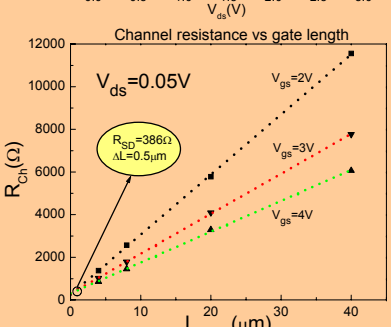
I_{ds}-V_{ds} Characteristics of n-channel InP MOSFET



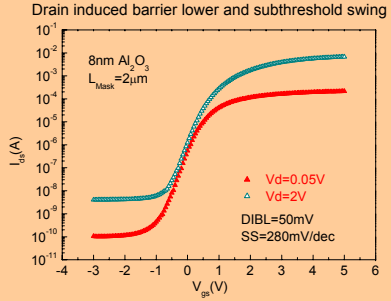
Intrinsic transfer characteristics



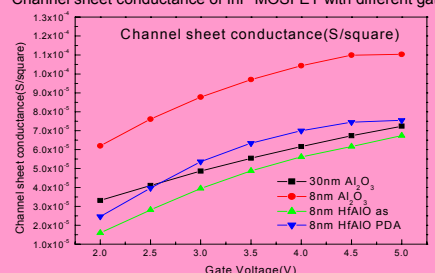
Channel resistance vs gate length



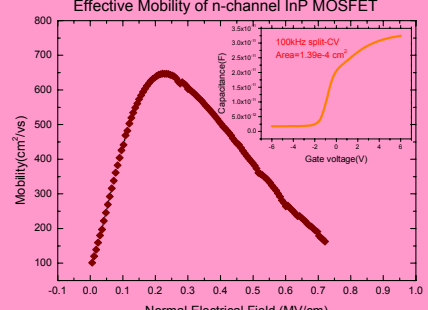
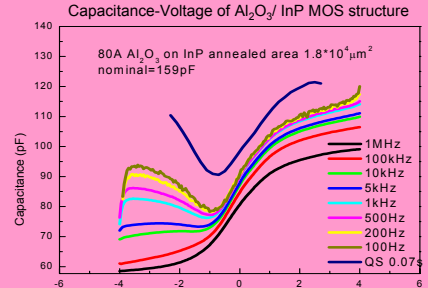
Drain induced barrier lower and subthreshold swing



Channel sheet conductance of InP MOSFET with different gate stack



Effective Mobility of n-channel InP MOSFET



Capacitance-Voltage of Al_2O_3/ InP MOS structure