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Myeong-Enn Hwang

Kaushik Roy

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A 135mV 0.13µW Process Tolerant 6T Subthreshold DTMOS SRAM in 90nm Technology

Myeong-Eun Hwang and Kaushik Roy Purdue University, West Lafayette, IN 47907, USA

Abstract

Cell stability and tolerance to process variation are of primary importance in subthreshold SRAMs. We propose a DTMOS based 6T SRAM suitable for subthreshold operation. For variation tolerant memory peripheral circuitry, we apply β -ratio modulation technique. DTMOS SRAM array fabricated in 90nm technology operates down to 135mV consuming 0.13 μ W at 750Hz. The proposed SRAM achieves 200% improvement in read static noise margin at iso-area compared to the conventional 6T SRAM at a supply voltage of 200mV.

Introduction

Efficient power management is becoming increasingly important with the rapid growth of portable, wireless, and battery-operated applications, such as laptop computers, personal digital assistants (PDAs), and portable communication devices. One of the promising approaches to achieve ultralow power dissipation in such applications is to use subthreshold (sub-V_T) logic [1][2]. In sub-V_T logic, circuits operate with a supply voltage (V_{dd}) lower than the transistor threshold voltage (V_{T}) and utilize the subthreshold leakage current as the operating current.

Lowering the supply voltage reduces the dynamic power quadratically and leakage power exponentially. However, supply voltage scaling also limits signal swing and thus reduces noise margin. Further, aggressive technology scaling in the sub-100nm region increases the sensitivity of the circuit electrical parameters to process variation (PV) [3][4]. This may result in device mismatch between the adjacent transistors and limits the circuit operation in the sub-V_T region, particularly for memories [5]. Embedded cache memories are expected to occupy 90% of the total die area of a system-on-a-chip [6]. Nano-scaled SRAM cells having minimum-sized transistors are vulnerable to inter-die as well as intra-die PVs. In addition to PVs, such as random fluctuations in electrical circuit parameters, low voltage operation results in reduced noise margin and various memory failures, such as read/hold/access/writes failure [7]. This seriously degrades robustness in sub-V_T memory systems.

For robust sub-V $_T$ SRAMs, various types of SRAMs have been proposed (Fig. 1). To maintain the clarity of the discussion, the conventional 6 transistor CMOS cell is referred to as "6T", and the 5, 7, 8 and 10 transistor SRAM cells are referred to as the 5T [8], 7T [9], 8T [10 and 10T [11], respectively. Adaptive circuit techniques such as source biasing, dynamic V_{dd} have been also proposed to improve PV tolerance [12]. The authors in [13] used reverse short-channel effect to improve writability and to decrease circuit variability. While 5T, 8T, and 10T cells employ single ended reading 6T and 7T cells utilize differential read operation. 8T and 10T cells use an extra sensing circuit for reading the cell contents, achieving improved read SNM. Recently, a memory cell operating at the supply voltage of 103mV has been reported with single ended read operation [14].

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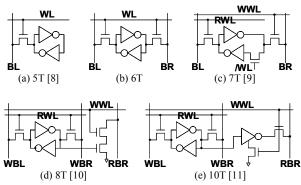


Fig. 1. Various SRAM cells.

This paper describes a dynamic threshold MOS (DTMOS) based 6T SRAM suitable for robust sub- V_T operations using positive feedback in the cells and body biasing in peripherals. The proposed SRAM requires no architectural change compared to the conventional 6T SRAM. Some highlights of our design are:

- Considerable improvement in read and hold stabilities for sub-V_T operation;
- Full functionality at low voltages, all the way to 135mV;
- Variation tolerant peripheral circuitry for sub-V_T memory.

DTMOS Technique

Fig. 2(a) shows a basic DTMOS inverter where the gate and the body of the transistor are tied together. Because of body effect, the threshold voltage (V_T) of the device changes dynamically based on input data. When the input 'in' is LOW, PMOS is ON with low- V_T and NMOS is OFF with normal- V_T (high- V_T). When 'in' is HIGH, the situation is the opposite. In other words, during the ON state, DTMOS scheme lowers V_T , increasing the overdrive voltage (V_{gs} – V_T).

Fig. 2(b) compares the subthreshold current-voltage characteristic $(I_d\hbox{-} V_{gs})$ of DTMOS and standard CMOS transistors obtained from HSPICE simulations at $V_{dd}\hbox{=}300mV$ in 90nm technology. During the OFF state, DTMOS scheme raises V_T , decreasing the leakage current. As a result, the trip voltage (V_M) of the DTMOS inverter increases or decreases depending on the direction of input transition. In the active mode, the inverter switches from LOW to HIGH with a higher speed because of the low- V_T PMOS. In the standby mode, the static leakage current is determined by the subthreshold current of the high- V_T NMOS.

In sub-V $_T$ DTMOS, the body terminal provides the additional transconductance $(g_{mb}=\delta I_d/\delta V_{bs})$, resulting in higher operational current through the device. This improves voltage transfer characteristics (VTC) of sub-V $_T$ DTMOS inverter as shown in Fig. 2(c), where we refer to the full (PMOS-only) DTMOS scheme as "DT" ("pDT") and the conventional CMOS scheme as "CMOS".

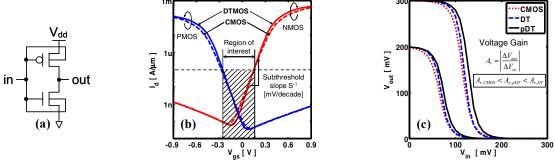


Fig. 2. DTMOS inverter. (a) Schematic, (b) I_d - V_{gs} curve and (c) VTC (simulation in 90nm technology). CMOS stands for the conventional CMOS scheme. "DT" means DTMOS scheme applied to both PMOS and NMOS transistors and "pDT" means DTMOS scheme applied to the PMOS transistor only.

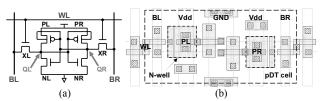


Fig. 3. Proposed 6T pDT SRAM cell. (a) Schematic. (b) Layout.

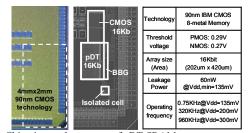


Fig. 4. Chip view and summary of pDT SRAM measurements.

The improved VTC results in an improved noise margin and tolerance to process variation. Note that the voltage gain (Av) of an inverter is the product of the transconductance and output resistance.

Proposed 6T DTMOS-based SRAM

Fig. 3(a) shows the proposed pDT 6T cell. At low V_{dd} 's, degradation in the gain of the cross-coupled inverter is of concern. To improve the inverter characteristics, DTMOS scheme is used. Transistors PL-NL form one pDT inverter while PR-NR form the other inverter. XL and XR are the access transistors. Positive feedback from the pDT inverter changes the inverter trip voltage dynamically depending on the direction of state transition. This gives a near ideal inverter characteristics in the cell essential for robust memory operation. The pDT cell utilizes differential operation, giving better noise immunity. Fig. 3(b) shows one possible layout of the pDT cell. Due to separation of body contacts for PMOS devices, the pDT cell requires 78% larger area than the standard CMOS cell in 90nm process.

Fig. 4 shows the test chip view and summary of the 16Kb pDT SRAM fabricated in 90nm CMOS memory technology. To measure the static noise margin of pDT and conventional SRAMs, their isolated cells are implemented with direct probing capability. Fig. 5 illustrates the architecture of pDT SRAM operating with one single supply voltage. DTMOS scheme (pDT) is used to the core array to increase cell sta-

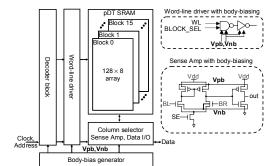


Fig. 5. pDT SRAM. Four columns share one sense amplifier.

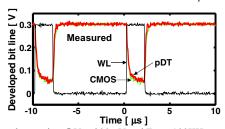


Fig. 6. Read operation @V_{dd}=300mV and Freq=100KHz.

bilities while body bias is applied to the peripheral circuits to improve variation tolerance in logic. The body bias generator (BBG) provides body bias voltages to the transistors in peripheral circuits (V_{pb} and V_{nb} for the pull-up and the pull-down networks, respectively).

Memory Operations

During a read operation (with QL=0 and QR=1 say), the voltage of the node QL rises due to voltage division between the access transistor XL and the pull-down transistor NL. If this voltage is greater than the trip voltage of the other inverter PR-NR, the content of the cell can get flipped resulting in a read failure. To avoid a read failure, it is necessary to increase the trip voltage of the inverter PR-NR. In a pDT cell, Transistors PR and NR have lower-V_T and higher-V_T, respectively, and thus increase the trip voltage of the inverter which is storing HIGH. DTMOS action helps preserve the logic '1' value of the cell. During a read operation with QL/QR=1/0, the situation is the opposite and DTMOS action helps preserve the logic '0'. Fig. 6 shows the waveforms when the bit-line is discharged during a read operation at $V_{\rm dd}=300 {\rm mV}.$

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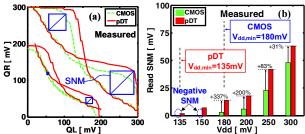


Fig. 7. Read SNM. (a) V_{dd} =300mV and 200mV. (b) The average of 32 measured data.

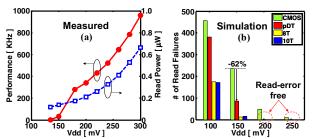


Fig. 8. Read operation. (a) Performance and power in pDT SRAM. (b) Read failure.

Fig. 7(a) shows the read static noise margin (SNM) of the pDT cell and its conventional counterpart (referred to as CMOS) measured at low V_{dd} 's. Fig. 7(b) shows the average SNM computed out of 32 measured data samples. The cell has two cross-coupled pDT inverters. pDT scheme augments the PMOS transistor (i.e., lowering PMOS V_T) and thus makes one inverter hold '1' stronger. This restrains the other inverter (involved in discharging) from flipping the cell value. As a result, the pDT cell improves the read SNM by 31% (200%) at V_{dd} =300mV (200mV) compared to the conventional cell and the degree of improvement in read SNM is considerable as V_{dd} is lowered. pDT SRAM shows correct functionality at a minimum V_{dd} of 135mV, read power of 0.13uW, and frequency of 750Hz.

One may consider upsizing would improve the read SNM in the conventional cell. At high V_{dd} 's (i.e., super- V_{T} region), the drain current varies linearly with the gate voltage. Transistor sizing increases the SNM considerably. However in the sub- V_{T} region, the drain current depends exponentially on the gate voltage. Any device upsizing will result in marginal change in the drain current. Thus in the sub- V_{T} region, SNM is relatively independent of device sizing [7]. For example, compared to the '5X-increased' conventional cell, the proposed 'minimum sized' pDT cell shows 160% improvement in read SNM at $V_{dd}\!=\!200\text{mV}$. This means that for a stable SRAM cell operating in the sub- V_{T} region, DTMOS technique can be more efficient than simple transistor upsizing in the conventional 6T cell.

Fig. 8(a) shows performance and power consumption during read operations in pDT SRAM. The minimum supply voltage of 135mV in the pDT SRAM provides a wider range of operable supply voltage whereas the conventional SRAM fails to operate below 180mV.

Fig. 8(b) shows the read failure obtained from 1000 Monte-Carlo simulations at iso-area condition in the sub- $V_{\rm T}$

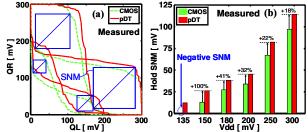


Fig. 9. Hold SNM. (a) $V_{\text{dd}}\!\!=\!\!300\text{mV}$ and 200mV. (b) The average of 32 measured data.

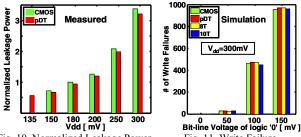


Fig. 10. Normalized Leakage Power in hold mode.

Fig. 11. Write Failure.

region. pDT SRAM exhibits 62% improvement compared to the conventional SRAM at 150mV (the measured minimum supply voltage was 180mV). To achieve iso-read error probability with pDT SRAM (V_{dd}=200mV), conventional SRAM requires the supply voltage of 330mV. Note that at a supply voltage of >200mV, pDT SRAM provides read-error free operation as do 8T and 10T SRAMs.

In the standby mode, supply voltage can be lowered to save leakage power and SRAMs enter the hold state while preserving the cell values. Hold SNM measured at low $V_{\rm dd}$'s is shown in Fig. 9(a). The improved VTC in a pDT inverter pair also increases the cell stability, introducing 18% (32%) improvement in hold SNM over the CMOS cell at 300mV (200mV) as shown in Fig. 9(b). Higher hold SNM clearly increases immunity to bit-line disturbance from environmental noise. Further, higher hold SNM provides more room for $V_{\rm dd}$ scaling, therefore, reduction in leakage power. Normalized leakage power of the pDT and the CMOS SRAMs measured during hold operations is shown in Fig. 10.

Write operation is performed externally to the cell and its analysis is important from environmental noise point view. Fig. 11 shows the write failure at iso-area. 1000 Monte-Carlo simulations have been performed at V_{dd} =300mV and various voltages of a bit-line holding '0'. pDT SRAM shows comparable write failure with other SRAMs.

BBG for Variation-Tolerant Peripheral Circuits

Variation tolerant peripherals are also essential for robust sub- V_T memory operations since noise margin is seriously limited in the sub- V_T region. The relative strength of PMOS and NMOS transistors changes due to process variation. If the β -ratio (pull-up to pull-down ratio) between PMOS and NMOS transistors is correctly chosen, the gate trip voltage (V_M) can be $0.5V_{dd}$, allowing maximum noise margin for peripheral circuits. The β -ratio given by β = W_p/W_n needs to be designed such that β × $I_{sub,p}/I_{sub,n}$ is close to unity where

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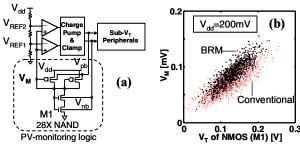


Fig. 12. BBG for subthreshold peripherals with β -ratio modulation. (a) Schematic. (b) Distributions of NAND trip voltage V_M and NMOS V_T at V_{dd} =200mV (simulation).

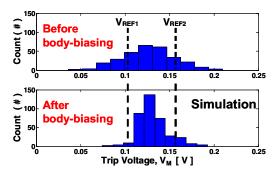


Fig. 13. V_M distribution before and after body biasing.

 $I_{\text{sub},p/n}$ is the PMOS/NMOS subthreshold current. This guarantees equal strength of the pull-up network and the pull-down network, which in turn reduces short circuit power and the impact of process variation (PV). However, the ratio of $I_{\text{sub},p}/I_{\text{sub},n}$ exponentially depends on V_T fluctuation and thus the impact of PV is more serious in the sub- V_T region.

In this work we use body biasing (BB) as a method to compensate device mismatches and to maximize circuit robustness under PV [4]. Note that body biasing is more effective in the sub-V_T region, since a little change in the bias can affect current in an exponential way. Fig. 12(a) shows the implemented body bias generator (BBG) that supplies BB voltages for the peripherals and performs adaptive β-ratio modulation (BRM). The NAND $V_{\rm M}$ in PV-monitoring logic is compared against two reference potentials of V_{REF1} and V_{REF2}. If V_M is below a predetermined reference potential (V_{REF1}), indicating that the pull-up network (PUN) is stronger than the pull-down network (PDN), we apply forward BB to the PUN to make the PUN and the PDN equally strong. If V_M is above V_{REF2}, the PDN is forward body biased. The generated body biases are again fed to the NAND gate, and the updated V_M is compared against the reverence voltages. Under PV, any mismatch between the PUN and the PDN leads to skewed NAND VTCs. 1000 Monte-Carlo simulations are done and the distributions of NAND V_M and its NMOS V_T at V_{dd} =200mV are plotted in Fig. 12(b). Fig. 13 illustrates other Monte-Carlo simulations of V_M before and after applying BB. Note that the application of BB can successfully change the relative strength of two networks and reduce the spread of both V_{M} and V_{T} , leading to increased robustness in sub-V_T peripheral circuits. This illustrates the effectiveness of β-ratio modulation (BRM) technique for sub-V_T operations.

To avoid failure due to N/P mismatches in the sub- V_T region it is essential to modulate the β -ratio adaptively such that V_M is close to $0.5V_{dd}$. BBG equalizes the transistors in strength and shifts V_M to $0.5V_{dd}$ while narrowing variability ($\sim \sigma/\mu$) in V_M distribution. Note that the circuit performance is also maximized when the PMOS and NMOS are of equal strength, i.e., V_M =0.5 V_{dd} . Hence, for both maximum performance and correct functionality under PV, we need to achieve the proper β -ratio in sub- V_T memory peripherals. Impact of PV in BBG can be reduced by increasing the size of PV-monitoring logic (e.g., 28X NAND in Fig. 12(a)).

Conclusions

This paper proposes a DTMOS based 6T SRAM suitable for sub- V_T operation. Cell stability and variation resilience are most important in sub- V_T SRAMs. Positive feedback mechanism in the cross-coupled DTMOS inverters in the cell provides considerable improvement in stability at the expense of area whereas, just increasing size of the cell does not improve cell stability. To increase tolerance to process variation in memory peripherals, we used body bias technique, adaptively adjusting the relative strength between pull-up and pull-down networks. Measurements from a test chip fabricated in 90nm technology confirm the validity of the proposed SRAM for robust sub- V_T operation. Our 16Kb DTMOS SRAM achieves 200% (32%) improvement in read (hold) stability at a supply voltage of 200mV and operates down to 135m, consuming 0.13uW at a frequency of 750Hz.

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