

9-1-2004

# Frequency response of top-gated carbon nanotube field-effect transistors

Dinkar V. Singh

Keith A. Jenkins

Joerg Appenzeller

*Birck Nanotechnology Center, Purdue University, appenzeller@purdue.edu*

D. Neumayer

Alfred Grill

*See next page for additional authors*

Follow this and additional works at: <http://docs.lib.purdue.edu/nanodocs>

---

Singh, Dinkar V.; Jenkins, Keith A.; Appenzeller, Joerg; Neumayer, D.; Grill, Alfred; and Wong, H.S. Philip, "Frequency response of top-gated carbon nanotube field-effect transistors" (2004). *Other Nanotechnology Publications*. Paper 9.  
<http://docs.lib.purdue.edu/nanodocs/9>

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact [epubs@purdue.edu](mailto:epubs@purdue.edu) for additional information.

---

**Authors**

Dinkar V. Singh, Keith A. Jenkins, Joerg Appenzeller, D. Neumayer, Alfred Grill, and H.S. Philip Wong

# Frequency Response of Top-Gated Carbon Nanotube Field-Effect Transistors

Dinkar V. Singh, Keith A. Jenkins, *Senior Member, IEEE*, J. Appenzeller, D. Neumayer, Alfred Grill, and H.-S. Philip Wong, *Fellow, IEEE*

**Abstract**—The ac performance of carbon nanotube field-effect transistors (CNFETs) has been characterized using two approaches involving: 1) time- and 2) frequency-domain measurements. A high input impedance measurement system was used to demonstrate time-domain switching of CNFETs at frequencies up to 100 kHz. The low level of signal crosstalk in CNFETs fabricated on quartz substrates enabled frequency-domain measurements of the ac response of CNFETs in the megahertz range, over five orders of magnitude higher in frequency than previously reported ac measurements of CNFET devices.

**Index Terms**—AC measurement, carbon nanotube (CN), high frequency.

## I. INTRODUCTION

RECENT progress in engineering carbon nanotube field-effect transistors (CNFETs) has resulted in CNFETs with excellent dc characteristics [1], [2], making them promising candidates for future nanoelectronics technologies. The excellent transport properties in carbon nanotubes (CNs), attributed in part to the suppressed carrier scattering rates in one-dimensional (1-D) systems results in high mobilities and long scattering lengths (on the order of several micrometers) [3]–[5]. Additionally, identical energy dispersion curves for the conduction and valence bands imply similar electron and hole effective masses and results in high performance for both n- and p-type CNFETs [6]. This is an advantage over conventional CMOS where the higher effective mass of holes compared to electrons degrades p-MOSFET performance compared to n-MOSFETs. However, despite the tremendous interest in CNFET devices for future circuit applications, there has been no direct demonstration that they operate at frequencies in excess of a few hundred hertz [7]. It is, therefore, vital to experimentally demonstrate high switching speeds in CNFETs.

The measurement of the frequency response of such narrow-width devices cannot use conventional methods. *S*-parameter measurements with a network analyzer are not possible because the parasitic probe pad capacitance is much larger than the intrinsic device capacitance and because of the small magnitude of the signal generated by a single-tube CNFET in a 50- $\Omega$  instrument. Since *S*-parameter measurements use the small-signal swing, the measured signal is too small even for CNFETs with maximum drain currents of the order of 10  $\mu$ A. Similarly, transit time measurements with a high bandwidth system [8] are not

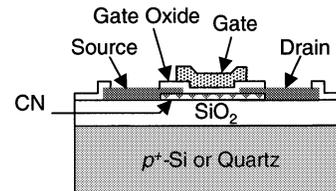


Fig. 1. Schematic device cross section of a top-gated CNFET used in this study.

possible because the signal is far below the measurement noise of oscilloscopes. Traditional circuits such as ring oscillators are difficult to fabricate due to the inability to place nanotubes at specific locations and orientations. In order to circumvent these problems, two different approaches were adopted, which are: 1) time-domain measurements using a high-impedance measurement system, which allows the measurement of small currents, but limits the bandwidth and 2) large-signal frequency-domain measurements using a spectrum analyzer. This study represents the first *direct* ac measurements of CNFET operation at frequencies as high as 100 MHz [9]. The methodology described in this paper is generally applicable to molecular transistors and nanowire transistors [10] where the individual conducting channel (e.g., a molecule) has a small conductance.

## II. DEVICE FABRICATION

CNFETs were fabricated on substrates comprising: 1) thick 100-nm  $\text{SiO}_2/\text{p}^+\text{-Si}$  and 2) quartz. CNs grown by laser ablation [11] were dispersed from a 1,2-dichloroethane solution by spinning onto the substrate. An atomic force microscopy image confirmed the presence of well-dispersed single-wall CNs, as well as small bundles of tubes. Ti source–drain contact pads with a spacing of 300 nm were then defined by electron beam lithography and liftoff. The top gate dielectric comprising 10 nm of  $\text{SiO}_2$  was deposited by low pressure chemical vapor deposition at 300  $^\circ\text{C}$  prior to patterning Ti gate electrodes. Finally, vias were etched to contact the source and drain pads. Fig. 1 shows a schematic cross section of a CNFET after complete fabrication. The contact pads are compatible with microwave probe geometry.

Since CNFETs are Schottky-barrier field-effect transistors (FETs) [12], [13], it is essential to be able to effectively modulate the barrier profile at the CN–metal interface in order to turn the device *on*. To ensure strong modulation of the Schottky barrier at the metal–CN interface, the gate electrode overlaps the source–drain contact electrodes, as shown in Fig. 1. Note that these transistors work in the enhancement mode and cannot

Manuscript received October 30, 2003; revised March 14, 2004.

The authors are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: singhd@us.ibm.com).

Digital Object Identifier 10.1109/TNANO.2004.828577

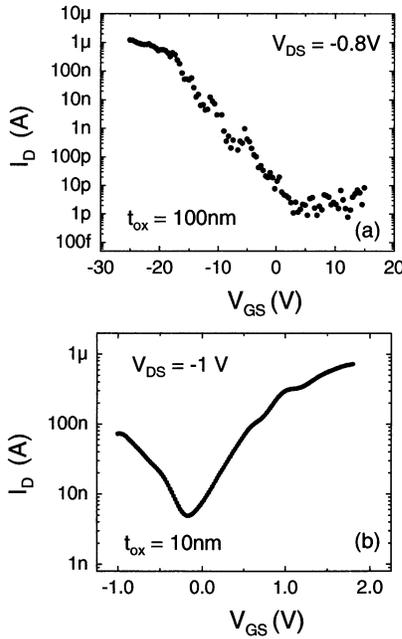


Fig. 2. Transfer characteristics of a CNFET measured after: (a) source–drain formation using the  $p^+$  substrate as a back gate and (b) complete fabrication using the top gate.

be operated without gate control in the contact area. In order to minimize parasitic capacitances associated with the gate–drain/gate–source overlap, e-beam lithography was used to define the gates, ensuring that the gate–source/gate–drain overlap was  $<50$  nm. In the case of the quartz substrates, a dual layer comprising 10-nm-thick aluminum on polymethyl-methacrylate (PMMA) resist was used to expose the features. The use of a thin Al layer on top of the PMMA resist layer minimizes the impact of substrate charging on e-beam lithography, which can be quite severe for insulating substrates such as quartz.

### III. TIME-DOMAIN MEASUREMENTS

#### A. DC Electrical Characterization

Time-domain measurements were performed on devices fabricated on substrates comprising 100 nm of  $\text{SiO}_2/p^+$  Si. During fabrication, dc electrical characterization of the CNFETs was performed subsequent to source–drain formation, utilizing the heavily doped substrate as a back gate. The back-gated CNFETs exhibited p-type characteristics, as shown in Fig. 2(a). It is evident from Fig. 2(a) that the tubes have high drive current and low *off* state currents. However, subsequent to forming the top-gated structures, the devices showed ambipolar characteristics [14] with larger drive currents for electron (compared to hole) injection, as shown in Fig. 2(b). The dc output characteristics of a typical top-gated CNFET after complete fabrication are shown in Fig. 3. The transformation from p-type to ambipolar characteristics indicates that Schottky barriers at the CN–metal interfaces strongly influence device operation. For a given band lineup at the metal–CN interface, bulk doping introduced into the tube during processing cannot explain the larger drive currents for electrons compared to holes. While bulk doping in the tube will strongly impact the device threshold voltage, the FET characteristics (n or p) are determined by the

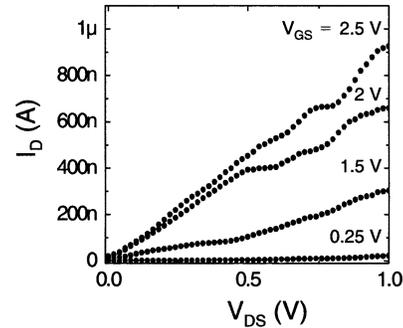


Fig. 3. Output characteristics of a top-gated CNFET operating as an *n*-FET.

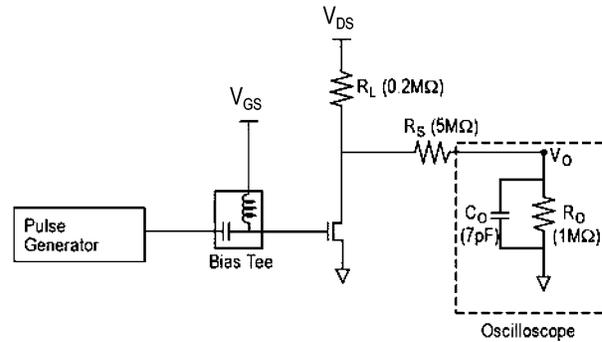


Fig. 4. Experimental setup used to measure the time-domain response of a CNFET.

relative heights of the Schottky barrier for electron and hole injection at the metal–CN interface [15]. The transformation of the CNFET from a p-CNFET to an ambipolar CNFET suggests a shift in the Fermi energy lineup at the source metal–CN interface from near the valence band edge toward the mid-gap. Such a Fermi-energy lineup results in near-symmetric Schottky barriers for electron and hole injection, resulting in ambipolar behavior and, in particular, for thin gate oxides in higher *off* state currents due to thinning of the barriers at the source and drain contacts [15]. The transformation of the CNFETs from p-type toward n-type behavior likely occurs during the deposition of the gate dielectric. Earlier studies involving back-gated CNFETs have shown that p-type devices get converted to n-type devices by annealing in vacuum, and subsequently revert first to ambipolar and then back to p-type devices upon exposure to oxygen [16]. It has been suggested that the concentration of oxygen on the surface determines the Schottky barrier height at the metal–CN interface. While this observed conversion from n-type to ambipolar FET behavior did not affect the experimental approach that we adopted for characterizing the ac performance of CNFETs, it confirms the importance of the Schottky barriers at the contacts on the operation of CNFETs.

#### B. Pulsed Measurements

The measurement setup used for performing the time-domain measurements is shown in Fig. 4. A pulse with a short rise time is applied to the gate of the device through a high-bandwidth 50- $\Omega$  transmission line. The rise time of the resulting output pulse measured on an oscilloscope is a measure of the bandwidth of the device. Owing to the low drive current in a CNFET, it is essential to optimize the input impedance of the measurement system

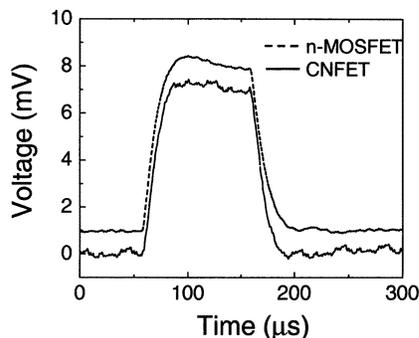


Fig. 5. Measured drain pulse in response to a gate pulse with a rise time of 10 ns using the experimental setup shown in Fig. 4. Applied  $V_{DS} = 1$  V,  $V_{GS} = 0$  V, and  $\Delta V_{GS} = 1.5$  V.

$R_s + R_o$ , as well as the load resistor  $R_L$  in order to generate an output signal that is above the noise threshold of the oscilloscope.  $R_o$  is the input resistance of the oscilloscope and  $R_s$  is an added series resistance. If  $R_s + R_o$  is too low, the apparent “off” current overwhelms the signal due to the CNFET. Here, the apparent “off” current refers to the current flowing through the input impedance of the measurement apparatus with the CNFET turned off, while the drain voltage remains on. The relative values of  $R_L$ ,  $R_s$ , and  $R_o$  must also be adjusted to ensure a signal that can be measured at the oscilloscope. In the measurement setup, the drain is loaded with an  $R_L = 200$  k $\Omega$  resistor to develop a significant voltage swing of 10–20 mV. The 1-M $\Omega$  oscilloscope input raises the apparent “off” current to approximately 1  $\mu$ A, thus, a 5-M $\Omega$  series resistor is used to reduce this current. This has the effect of attenuating the measured voltage swing, thus, the net signal is a few millivolts.

During the pulsed measurements, the CNFETs are biased at  $V_{DS} = 1$  V,  $V_{GS} = 0$  V, and the gate pulse amplitude  $\Delta V_{GS}$  is varied from 1.5 to 2.5 V. For sufficiently large  $V_{GS}$ , the drain current of the CNFET exceeds the apparent “off” current giving rise to a measurable voltage pulse across the load resistor  $R_L$ , as shown in Fig. 5. While the height of the voltage pulse measured across  $R_L$  varies with varying  $\Delta V_{GS}$ , the rise time is  $\sim 10 \pm 2$   $\mu$ s (100-kHz bandwidth) independent of the amplitude of  $\Delta V_{GS}$ . This represents the *highest* directly demonstrated switching speed for a CNFET. The bandwidth of the measurement system limits the rise time to 4  $\mu$ s. The somewhat larger rise time of the CNFET is attributed to the RC constant associated with the high on resistance  $R_{on}$  of the CNFET and the external capacitive load  $C_L$  due to the cable and oscilloscope. The pulse response of a conventional 150-GHz n-MOSFET for comparable drive currents (and comparable  $R_{on}$ ) attained by operating the MOSFET in sub-threshold is shown in Fig. 5. The nearly identical response of the MOSFET supports the idea that the measured rise time of the output pulse generated by the CNFET is limited by the combined effects of high  $R_{on}$  and the measurement setup.

#### IV. FREQUENCY-DOMAIN MEASUREMENTS

AC characterization of CNFETs at significantly higher frequencies is possible with a spectrum analyzer if the crosstalk between the gate and drain is sufficiently small. Fig. 6 shows

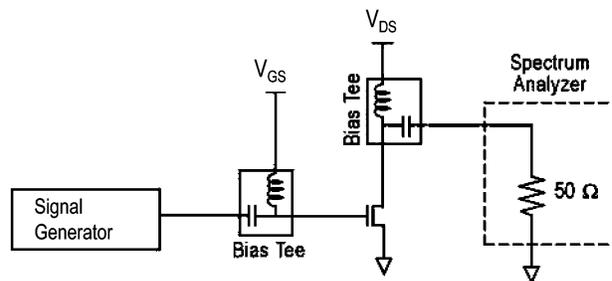


Fig. 6. Experimental setup used to measure the frequency response of CNFETs.

the apparatus used to measure the frequency response of a CNFET with a spectrum analyzer. DC biases of the CNFET gate and drain were provided with bias networks from 10-kHz to 10-GHz bandwidth. The gate was biased to operate at the midpoint of the drain current output and a signal generator was used to apply a large-signal sine wave. CNFET response was observed as a single frequency on the spectrum analyzer. The response of the device was measured as a function of frequency by varying the input frequency. Since the crosstalk signal increases with frequency, while the signal associated with the CNFET remains constant or rolls off with frequency, the measurement is ultimately limited by the ability to extract the CNFET signal from the crosstalk. Since the crosstalk arises primarily due to capacitive coupling, it is essential to minimize the capacitive path between the gate and drain. For devices fabricated on 100-nm SiO<sub>2</sub>/p<sup>+</sup> Si, there is a significant amount of crosstalk between electrodes due to coupling through the heavily doped Si substrate. The high level of crosstalk in these samples makes it very difficult to accurately extract the signal attributed to the CNFET.

In order to lower the crosstalk level, CNFETs were fabricated on a quartz substrate. The excellent insulating properties of quartz effectively removes the component of crosstalk arising from the coupling through the substrate and lowers the overall crosstalk level. The CNFETs fabricated on quartz substrates are enhancement mode devices exhibiting p-type characteristics. Estimates of the crosstalk power  $P_{CT}$  with the CNFET off and the total signal power  $P_{CT+CNFET}$  measured at the spectrum analyzer with the CNFET on are shown in Fig. 7(a). The calculations are based on the measured gate–drain capacitance, an applied peak–peak gate voltage of 0.6 V, and a CNFET current swing of 500 nA, consistent with the measured  $I_D - V_{GS}$  curves. For low frequencies up to a few megahertz,  $P_{CT+CNFET}$  far exceeds  $P_{CT}$ ; however, as the input frequency increases,  $P_{CT+CNFET}$  and  $P_{CT}$  asymptotically approach each other. The measured  $P_{CT}$  and  $P_{CT+CNFET}$  for the CNFETs fabricated on quartz are shown in Fig. 7(b). Measured  $P_{CT}$  on quartz is consistent with theoretical predictions and is sufficiently small to allow the extraction of the CNFET response by power subtraction up to approximately 100 MHz. Fig. 8 shows the extracted CNFET signal versus frequency for two different drain biases. The rms value measured by the spectrum analyzer was converted to peak-to-peak voltage for the data presented in Figs. 8 and 9. The extracted value of the CNFET signal at low frequencies is consistent with the measured dc  $I_D - V_{GS}$  characteristics;

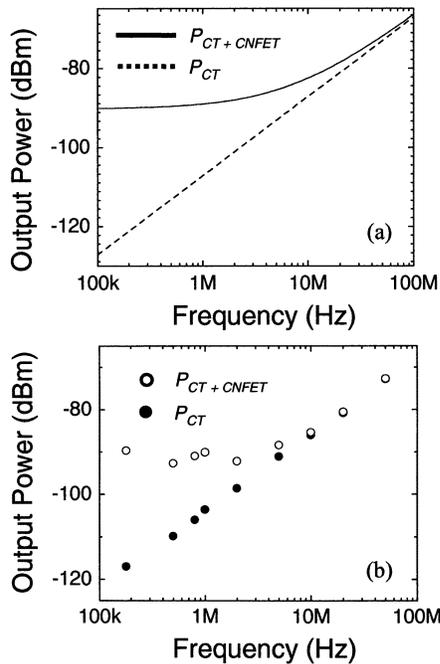


Fig. 7. (a) Calculated and (b) measured values of the crosstalk power  $P_{CT}$  and the total power  $P_{CT+CNFET}$  for CNFETs fabricated on quartz for  $V_{GS} = -1.2$  V,  $\Delta V_{GS} = \pm 0.3$  V, and  $V_{DS} = -1$  V.

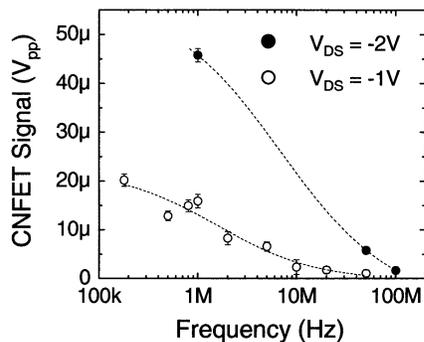


Fig. 8. Extracted CNFET signal versus frequency for two different drain biases.  $V_{GS} = -1.2$  V and  $\Delta V_{GS} = \pm 0.3$  V.

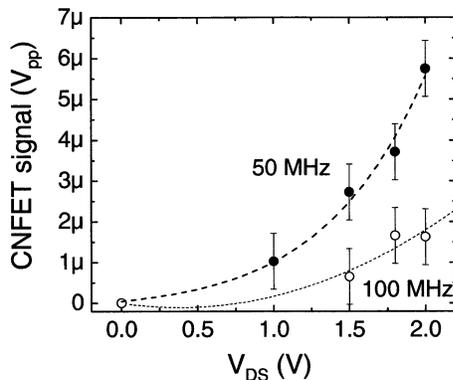


Fig. 9. Extracted CNFET signal versus  $V_{DS}$  for different input signal frequencies  $V_{GS} = -1.2$  V and  $\Delta V_{GS} = \pm 0.3$  V.

however, there is a distinct rolloff in the response versus frequency. While a response was observed even at 100 MHz, the extracted CNFET signal is reduced compared to its value at low frequencies. The observed rolloff is due to interference effects

arising from the phase difference between the capacitively coupled crosstalk and drain current of the CNFET, and is consistent with a flat current response in the frequency range measured. Fig. 9 shows the extracted CNFET signal versus  $V_{DS}$  at 50 and 100 MHz. An increase in the extracted ac CNFET signal versus  $V_{DS}$  is consistent with increasing  $I_D$  with drain bias. Since  $P_{CT}$  is independent of drain bias, this increase with drain bias confirms that the signal measured is due to the CNFET response at 100 MHz.

Thus, the ac performance of CNFETs has been studied using time- and frequency-domain measurements. Time-domain response is limited to 100 kHz by the RC time constant of the measurement system. Frequency-domain measurements have shown operation up to 100 MHz. This should be considered as the lower bound for the frequency response of the CNFET.

#### REFERENCES

- [1] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris, "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett.*, vol. 80, no. 20, pp. 3817–3819, 2002.
- [2] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. Dai, "High- $\kappa$  dielectrics for advanced carbon-nanotube transistors and logic gates," *Nature Mater.*, vol. 1, pp. 241–246, 2002.
- [3] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Brintlinger, "High-mobility nanotube transistor memory," *Nano Lett.*, vol. 2, pp. 755–759, 2002.
- [4] S. Wind, J. Appenzeller, and P. Avouris, "Lateral scaling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 91, p. 058 301/1–4, 2003.
- [5] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654–657, 2003.
- [6] M. Radosavljevic, J. Appenzeller, and P. Avouris, "High performance of potassium n-doped carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, 2003, submitted for publication.
- [7] A. Javey, Q. Wang, A. Ural, Y. Li, and H. Dai, "Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators," *Nano Lett.*, vol. 2, no. 9, pp. 929–932, 2002.
- [8] K. A. Jenkins and J. N. Burghartz, "Measurement of the switching speed of single FET's," *IEEE Trans. Electron Devices*, vol. 45, pp. 1369–1373, June 1998.
- [9] D. J. Frank and J. Appenzeller, "High frequency response in carbon nanotube field-effect transistors," *IEEE Electron Device Lett.*, vol. 25, pp. 34–36, Jan. 2004.
- [10] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, vol. 294, pp. 1313–1316, 2001.
- [11] A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. Xu, Y. H. Lee, S. G. Kim, A. G. Rinzler, D. T. Colbert, G. E. Scuseria, D. Tomanek, J. E. Fischer, and R. E. Smalley, "Crystalline ropes of metallic carbon nanotubes," *Science*, vol. 273, pp. 483–487, 1996.
- [12] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and P. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Phys. Rev. Lett.*, vol. 89, p. 126 801/1–4, 2002.
- [13] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon nanotubes as Schottky barrier transistors," *Phys. Rev. Lett.*, vol. 89, p. 106 801/1–4, 2002.
- [14] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersoff, and P. Avouris, "Ambipolar electrical transport in semiconducting single-wall carbon nanotubes," *Phys. Rev. Lett.*, vol. 87, no. 25, p. 256 805/1–4, 2001.
- [15] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. Wind, and P. Avouris, "Carbon nanotube electronics," *IEEE Trans. Nanotechnol.*, vol. 1, pp. 184–189, Dec. 2002.
- [16] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, "Controlling doping and carrier injection in carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 80, no. 15, pp. 2773–2775, 2002.



**Dinkar V. Singh** received the B.Tech. degree in engineering physics from the Indian Institute of Technology, Bombay, India, in 1995, and the M.S. and Ph.D. degrees in applied physics from Stanford University, Stanford, CA, in 1998 and 2001, respectively.

In 2001, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member. His current research interests include the study of Si-based heterostructure devices, new processes and materials for advanced device applications, and carbon-nanotube-based FETs.

Dr. Singh served on the International Technical Program Committee of the 1st and 2nd International SiGe Technology and Device Meetings.

**Keith A. Jenkins** (M'98–SM'98) received the Ph.D. degree (for experimental work in high-energy physics) in physics from Columbia University, New York, NY.

He is currently a Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he is a member of the Communications Technology Department. While with the IBM Research Division, he has performed research in a variety of device and circuit subjects, including high-frequency measurement techniques, electron beam circuit testing, radiation–device interactions, low-temperature electronics, and silicon-on-insulator (SOI) technology. His current activities include designing circuits for analog built-in self-tests, investigations into substrate coupling in mixed-signal and RF circuits, and studying the impact and mechanisms of self-heating in advanced CMOS technologies.



**J. Appenzeller** received the M.S. and Ph.D. degrees in physics from the Technical University of Aachen, Aachen, Germany, in 1991 and 1995, respectively. His doctoral dissertation concerned quantum transport phenomena in low-dimensional systems based on III/V heterostructures.

For one year, he was a Research Scientist with the Research Center, Juelich, Germany, prior to becoming an Assistant Professor with the Technical University of Aachen, in 1996. During his professorship, he explored mesoscopic electron transport

in different materials including CNs and superconductor/semiconductor-hybrid devices. From 1998 to 1999, he was a Visiting Scientist with the Massachusetts Institute of Technology (MIT), Cambridge, during which time he explored the ultimate scaling limits of silicon MOSFET devices. Since 2001, he has been with the IBM T. J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member, where he is mainly involved in the investigation of the potential of CNs for a future nanoelectronics.



**D. Neumayer** received the B.S. degree in chemistry/classics from Tufts University, Medford, MA, in 1986, and the Ph.D. degree in inorganic/materials chemistry from Northwestern University, Evanston, IL, in 1993.

Prior to attending graduate school, she was a Production Chemist involved with the synthesizing of radioactive nucleotides and nucleosides at DuPont and W. R. Grace and Company, where she developed new products and applications for vermiculite colloidal dispersions. While at Northwestern University,

she synthesized new chemical-vapor-deposition precursors for metal oxides and grew superconducting and insulating metal oxide films by chemical vapor deposition. Upon completion of the Ph.D. degree, she was a Post-Doctoral Associate with The University of Texas, where she synthesized new chemical-vapor-deposition precursors for growth of gallium nitride. In 1995, she joined the Electronic Materials and Structures Group, IBM T. J. Watson Research Center, Yorktown Heights, NY. While with the IBM T. J. Watson Research Center, she has specialized in chemical solution deposition and chemical vapor deposition of materials for use in microelectronic applications. She is interested in the transformation of chemical precursors into films and how the physical and electrical properties of the films are controlled by processing. She has authored or coauthored several dozen papers. She holds numerous patents.



**Alfred Grill** received the Ph.D. degree in physics from the Hebrew University, Jerusalem, Israel, in 1973.

In 1975, he joined the Materials Engineering Department, Ben-Gurion University, Be'er Sheva, Israel, where he was Head of the department for two terms and became a Full Professor in 1986. In 1989, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he is currently the Manager of the Electronic Materials—PECVD Dielectrics Group. This group develops and characterizes low and ultra-low dielectric-constant materials for interconnect dielectrics. His own expertise is in chemical vapor deposition and PECVD for deposition and treatment of materials. He developed the low-k SiCOH dielectrics and currently concentrates on development and improvement of ultra-low-k porous SiCOH. He also possesses extensive experience on diamond-like carbon films. He has authored or coauthored over 200 papers appearing in peer-reviewed journals. He authored *Cold Plasma in Materials Fabrication: From Fundamentals to Applications* (Piscataway, NJ: IEEE Press, 1994). He holds or co-holds 61 patents.

Dr. Grill is an active member of the Materials Research Society and the Electrochemical Society. He was the recipient of the 1992 IBM Outstanding Innovation Award for his work on carbon overcoats for the magnetoresistive head.



**H.-S. Philip Wong** (S'81–M'82–SM'95–F'01) received the Ph.D. degree in electrical engineering from Lehigh University, Bethlehem, PA, in 1988.

In 1988, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member. He is currently the Senior Manager of the Nanoscale Materials, Processes, and Devices Department, IBM T. J. Watson Research Center, where he is responsible for the shaping and implementing of IBM's strategy on nanoscale science and technology. Prior to this appointment, he was Senior Manager of

the Exploratory Devices and Integration Technology Department. His department was responsible for defining and executing IBM's exploratory devices and technology roadmap for silicon technology. While he has managed a wide range of technical activities from e-beam lithography, silicon materials and devices, molecular electronics and assemblies, nanotechnology, to quantum device modeling, he has maintained an active personal research career that centers on solid-state devices, device physics and fabrication technology, system applications of nanoelectronic and microelectronic devices, and solid-state image sensors. He has worked on charge-coupled devices (CCDs), CMOS image sensors, device modeling, double-gate FETs, strained Si CMOS, ultra-thin body silicon-on-insulator (SOI), device applications of wafer bonding, and most recently, Ge FETs, and CNFETs.

Dr. Wong serves on the IEEE Electron Devices Society (IEEE EDS) as an elected Administrative Committee (AdCom) member. He serves on the International Electron Devices Meeting (IEDM) Committee (1998–2004) and serves on the International Solid-State Circuits Conference (ISSCC) Program Committee (1998–2004). He is a Distinguished Lecturer of the IEEE EDS. He has taught several short courses at the IEDM, ISSCC, SOI Conference, and SPIE conferences. He is a member of the Emerging Research Devices Working Group, International Technology Roadmap for Semiconductors (ITRS).