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Templated Vertical Carbon Nanotube Transistors

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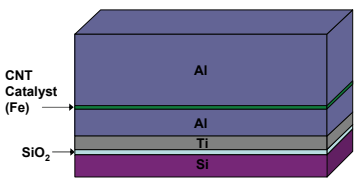
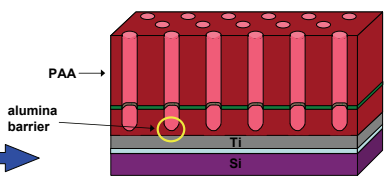
Abstract

Single-walled carbon nanotubes (CNTs) are a potential channel material for the next generation field-effect transistors (FETs). With properties such as quasi-ballistic transport and high thermal conductivity, CNTFETs have the ability to outperform Si MOSFETs. To date, all reported CNTFETs have been created in a planar geometry, with the CNT horizontal to the supporting substrate. While planar CNTFETs have provided an important platform for exploring device properties, they have yet to overcome the impending issues related to large-scale device fabrication. Obstacles such as precise placement, addressability, and high-density integration of CNTFETs can be overcome using a vertical device geometry. In the present work, vertical CNTs (v-CNTs) are synthesized within porous alumina templates and contacted *in situ* with vertical Pd nanowires. Semi-vertical CNTFETs are subsequently fabricated to provide a comparison of the vertical nanowire contact to a more conventional planar contact. Further fabrication work is also presented, displaying our progress towards fabricating addressable arrays of v-CNTFETs.

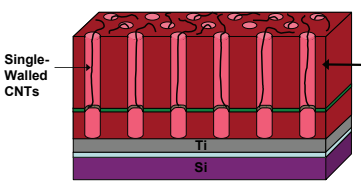
Synthesizing Vertical CNTs



(a) Ti/Al/Fe/Al films deposited onto supporting Si substrate.

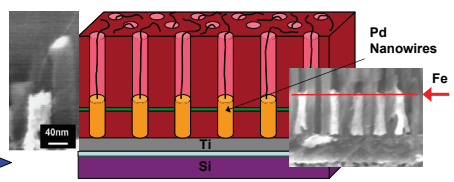


(b) Anodization in acid electrolyte to create porous anodic alumina (PAA) template.



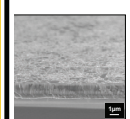
Vertical SWCNT channels of variable length (0.1—1μm)

(c) Single-walled CNTs grown vertically within pores by plasma enhanced CVD,[1] and alumina barrier penetrated by hydrogen plasma.[2]

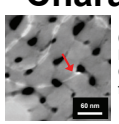


(d) Pd electrodeposited via underlying Ti layer to form vertical Pd nanowires that contact v-CNTs.[2,3]

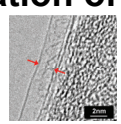
Characterization of CNTs



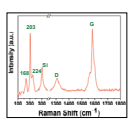
(a) Tilted cross-sectional FESEM showing CNTs on PAA surface.



(b) Top-view FESEM showing CNT emerging from a pore.

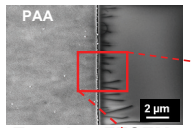


(c) TEM of individual single-walled CNT removed from PAA.[1]

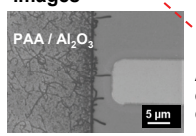


(d) Raman spectra (785 nm excitation) showing RBMs for single-walled CNTs from PAA.[3]

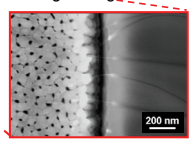
Semi-Vertical CNTFET



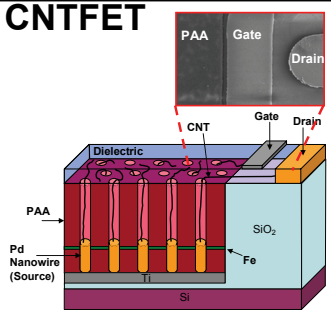
Top-view FESEM images



CNTs grow vertically within the porous channels and then extend horizontally onto a neighboring oxide.



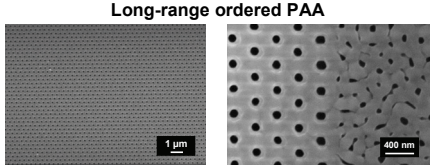
Al_2O_3 is deposited using atomic layer deposition (ALD) and the drain contact is created by etching the Al_2O_3.



The PAA/v-CNT structure is embedded within SiO_2 and semi-vertical CNTFETs are fabricated with a Pd nanowire source and planar Pd drain.

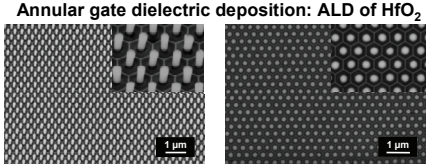
Progress towards Vertical CNTFET

Long-range ordered PAA



Addressability of v-CNTFETs will be achieved by creating PAA templates with long-range order.

Annular gate dielectric deposition: ALD of HfO_2

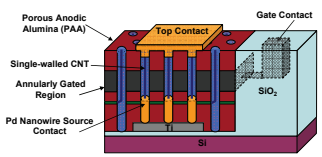


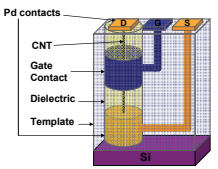
FESEM images of PAA pores filled with a silicate spin-on glass material that has been used as a placeholder for ALD of HfO_2. After filling, the PAA is selectively etched back.

Vertical CNTFET

Advantages of verticality:

- Packing density (up to 10^{10} pores/cm^2 in PAA)
- Controllable quasi-ballistic channel lengths
- Annular gate
  - Most effective gate geometry
  - Low-voltage operation
- Si-compatible processing
- Potential 3D integration





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[1] M.R. Maschmann, A.D. Franklin, P.B. Amama, D.N. Zakaharov, E.A. Stach, T.D. Sands, T.S. Fisher, *Nanotechnology* **2006**, *17*, 3925.

[2] A.D. Franklin, M.R. Maschmann, M. DaSilva, D.B. Janes, T.S. Fisher, T.D. Sands, *J. Vac. Sci. Technol. B* **2007**, *25*, 343.

[3] M.R. Maschmann, A.D. Franklin, A. Scott, D.B. Janes, T.D. Sands, T.S. Fisher, *Nano Lett.*, **2006**, *6*, 2712.

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