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## Ambipolar conduction in transistors using solution grown InAs nanowires with Cd doping

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Nanowire field effect transistors have been fabricated using Cd doped InAs nanowires synthesized using a solution-liquid-solid technique. Both *n*-channel and *p*-channel characteristics have been observed, which implies that the surface Fermi level is not pinned in the conduction band. The observation of a *p* channel is attributed to the passivation of surface states by surface ligands introduced during nanowire synthesis and to the effects of heavy acceptor doping. Devices in which the surface ligands are removed by O<sub>2</sub> plasma treatment exhibit only *n*-channel conduction, which would be consistent with surface Fermi level pinning in the conduction band. © 2007 American Institute of Physics. [DOI: 10.1063/1.2457249]

InAs is a direct, small band gap material (0.354 eV), which is potentially a good optoelectronic device candidate in the infrared range. InAs is also interesting for applications in high performance transistors, as well as applications utilizing the ferromagnetic properties that can be achieved in *p*-type InAs.<sup>1</sup> Electrical devices based on InAs nanowires have been reported by several groups,<sup>2-5</sup> however, most of these studies have concentrated on device behavior at low temperature with emphasis on single-electron transistors and supercurrent. As-produced InAs nanowires formed from chemical vapor deposition<sup>4</sup> or chemical beam epitaxy<sup>2,3,5</sup> exhibit only *n*-type conduction. In InAs thin films, it has been observed that the surface Fermi level is pinned in the conduction band regardless of the crystal orientation or dopant type.<sup>6-8</sup> This Fermi level pinning makes it relatively easy to form Ohmic contacts to InAs using a variety of contact metals. However, the pinning makes it difficult to achieve *p*-channel conduction in thin films or quasi-one-dimensional nanowires. It has been observed<sup>3</sup> that it is difficult to realize *p*-channel conductivity in InAs nanowires, possibly due to this Fermi level pinning. The availability of *p*-channel nanowire transistors would enable complementary circuits and many other interesting physical phenomena. In this letter, we report the development and characterization of field effect transistors (FETs) employing Cd doped InAs nanowires as channels, which show *n*- and *p*-channel operations.

The InAs nanowires were grown in polydecene from Bi nanoparticles at 325 °C by the solution-liquid-solid mechanism.<sup>9</sup> In(myristate)<sub>3</sub> (0.235 mmol) and As(SiMe<sub>3</sub>)<sub>3</sub> (0.158 mmol) were used as the In and As precursors, respectively. Cadmium tetradecylphosphonic acid (TDPA)

(0.086 mmol) was used as the Cd precursor. Cd was chosen as a dopant in order to achieve a Fermi level near the valence band so that *p*-channel conduction can be observed under moderate negative gate bias. Hexadecylamine (HDA) (1.28 mmol) and trioctylphosphine (0.226 mmol) were used as additional stabilizers. Transmission electron microscopy indicates an average diameter of 20 nm. Energy dispersive x-ray spectroscopy (EDS) on multiple nanowires shows Cd concentrations as high as 4% in the nanowires. Changes in EDS results following chemical ligand exchange experiments with either pyridine or oleic acid indicate that ~75% of the Cd is in the nanowire body and ~25% of the Cd is on or near the nanowire surface. The accumulation of Cd near the surface is also observed in x-ray photoelectron spectroscopy (XPS) measurements, which indicate an atomic ratio of Cd (3d) to In (3d) of ~25%. Powder x-ray diffraction pattern indicates that the nanowires maintain the zinc-blende crystal structure. The measured (theoretical<sup>10</sup>) *d*-plane spacings are  $d_{111}=3.5145$  (3.498) Å,  $d_{220}=2.1456$  (2.142) Å, and  $d_{311}=1.8282$  (1.826) Å, indicating that the lattice dimensions are the same as the bulk values within experimental uncertainty. Wires grow in the [111] direction as indicated by the selected-area electron diffraction pattern. Mass spectrometric analysis of the recovered ligands from nanowire surface indicates the presence of HDA and TDPA molecules on the surface with a molar ratio of 2:1. XPS also confirms the presence of surface ligands, exhibiting peaks for N and P, presumably from the HDA and TDPA, in addition to In and As peaks.

The initial substrate for single-nanowire FET fabrication consists of a heavily doped *p*-type Si substrate, which serves as a back gate, with a 40 nm thermal SiO<sub>2</sub> gate insulator and metal alignment marks for subsequent electron beam lithography (EBL). A suspension of the InAs nano-

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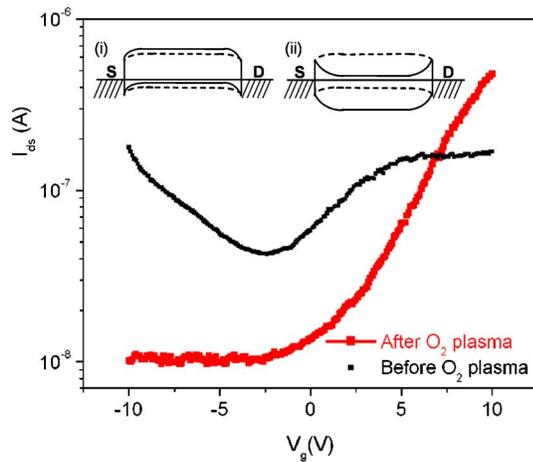


FIG. 1. (Color online) Electrical characteristics of a representative Cd doped InAs nanowire FET. The black curve shows ambipolar conduction of the Cd doped InAs nanowire before  $O_2$  plasma. The red curve shows  $n$  channel only conduction after  $O_2$  plasma. Insets depict band diagrams for InAs nanowire FET at  $V_{ds}=0$  V: (i) negative gate bias, corresponding to  $p$ -channel conduction (accumulation), and (ii) positive gate bias, corresponding to  $n$ -channel conduction (inversion). In each case, the zero-bias condition is illustrated by a dashed line.

wires in isopropanol and toluene is purified by several cycles of ultrasonication and centrifugation, then dropped onto the wafer, and the solvent is allowed to evaporate. Scanning electron microscopy imaging is performed to locate the nanowires relative to the alignment marks. EBL using polymethyl methacrylate (PMMA) resist is used to define openings for the source and drain contacts. The samples were then exposed to  $O_2$  plasma cleaning (15 s at a pressure of 1 torr, a plasma power of 100 W at an  $O_2/Ar$  ratio of 20%) followed by immersion in dilute buffered HF (BHF) (1:1, de-ionized water: BHF) in order to strip the residual PMMA from the source/drain contact areas. The source/drain contacts were formed by electron beam evaporation of Ni and Au, followed by lift-off patterning. Based on its work function (5.15 eV), Ni should provide a relatively small barrier to the valence band of InAs, which has an electron affinity of 4.9 eV, and the band gap mentioned previously.

Room temperature and variable temperature electrical measurements were performed on a HP 4156A semiconductor parameter analyzer and a Keithley 4200 semiconductor characterization system, respectively. The transfer characteristics ( $I_{ds}$  vs  $V_g$  at  $V_{ds}=1$  V) of a representative Cd doped InAs FET are shown in Fig. 1, with the black curve corresponding to the “as-fabricated” device and the red curve to the same FET following  $O_2$  plasma treatment, which will be discussed later. The as-fabricated device shows ambipolar conduction, with positive gate voltage inducing an electron ( $n$ ) channel and negative voltages inducing a hole ( $p$ ) channel. For clarity, the transfer curve is plotted for a constant voltage (+1 V) between source/drain terminals; note that this corresponds to bias conditions of  $V_s=0$  V and  $V_d=+1$  V for  $n$  channel, but  $V_s=+1$  V and  $V_d=0$  V for  $p$  channel. However, the current on/off ratio is low, less than 10 for both channels. This is consistent with the expected results for a narrow band gap nanowire, assuming the contact metal can efficiently inject carriers of both types. Figure 2 shows the measured  $I_{ds}$  vs  $V_{ds}$  (from 0 to  $-1$  V) at different gate biases (from  $-2$  to  $-7$  V) for  $p$  channel. The decrease in gating effect for small negative biases reflects the transition to the

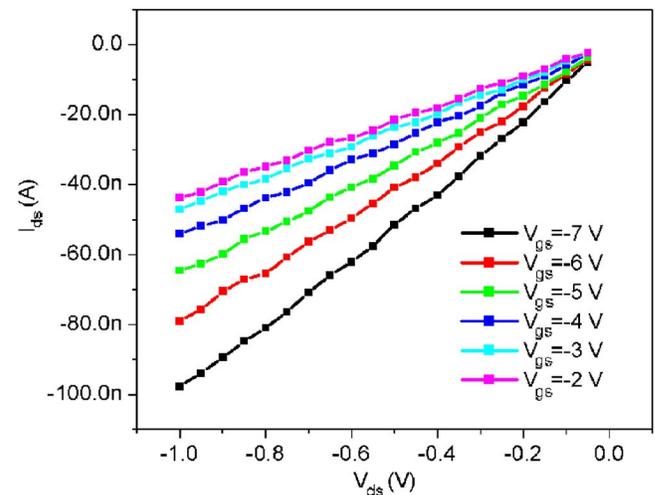


FIG. 2. (Color online) Measured source drain current  $I_{ds}$  vs source drain bias  $V_{ds}$  for a representative device.

$n$ -channel region. For the gate biases presented in this figure, the current is not expected to fully saturate until larger drain biases. The mobilities inferred from the transfer characteristic and the capacitance calculated using the cylinder on the plane model<sup>11</sup> are  $3.9$   $cm^2/Vs$  for  $n$  channel and  $8.3$   $cm^2/Vs$  for  $p$  channel. The transconductance  $g_m$  is taken from the derivative of Fig. 1 with respect to gate voltage. The mobilities inferred from this technique will include the effects of contacts between source/drain and channel, which will degrade the measured transconductance and therefore lower the mobility. The relatively low mobilities are likely due, in part, to surface scattering and ionized impurity scattering, which would arise from the large surface-to-volume ratio of the nanowires and the heavy doping level within the nanowires, respectively.

In order to investigate the contact properties between source/drain and channel, the current-voltage characteristics were measured versus temperature. Figure 3 shows an Arrhenius plot for the  $p$  channel of a device with various values of  $V_{ds}$  and a gate voltage of  $-6$  V. The relatively large negative gate voltage is chosen to ensure that the channel

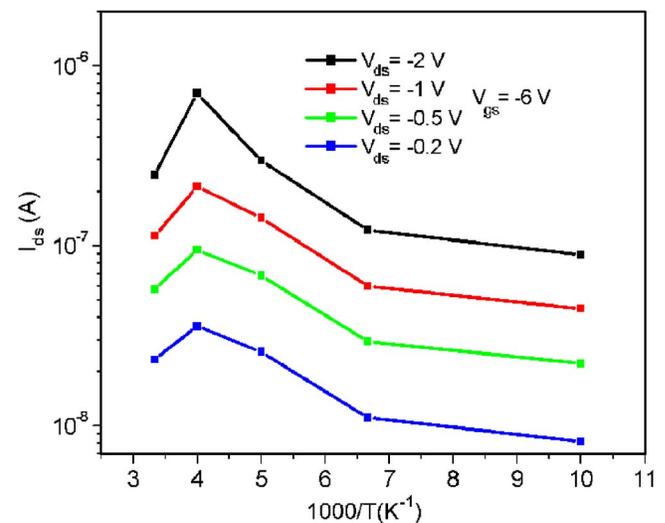


FIG. 3. (Color online) Variable temperature measurements for Cd doped InAs nanowire FET. These curves show  $I_{ds}$  vs temperature with  $V_{gs}=-6$  V and  $V_{ds}$  varying from  $-0.2$  to  $-2$  V.

remains strongly turned on at all temperatures and drain-source voltages. In this case, the contact between source and channel should dominate the temperature dependence of the conduction. From the curves, it is concluded that the average thermal activation energy for the  $p$  channel is approximately 44 meV. A comparable measurement for the  $n$  channel performed at a gate voltage of 6 V yielded an average thermal activation energy of 32 meV. At the gate bias points used in these measurements, the Fermi level in the channel approximately lines up with the conduction or valence band edge for the  $n$  channel and  $p$  channel, respectively, as inferred from the channel charge calculated from the capacitance relationship. For this bias condition, a small barrier height and therefore a small activation energy are expected as long as the contact is sufficiently transparent. These variable temperature measurements indicate that there are modest Schottky barriers (SBs) between the source/drain contacts and the channel. The SBs can explain, in part, the relatively low mobility and low on/off current ratio.

Band diagrams which can explain the observed behavior of the Cd doped InAs nanowire FETs are shown in the insets of Fig. 1. The dashed lines shown in insets (i) and (ii) represent the expected equilibrium ( $V_{gs}=0$ ) band bending, based on the effective work function of heavily  $p$  doped InAs. As gate voltage becomes more positive, the energy bands of InAs nanowire will be pulled down, and an inversion  $n$  channel will form, as shown in inset (ii). Notice that when the bands are pulled down, there will be SBs formed between the  $n$  channel and the source and drain contacts, which is consistent with our low temperature investigation. When the gate voltage becomes more negative, the energy bands will be pushed up, as shown in inset (i), resulting in an accumulation ( $p$ ) channel.

The lack of  $p$ -channel operation in InAs nanowire devices reported to date is believed to be due to surface Fermi level pinning in the conduction band. The observation of a  $p$  channel at modest negative gate voltage in our devices implies that the Fermi level is not pinned in the conduction band. The ligands which have been observed on the surface of InAs nanowires are believed to be responsible for this unpinning, either by significantly reducing the surface state density or by shifting the energies of the surface states away from the conduction band. This observation is also consistent with a prior study which used alkane thiols to passivate an InAs thin film,<sup>12</sup> which reported that the Fermi level was not pinned in the conduction band after formation of an alkane thiol self-assembled monolayer. The relatively high Cd doping level is integral to realizing  $p$ -channel conduction with current levels comparable to the  $n$  channel at modest gate biases. The heavy acceptor doping allows a significant density of holes within the channel, even in the presence of a modest surface state density or work function differences between the gate and the nanowire. Devices fabricated with nominally undoped InAs nanowires also exhibited ambipolar conduction when encapsulated by ligands, but with much lower  $p$ -channel current at comparable gate biases.

In order to verify that the Fermi level unpinning is associated with the surface-bound ligands, we have performed  $O_2$  plasma treatments of the nanowire transistors after initial electrical characterization. The  $O_2$  plasma treatment (20 s at a pressure of 1 torr, a plasma power of 100 W at an  $O_2/Ar$  ratio of 20%) is expected to remove the surface ligands and likely also induces an oxidized layer at the nanowire surface. The plasma parameters were chosen based on conditions required to remove a polymer thickness comparable to the ligand length. While this approach was employed to minimize surface damage, it is possible that lower-damage approaches could be developed. The red curve in Fig. 1 shows the transfer characteristics of the FET following  $O_2$  plasma treatment. In this case, only  $n$ -channel conduction is observed. The same estimation method is used to calculate the electron mobility in this case, which yields  $22.1 \text{ cm}^2/\text{V s}$ .

This letter demonstrates ambipolar conduction in FETs constructed from Cd doped InAs nanowires synthesized by a solution-liquid-solid method. The ambipolar characteristics are believed to be the result of unpinning of the Fermi level from the conduction band, which in turn is attributed to the passivating effects of surface ligands. In order to investigate the effects of the passivation,  $O_2$  plasma is used to remove the surface ligands. Following the plasma treatment, the InAs nanowire FETs become unipolar, exhibiting only a  $n$  channel, as reported by other groups. This indicates that the surface ligands help to passivate the surface states, resulting in the Fermi level unpinning from the conduction band. The study provides insights about approaches to realize complementary devices for InAs nanowire circuits.

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