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Ju, Sanghyun; Chen, Pochiang; Zhou, Chongwu; Ha, Young-Geun; Facchetti, Antonio; Marks, Tobin J.; Kim, Sun Kook; Mohammadi, Saeed; and Janes, David B., "1f noise of SnO2 nanowire transistors" (2008). *Department of Electrical and Computer Engineering Faculty Publications*. Paper 2.
http://dx.doi.org/http://dx.doi.org/10.1063/1.2947586

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1/*f* noise of SnO_2 nanowire transistors

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(Received 25 April 2008; accepted 24 May 2008; published online 19 June 2008)

The low frequency $(1/f)$ noise in single SnO_2 nanowire transistors was investigated to access semiconductor-dielectric interface quality. The amplitude of the current noise spectrum (S_I) is found to be proportional to I_d^2 in the transistor operating regime. The extracted Hooge's constants (α_H) are 4.5×10^{-2} at $V_{ds}=0.1$ V and 5.1×10^{-2} at $V_{ds}=1$ V, which are in general agreement with our prior studies of nanowire/nanotube transistors characterized in ambient conditions. Furthermore, the effects of interface states and contacts on the noise are also discussed. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2947586]

Building integrated nanowire transistors (NWTs) and complementary circuits using semiconducting nanowires have recently become an emerging device technology with great potential for digital and analog circuits, flexible and transparent display/communication technologies, and chemical/gas sensor elements.[1–3] The NWTs are attractive because of several unique and interesting features: (i) high performance transistor characteristics, especially enhanced field-effect mobility compared to the bulk mobility for the same semiconductor, (ii) optical transparency and mechanical flexibility, (iii) low-temperature processing (e.g., device fabrication on plastic and polymer substrates), and (iv) high-sensitivity gas/chemical sensing capabilities. Among the several known semiconducting NW materials, SnO_2 NWs have been shown to be an excellent candidate for integrating into high performance thin film transistors (TFTs), flexible and transparent NWTs, and gas sensors.[4–7] SnO_2 with a tetragonal crystal structure (lattice parameters $a=4.737$ Å and $c=3.185$ Å) is an excellent candidate for novel electronic devices thanks to the wide band gap of 3.6 eV and a high surface-to-volume ratio.[8,9] Applications include integrating high-performance TFTs, flexible and transparent NWTs, and gas sensors.[4–7] However, in order to optimize transistor performance even further, it is important to understand the NW transport characteristics and to control the semiconductor-dielectric interface properties in these NW-based devices. In this study, we report on the fabrication and performance of SnO_2 nanowire/self-assembled nanodielectrics (SAND) transistors and examine the quality of the device interfaces using the low frequency $(1/f)$ noise measurement.

Figure 1 shows the cross section of the SnO_2/SAND NWT structure. Deposition and patterning of the indium tin oxide (ITO) gate electrode was followed by deposition of a gate insulator consisting of layers periods of a SAND layer-by-layer molecular structure with a total thickness of 15 nm. Details of this self-assembly procedure SAND have been reported previously.[10,11] The SnO_2 nanowries were synthesized on a SiO_2/Si substrate covered with 10 nm gold nanoparticles, using a process performed in Ar with a trace of oxygen and employing laser ablation from a Sn target (99.99%, Alfa-Aesar). Details of the synthesis procedure have been described previously.[12] Based on subsequent imaging by field-emission scanning electron microscope (FE-SEM), the average diameter and length of the NWs are 10–50 nm and over 10 μm, respectively. The NWs are not intentionally doped, but they exhibit *n*-type transistor behavior due to donor doping by oxygen vacancies. The NWs were deposited from solution onto the surface. The FE-SEM imaging was employed to determine the number of nanowires between the source and drain contacts in each device, as shown in the inset of Fig. 1; the representative device reported in this study contains a single SnO_2 NW. The spacing between Al source and drain electrodes is ~1.5 μm. To optimize the transistor characteristics, in terms of on-current, threshold voltage, subthreshold slope and on-off ratio,[13] an ozone treatment (2 min) was performed after deposition and patterning

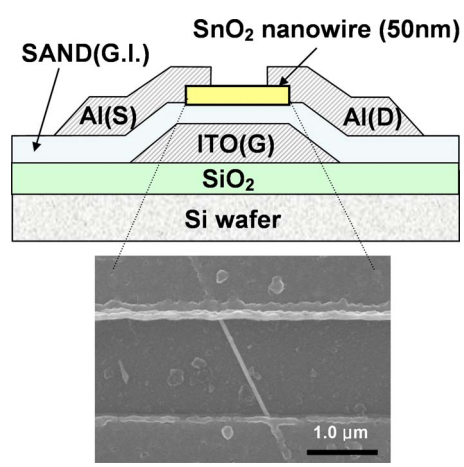

FIG. 1. (Color online) Thin-film NWT geometry with an ITO bottom gate and an organic SAND as the gate insulator. Electron micrograph of single SnO_2 nanowire between Al source/drain contacts in this device.

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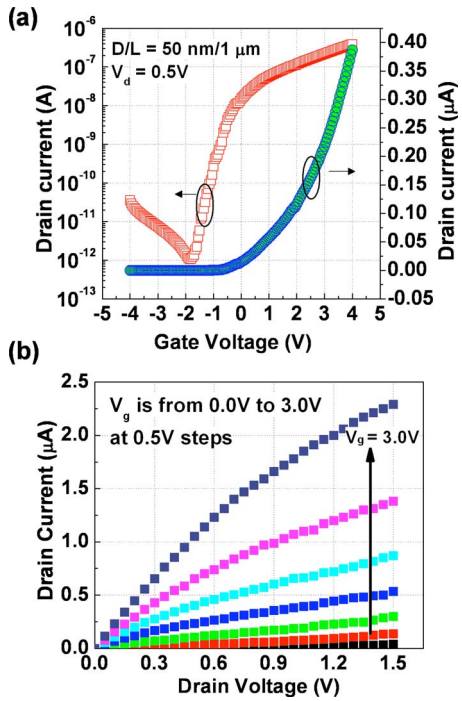

FIG. 2. (Color online) (a) Measured transfer curves (linear and semilog scales) for representative NWT at V_{ds}=0.1 V. (b) Measured drain current vs drain-source voltage for same device.

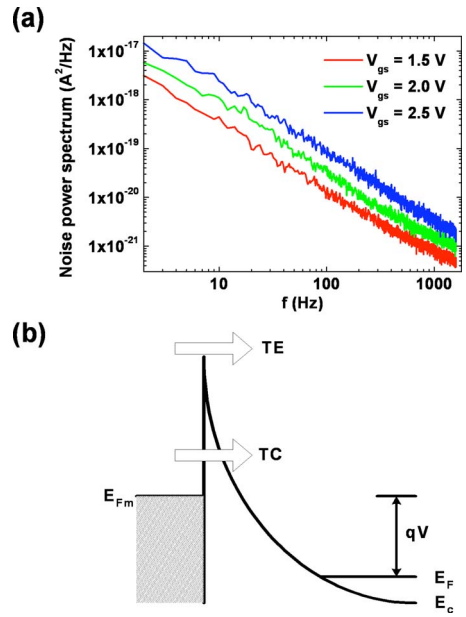

FIG. 3. (Color online) (a) Measured drain current noise spectrum of SnO_2 NWT as a function frequency for indicated gate biases at constant drain bias of 0.1 V. (b) Energy-band diagram of Schottky barrier (metal to n-type degenerate semiconductor) under reverse bias. (T_E=thermionic emission, T_C=tunneling current.)

of the source-drain contacts, modifying the unmetallized surfaces of the nanowires. Low frequency noise $(1/f)$ characteristics were then measured in ambient using a SR 570 current amplifier and a HP 3561 A dynamic signal analyzer.[5]

Figure 2(a) shows the measured drain current versus gate-source voltage (I_{ds}-V_{gs}) characteristics on both linear and semilog scales for a representative SnO_2 NWT. The device exhibits a subthreshold slope (S) of ~0.3 V/decade, an on-off current ratio (I_{on}/I_{off}) of 10^6, and a threshold voltage (V_{th}) of −1.9 V. The drain current versus drain-source voltage (I_{ds}-V_{ds}) characteristics of the same NWT are shown in Fig. 2(b), exhibiting a I_{on} ~2 μA at V_{ds}=1.2 V, V_{gs}=3.0 V, respectively. The field-effect mobility ($\mu = dI_{ds}/dV_{gs} \times L^2/C_i \times 1/V_{ds}$) is extracted from transconductance ($g_m \sim 1.78 \times 10^{-7}$ S at V_d=0.5 V) and the calculated gate-to-channel capacitance $[C_i = 2\pi\varepsilon_0 k_{eff} L/\cosh^{-1}(1+t_{ox}/r)]$, using the effective dielectric constant of the SAND ($k_{eff} \sim 3.0$), the device channel length ($L \sim 1.5$ μm), and the NW radius ($r \sim 25$ nm). The capacitance is $C_i = 2.391 \times 10^{-16}$ F and the peak value of μ is ~172 cm^2/V s. This mobility is considerably higher than recently reported SnO_2 thin film and NW mobilities in the range of 40–100 cm^2/V s.[12,14]

Low frequency noise measurements were carried out to study current fluctuation by examining the correlation bias and amplitude of the $1/f$ noise. Figure 3(a) shows the current noise power spectrum (S_I) as a function of gate bias at a constant drain bias of 1.0 V. In the low frequency regime, S_I varies as $f^{-\beta}$, where the exponent β ranges between 1 and 1.15.

According to Hooge's empirical model, the $1/f$ noise can be expressed by

$$S_I(f) = \frac{\alpha_H \times I_d^2}{f \times N}, \tag{1}$$

where α_H is the Hooge's constant, I_d is the drain current, and N is the total number of carriers in the NWT channel. The equilibrium charge in the case of strong inversion or strong accumulation, when V_{gs} exceeds V_{th}, is given by

$$Q_N = Nq \cong -C_i(V_{gs} - V_{th}), \tag{2}$$

where the calculated gate-to-channel capacitance (C_i) is $\sim 1.593 \times 10^{-16}$ F. Combining Eqs. (1) and (2), the current noise power spectrum in strong inversion regime can be calculated via Eq. (3).

$$S_I = \frac{AI_{ds}^{\beta}}{f} = \frac{q\alpha_H I_d^2}{|V_{gs} - V_{th}| C_i f} \quad (\text{where } 1/A = C_i/q\alpha_H|V_{gs} - V_{th}| = N/\alpha_H). \tag{3}$$

In order to investigate the source of the $1/f$ noise, S_I at 100 Hz and the normalized square of the drain current $[I_d^2(V_{gs} - V_{th})]$ are plotted versus gate voltage in Figs. 4(a) and 4(b), for gate-source biases of 0.1 and 1.0 V, respectively. Since the carrier concentration should be proportional to $(V_{gs} - V_{th})$, the I_d^2 is effectively normalized to the carrier concentration in the NW. Figures 4(a) and 3(d) show that the noise amplitude is approximately proportional to the normalized I_{ds}^2, which is similar to that reported for one dimensional carbon nanotube transistors (CNTs) and ZnO NWTs.[15,16] The gate bias dependence of the $1/f$ noise amplitude calculated from Eq. (3) is in excellent agreement with our experimental data.

From the experimental data and Eq. (3), α_H values of 4.5×10^{-2} and 5.1×10^{-2} are calculated at V_{ds}=0.1 and 1 V, respectively. The similar α_H values verify that gate dependence at the device is more affected by excess noise than drain dependence. Reported α_H value for nanowire/nanotube transistors include CNT ($\alpha_H \sim 9.3 \times 10^{-3}$) and ZnO NWTs

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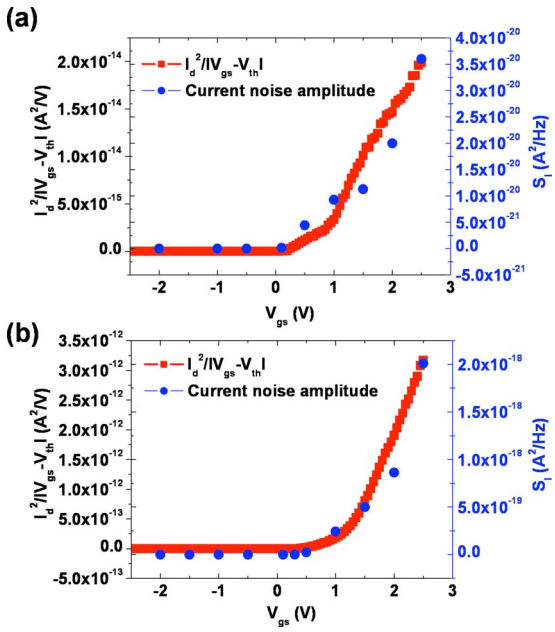

FIG. 4. (Color online) Measured $I_d^2/(V_g - V_t)$ and the amplitude of current noise spectrum at 100 Hz plotted as a function of gate bias at drain biases of 0.1 V (a) and 1 V (b), respectively.

($\alpha_H \sim 5\times 10^{-3}$) measured in ultrahigh vacuum (UHV),[15,16] and ZnO NWTs measured in air (2–4× increase with respect to UHV).[16] Another study on ZnO NWTs showed the use of the SAND dielectric resulted in a reduced α_H value with respect to that of devices with a SiO_2 gate dielectric.[17] The α_H of SAND-based SnO_2 NWT is comparable to the prior reported values for NWTs in ambient. In the present study, the ozone treatment is believed to greatly reduce the surface/interface state density, as evidenced from improvements in subthreshold slope. The ozone postannealing process is believed to improve the nanowire-metal interface, lowering the Schottky barrier. These factors are both expected to reduce the $1/f$ noise with respect to untreated devices.

The $1/f$ noise in a NWT may contain contributions from (i) excess noise in the metal-nanowire Schottky barrier and (ii) interaction of carriers with charges associated with oxide charges, interface traps, and mobile ions, which can be modified by ambient conditions. In the first case, the room-temperature charge-transport mechanism is governed by thermionic emission and/or tunneling, e.g., by thermionic-field emission, through the source contact, as illustrated in Fig. 3(b). The barrier is primarily modulated by gate voltage, but can also be modulated by the fluctuation of surface charge near the interface and charge density of trap centers located in the space charge region. The resulting fluctuations in the barrier lead to a fluctuation in the current flowing in the channel. The second case is the one typically considered in metal-oxide-semiconductor field-effect transistors in which contact effects play a relatively small role in the overall transport. In this case, carrier populations in the channel are modulated by trapping-detrapping processes involving charges in the oxide and interface traps. While it is difficult to drawn quantitative comparisons between these two effects, or between surface/interface state effects in devices employing various material systems and nanowire diameters, the relative effects of interface states appear to be comparable to those in previous studies.

In conclusion, high performance SnO_2/SAND NWTs were fabricated, and the interface quality of SAND-based SnO_2 NWTs was examined by low frequency noise measurement. The $1/f$ noise results show expected dependences on gate bias and channel current, with measured values for α_H of 4.5×10^{-2} at $V_{ds}=0.1$ V and 5.1×10^{-2} at $V_{ds}=1$ V. The SAND dielectric and various surface treatments and annealing steps were employed in order to reduce the interface state densities, and therefore, to achieve acceptable noise densities.

This work was supported in part by the NASA Institute for Nanoelectronics and Computing (NCC 2-1363) and by the National Science Foundation under NIRT Grant No. ECE-0506802.

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